Status Report on the PCI-NIM Based DAQ System

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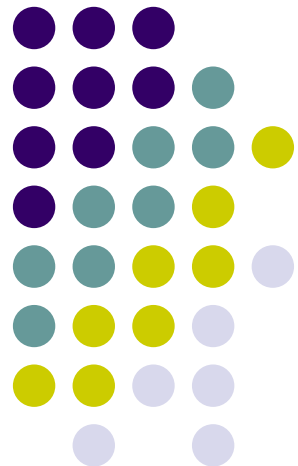
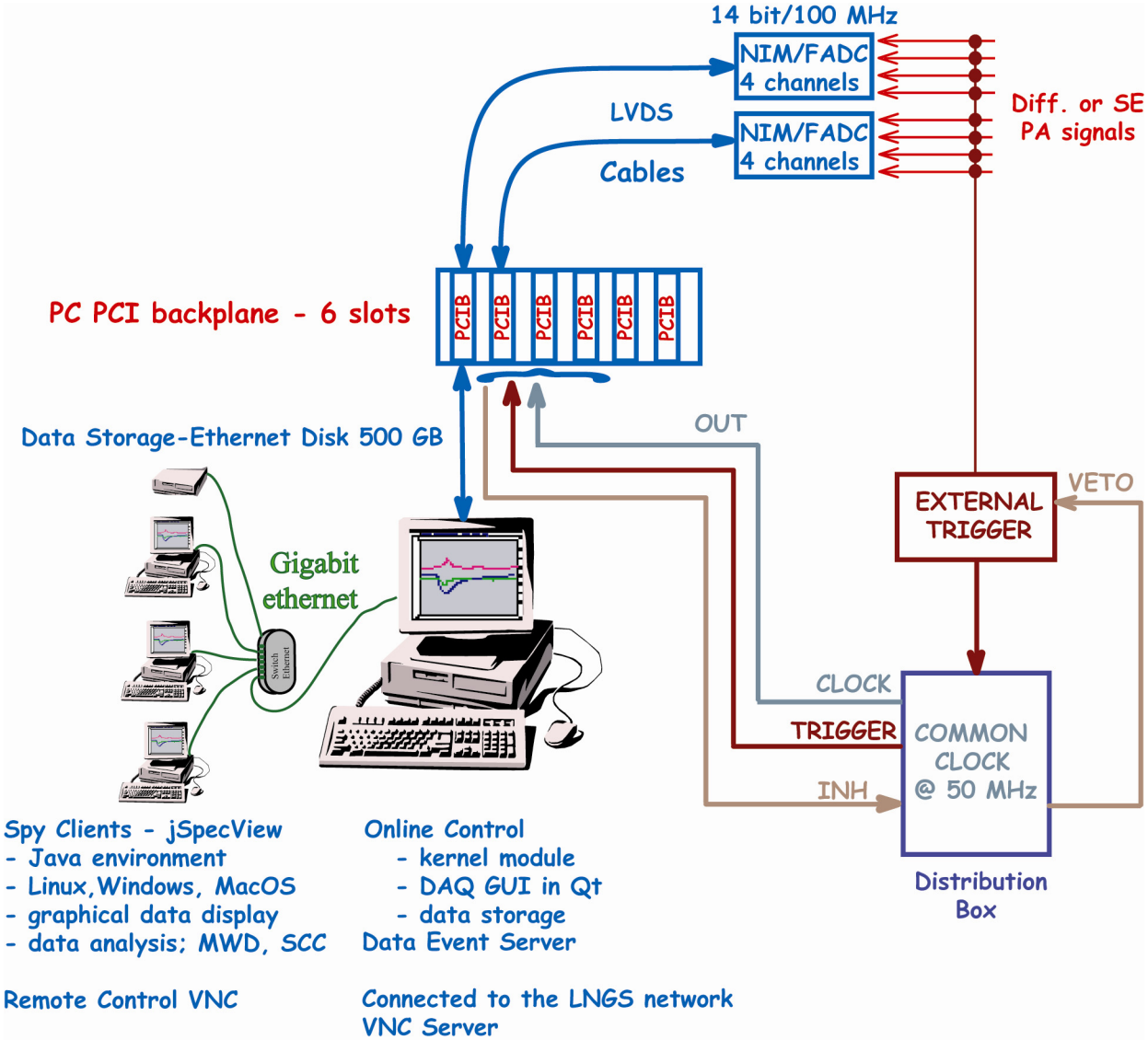


System Installed at LNGS - 2006



Main Features and Problems in 2006

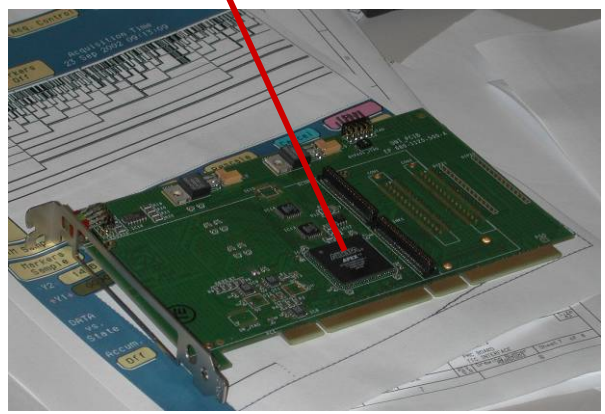
	MD2S Padova
Channels	4/module
FADC bits	14 (13)
FADC rate (MHz)	100
FPGA k-gates/ch	100
Internal trigger	no
Trace length (samples)	max 2048
Control & i/f	NIM/PCI
Data xfr	PCI 32bit/33MHz
Max output rate (MB/s)	6

Limited FPGA resources

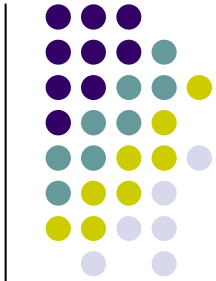
Obsolete Core PCI

Interrupt based RO

ALTERA APEX 20K200EFC484
200.000 Gates,
up to ~13 Kb of memory



Solutions



- tried to implement DMA RO → failed !

- updated the core PCI → PCI transfer at 32bit/66MHz

→max.output rate = 10 ÷ 12 MB/s

-2048 samples (10 ns) → 20 μs of signal + baseline

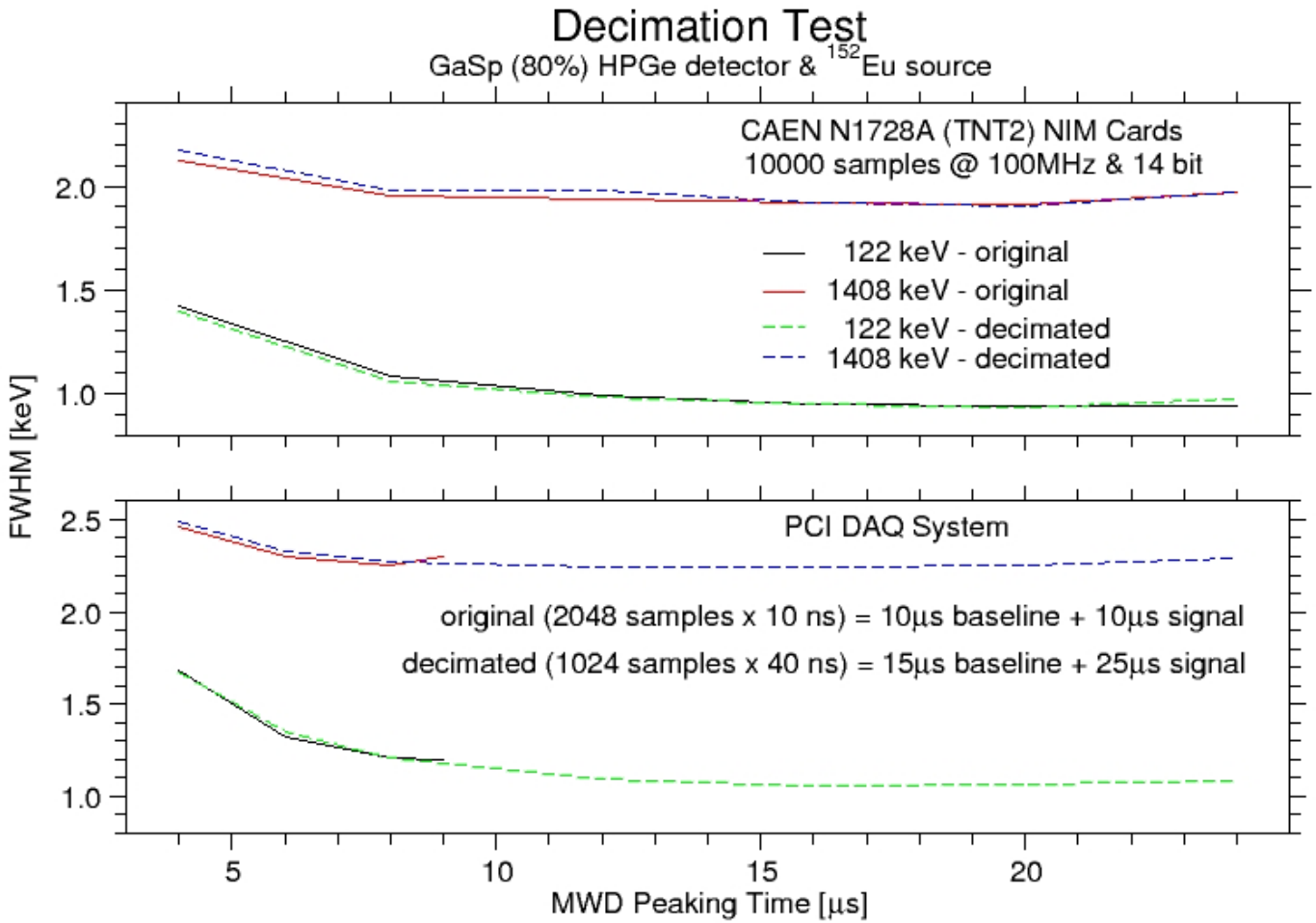
→ limit in equiv. shaping time (energy resolution)

→ decimation = sum 4 samples together (14bit → 16bit words)

- test in software (TNT2 digital data)

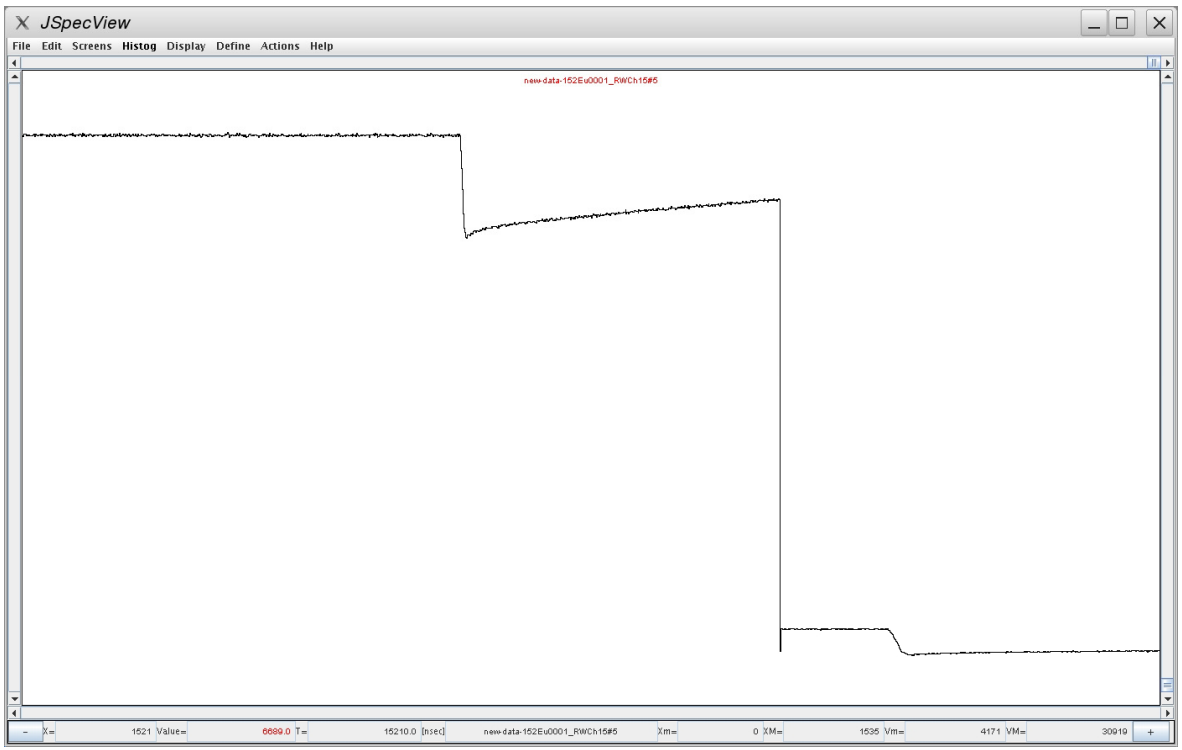
- implement the algorithm in hardware (FPGA)

Decimation

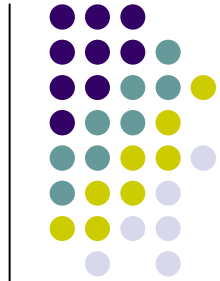

Decimation Test
GaSp (80%) HPGe detector & 152Eu source
CAEN N1728A (TNT2) NIM Cards
10000 samples @ 100MHz & 14 bit
122 keV - original
1408 keV - original
122 keV - decimated
1408 keV - decimated
PCI DAQ System
original (2048 samples x 10 ns) = 10µs baseline + 10µs signal
decimated (1024 samples x 40 ns) = 15µs baseline + 25µs signal
FWHM [keV]
MWD Peaking Time [µs]

New Data Format

- 1536 samples long waves/channel
  - -1024 (40 ns) decimated –for energy
  - - 512 (10 ns) original – for timming & PSA
    - → conserve the information on 14 bit for PSA
    - → 40 μs for extracting energy information



New Data Format

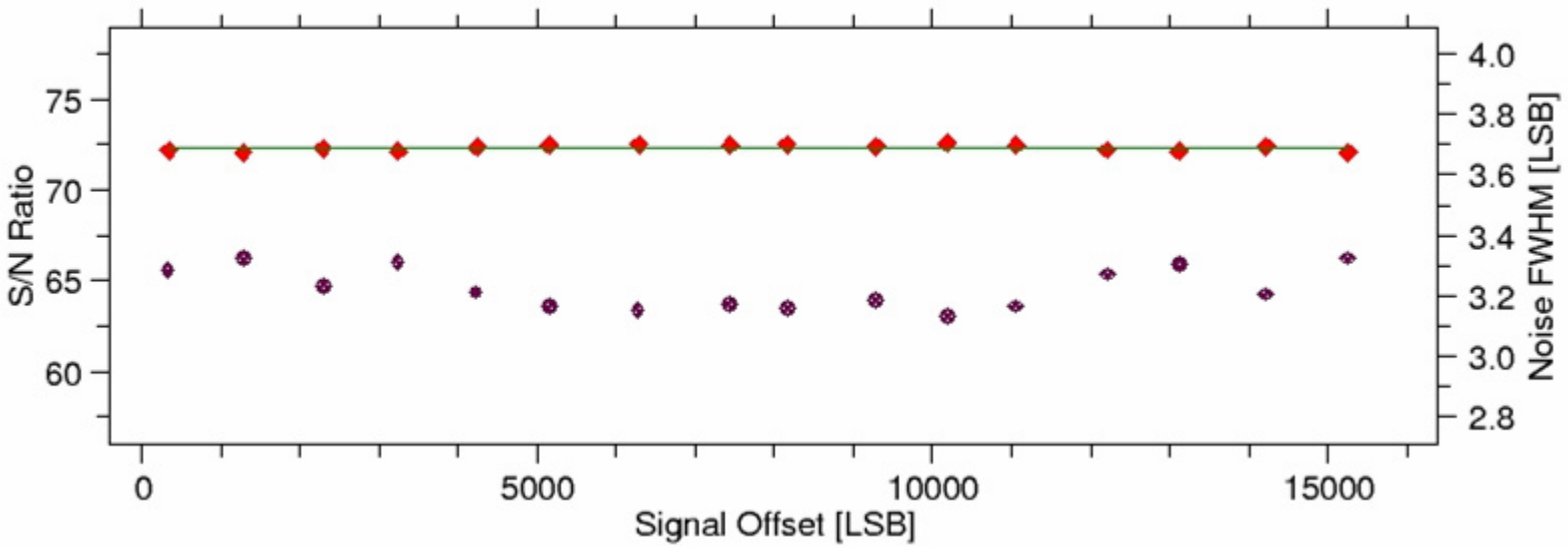


- implemented hardware (FPGA)
  - trigger counter
  - 32 bit time stamp

- in progress – modification of the GUI to control the new features of the system
  - modification of jSpecView to analyze the data in the new format

Effective Number of Bits

Noise measurement without input signal

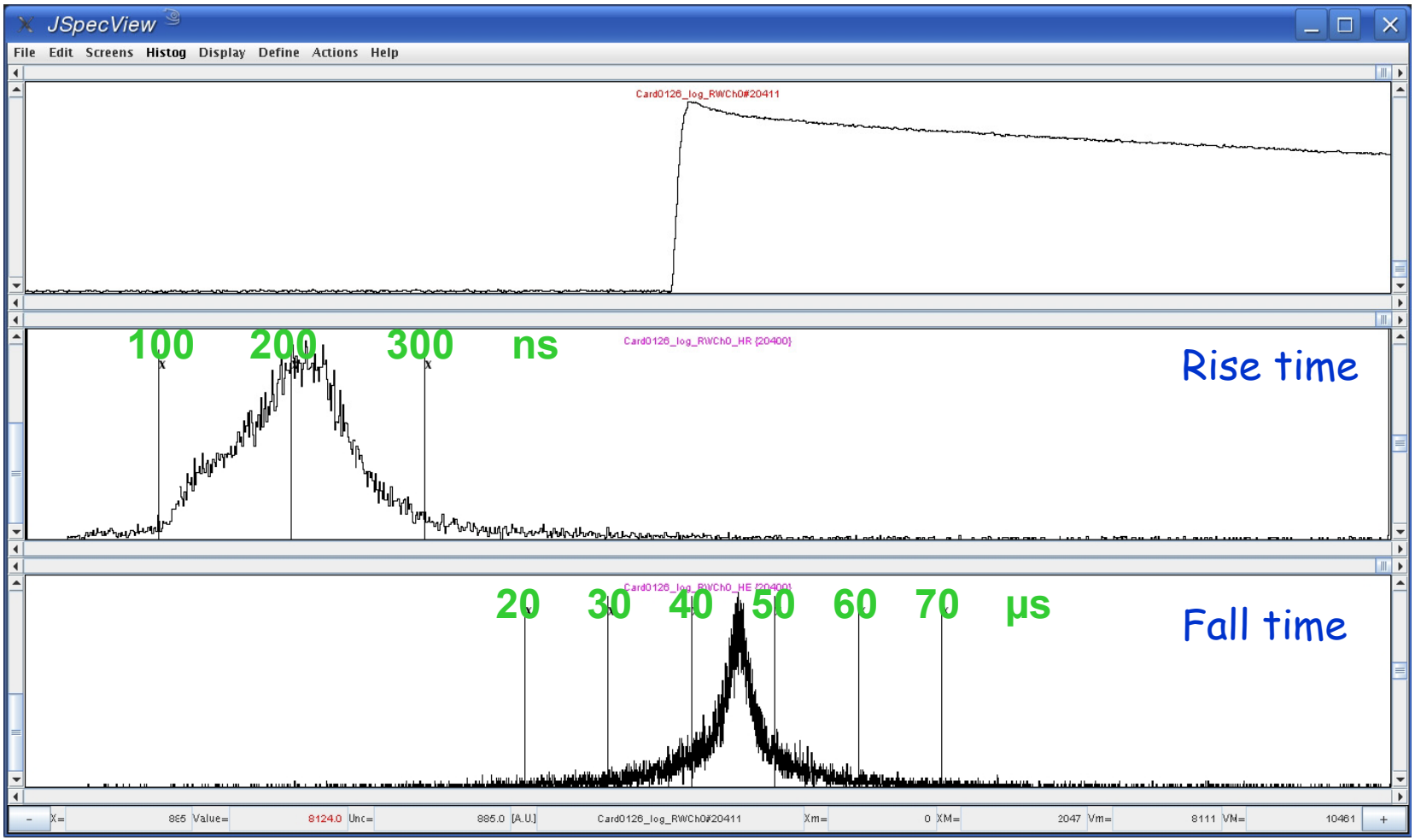


$S/N = 20*\log(FS_{rms}/\sigma) = 6.02*ENOB + 1.76$

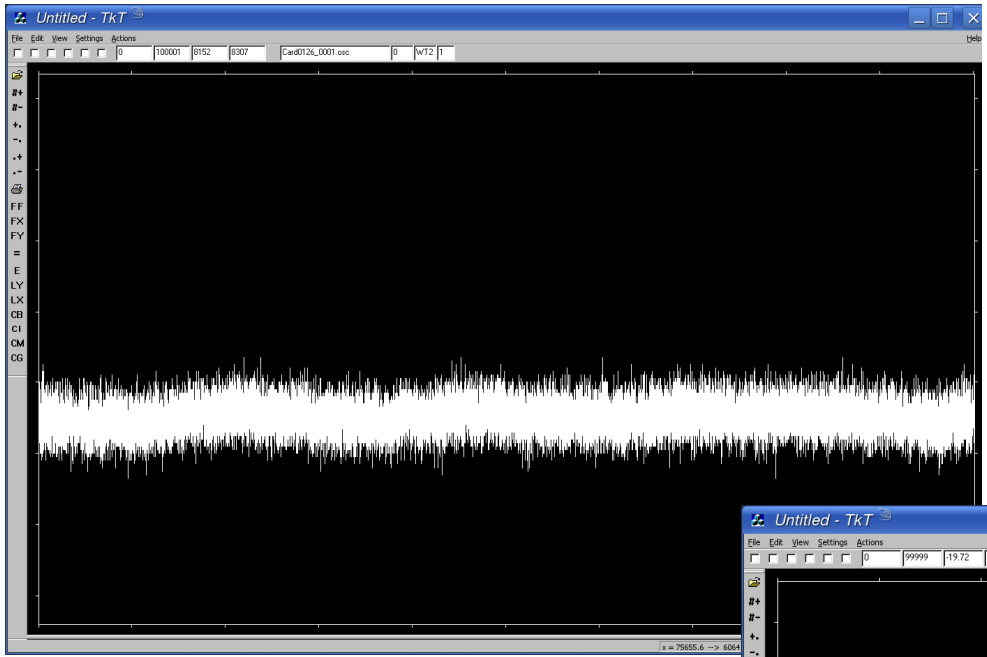
$\langle S/N \rangle = 72.3 \rightarrow ENOB = 11.7$

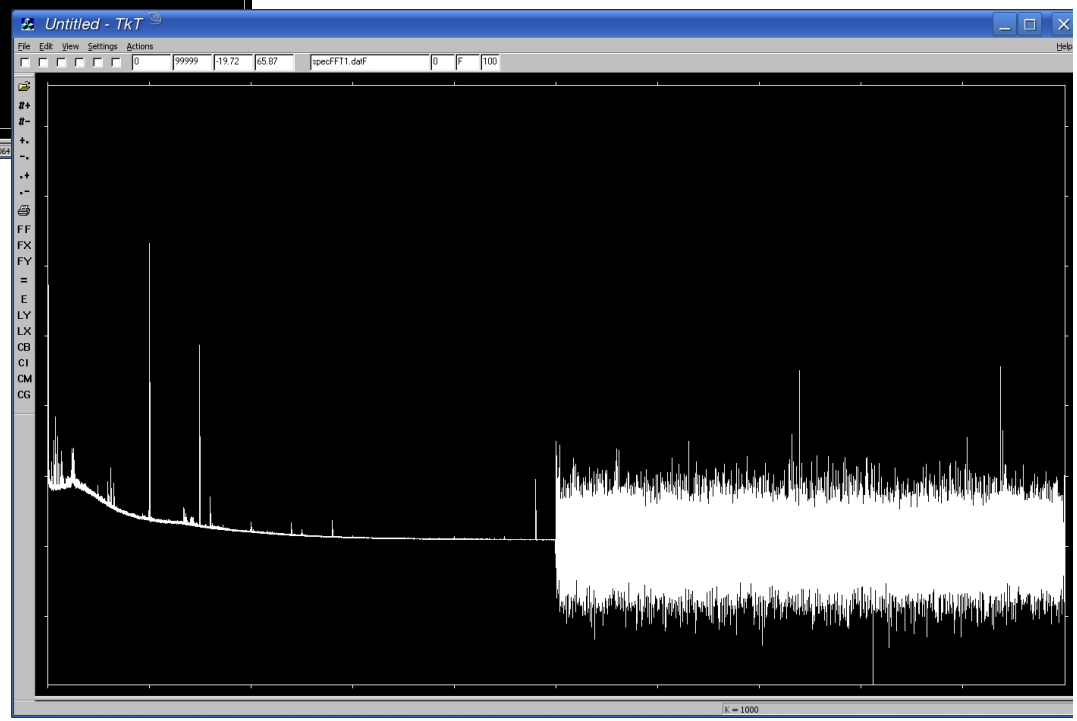
Analysis Program - jSpecView

Histogram signal rise times



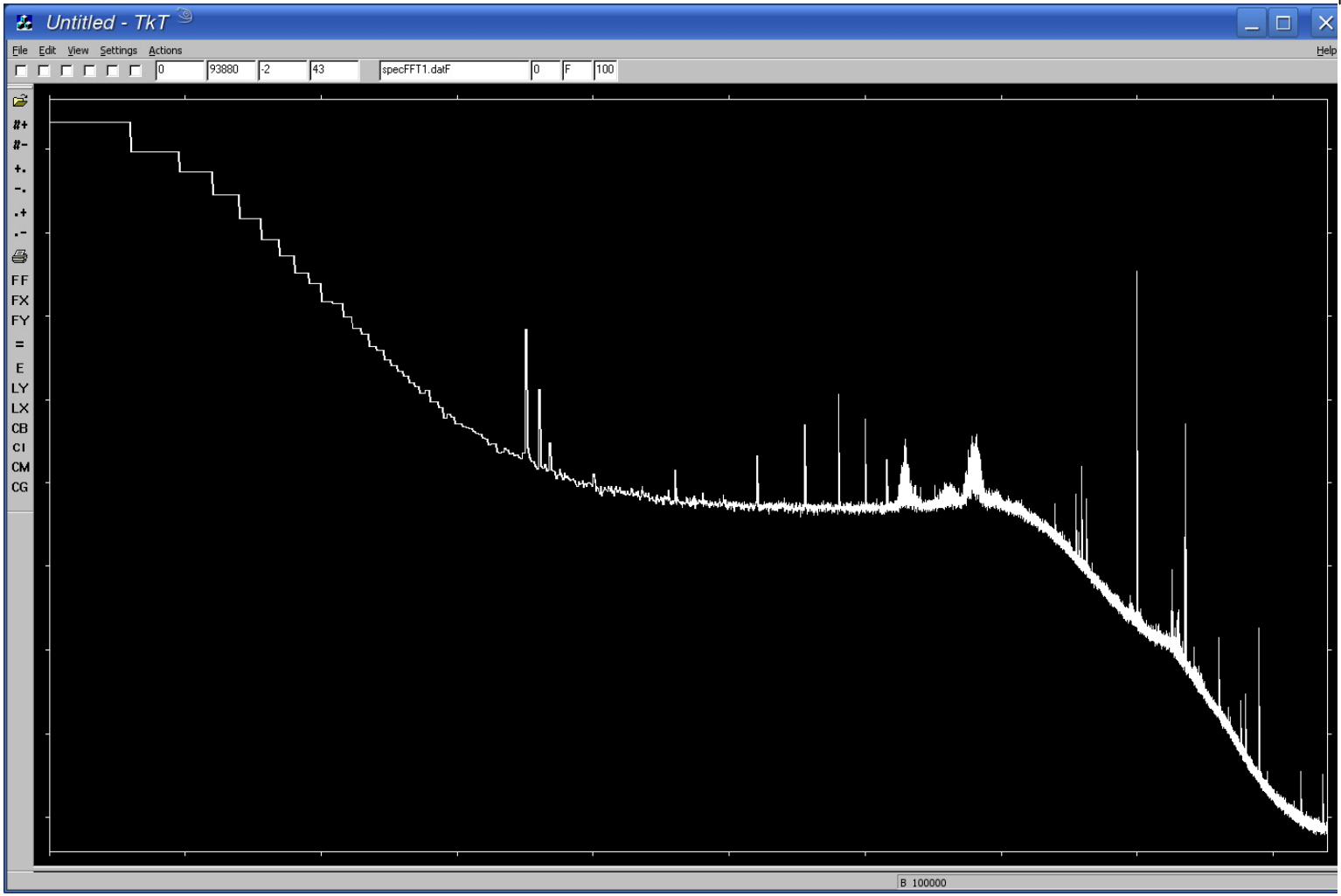
DFT – Analysis





DFT – Analysis

Bode plot → noise identification & antialias filter optimization



Status & Perspectives

- modified the PCI – DAQ
  - to recover 14 bit for PSA
  - longer shaping times possible for energy reconstruction
  - PCI transfer at 66 MHz

- implement the new firmware in the PCI boards at LNGS
- modify the control interface (Qt)
- design & optimize the antialiasing circuits (DFT analysis)
- provide the signals for the external trigger
- implement trigger algorithm in FPGA?

Website: http://agata.pd.infn.it Digital DAQ