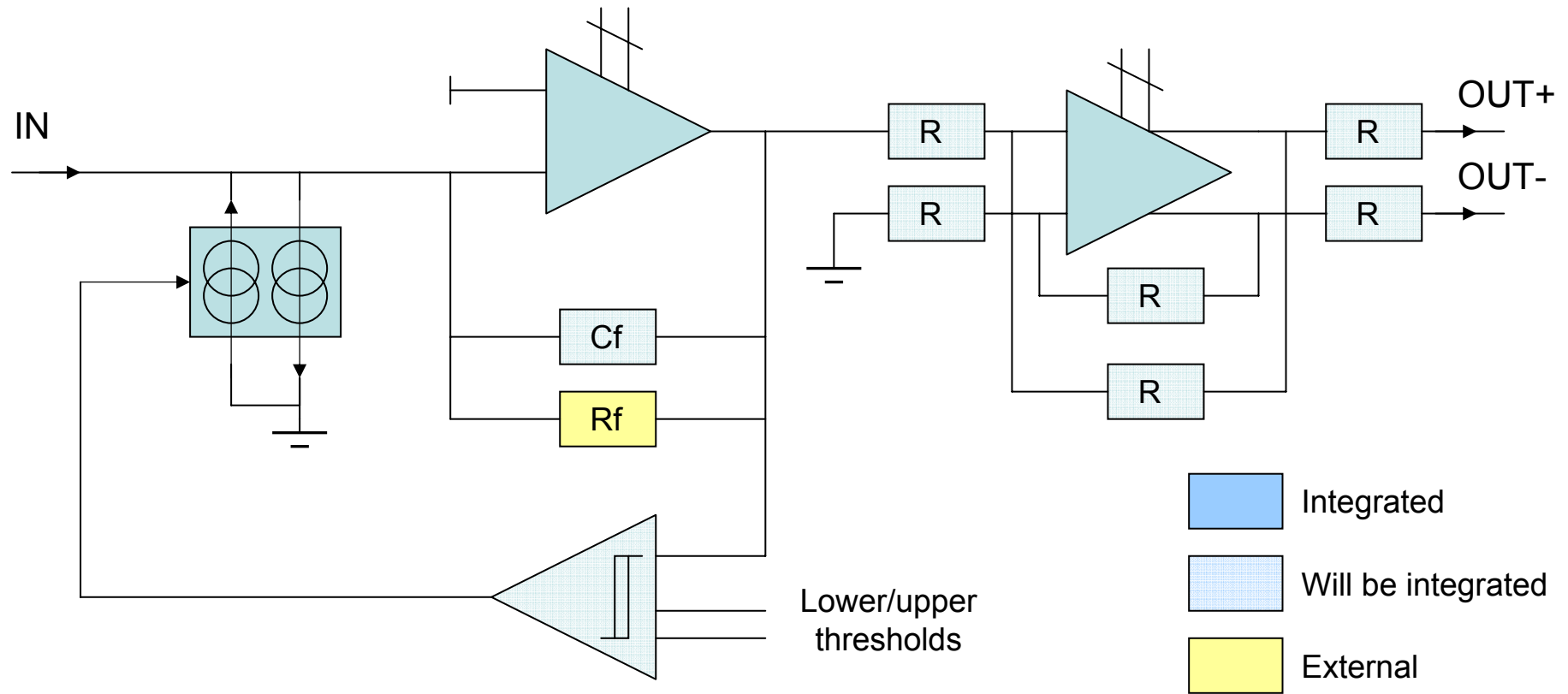S. Riboldi, A. Pullia, F. Zocca,
C. Boiano, R. Bassini, C. Cattadori

Charge Preamplifier with Fully Differential Line Driver Integrated in AMS CMOS 0.8um CZX Tech. for the GERDA Experiment
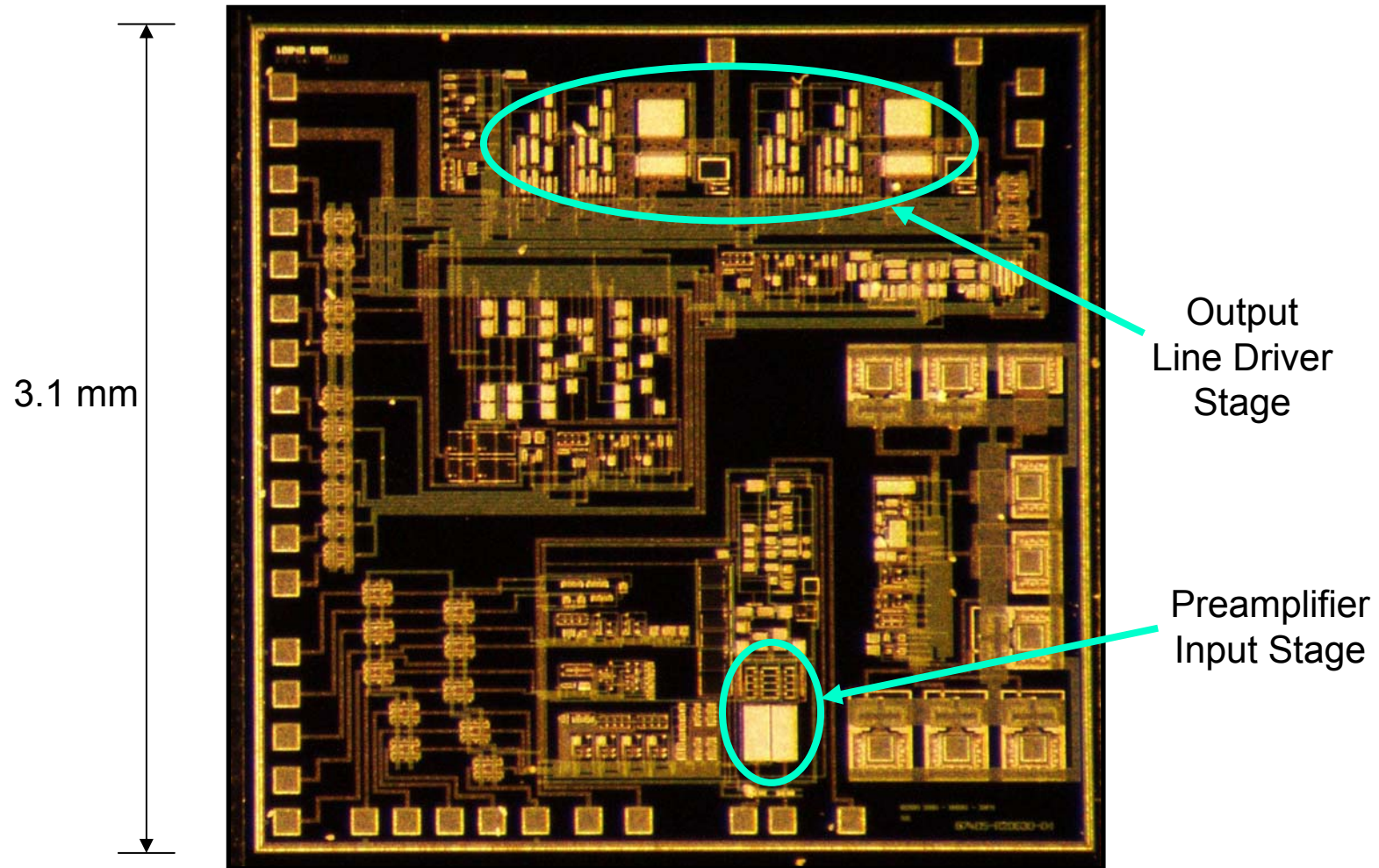
Schematic design

Legend:
- Integrated
- Will be integrated
- External

- Dual Power Supply (+2.5v / -2.5v), no additional Vref required
- Fully Differential Circuit Design for both Preamp. and Line Driver
- Tunable system
- Can operate with continuous reset (external Rf) or pulsed reset

PZ1 IC Layout

3.1 mm

Output Line Driver Stage

Preamplifier Input Stage

# Planned activity

- Manufacturing of the preliminary board :   Done

- IC Functionality test :   Done
  Separate test of Preamplifier (PRE) and Differential Line Driver (DLD)
  Results show that Bandwidth and Noise of PR are not limited by DLD

- Preliminary characterization of PRE+DLD with Rf :   Done
  Analysis of: Bandwidth, Noise, (Linearity TDB with prototype board)

- Manufacturing of the prototype board (2 layer PCB) :   TBD
  (Suitable also for operation @ T=77K)

- Characterization of PRE+DLD with Rf and Pulsed Reset :   TBD

- Charact. of PRE+DLD with Rf and Pulsed Reset @77K :   TBD
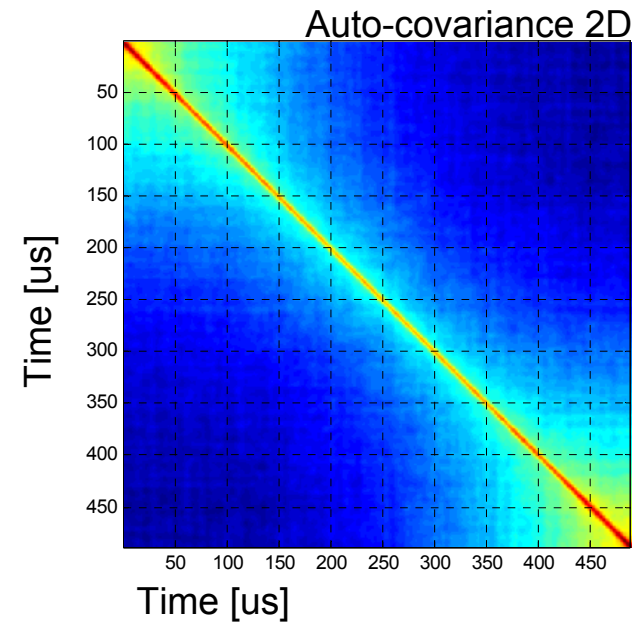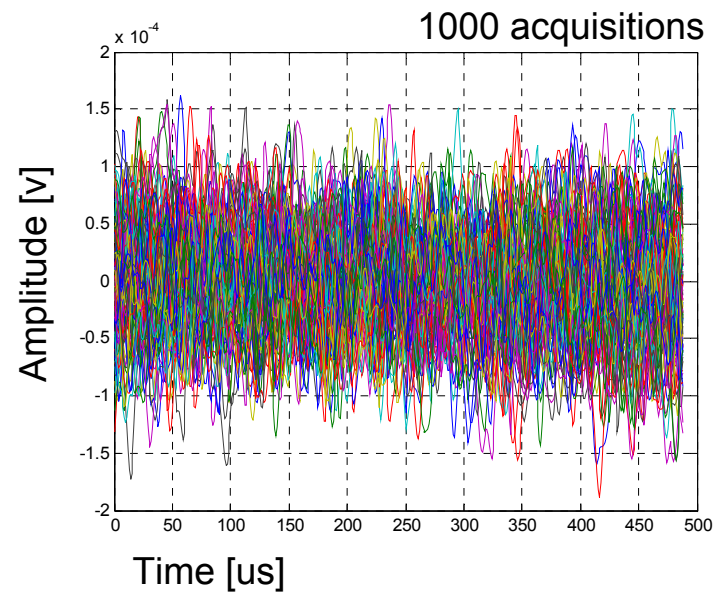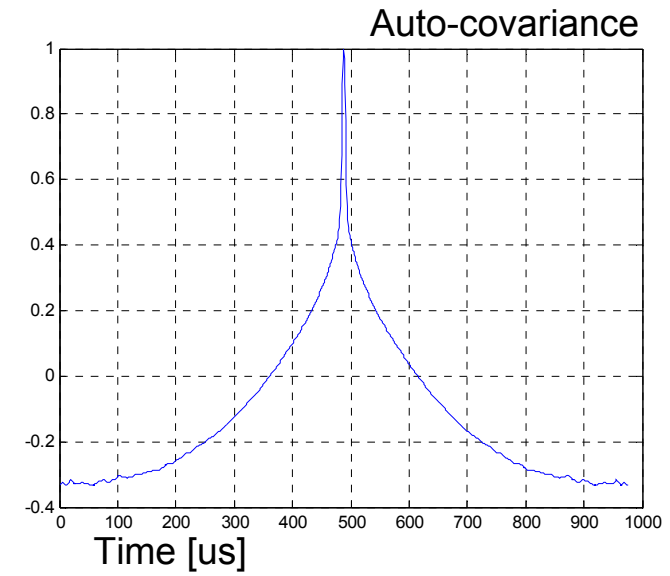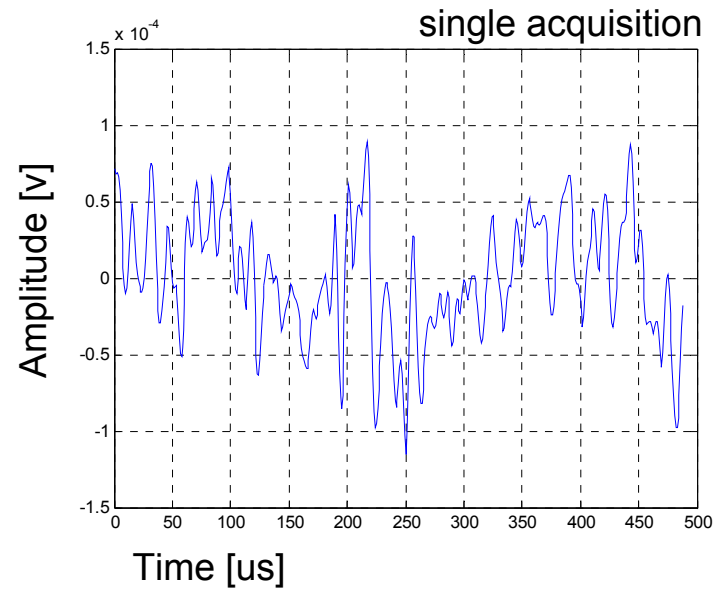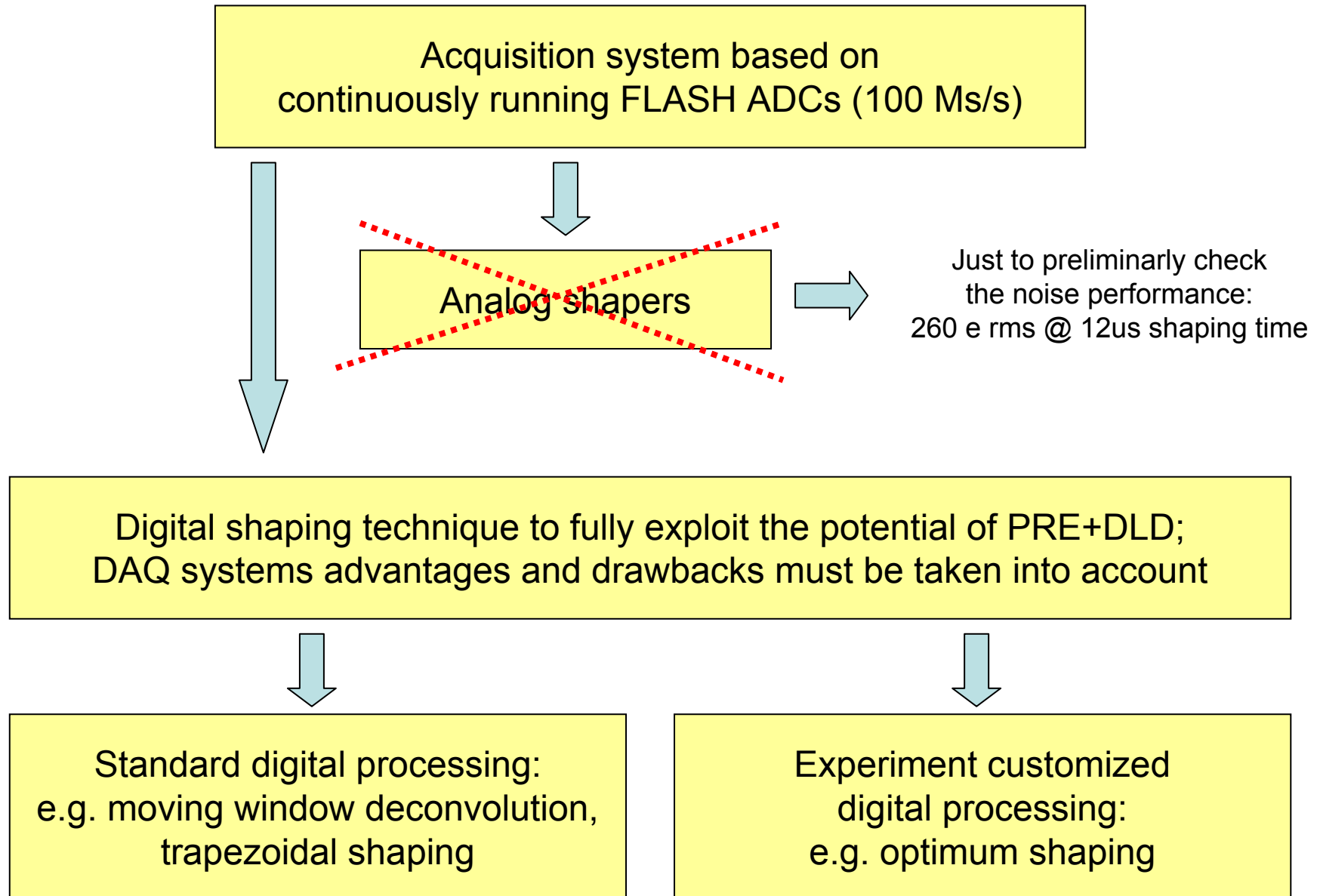
Preliminary IC board
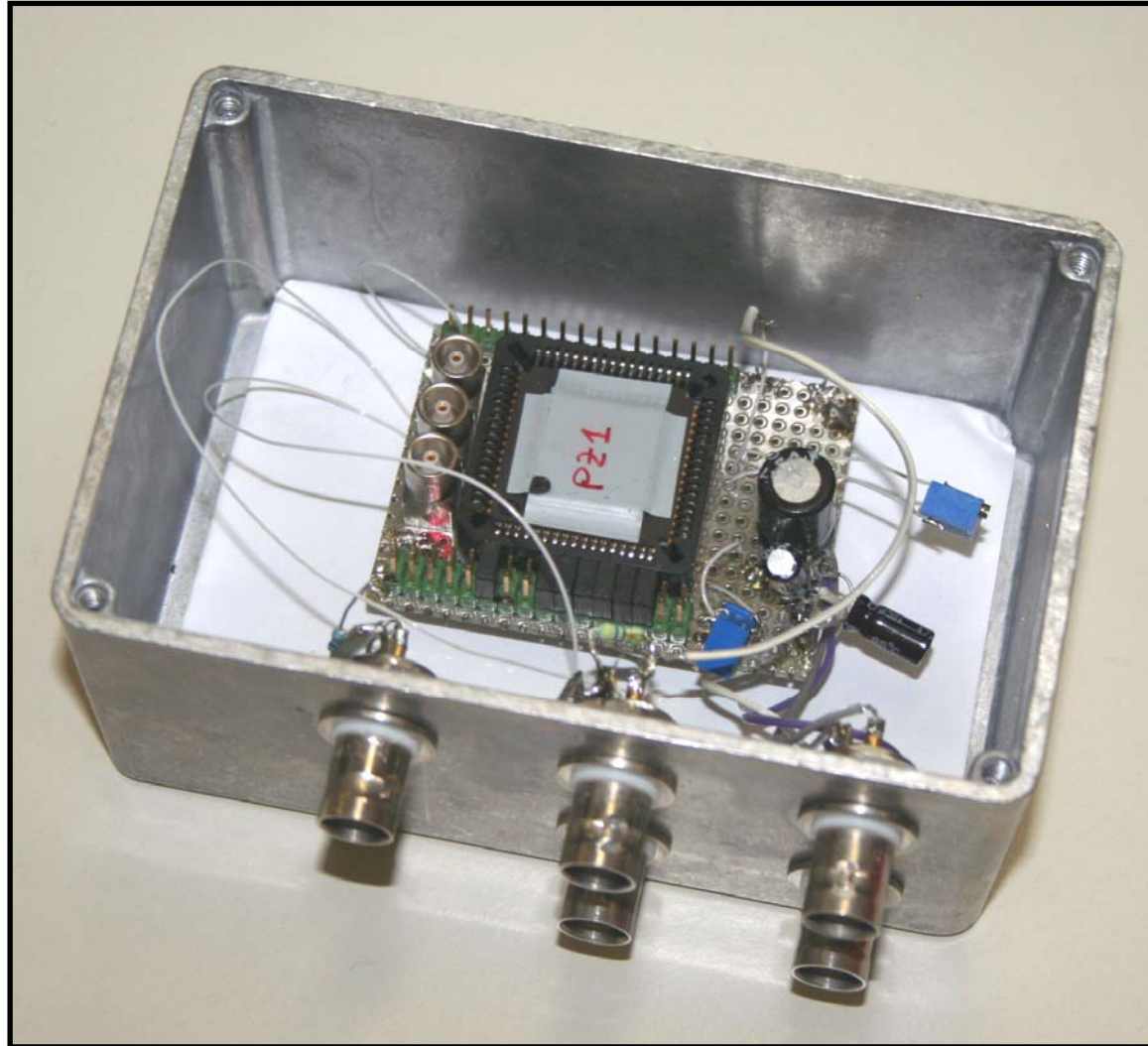
PRE+DLD Output (+)
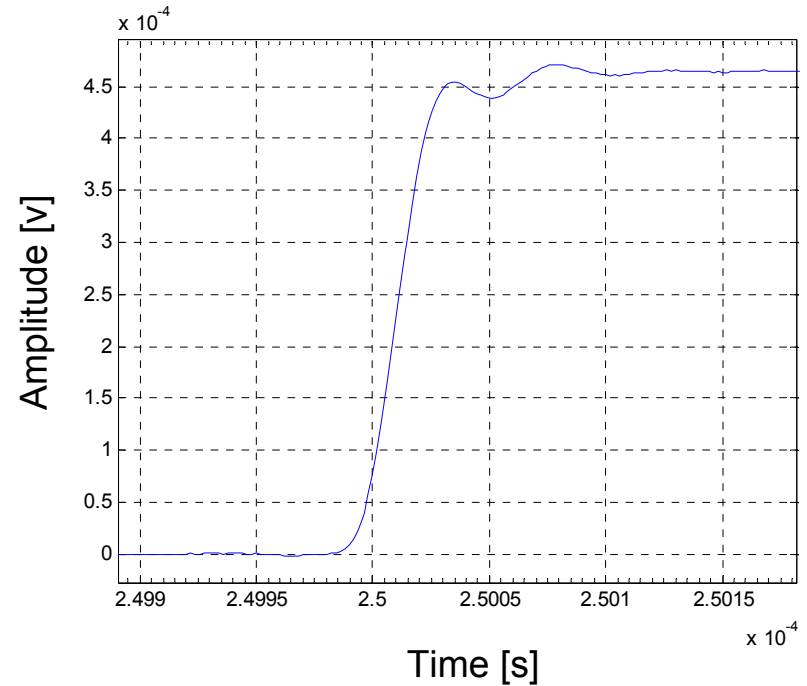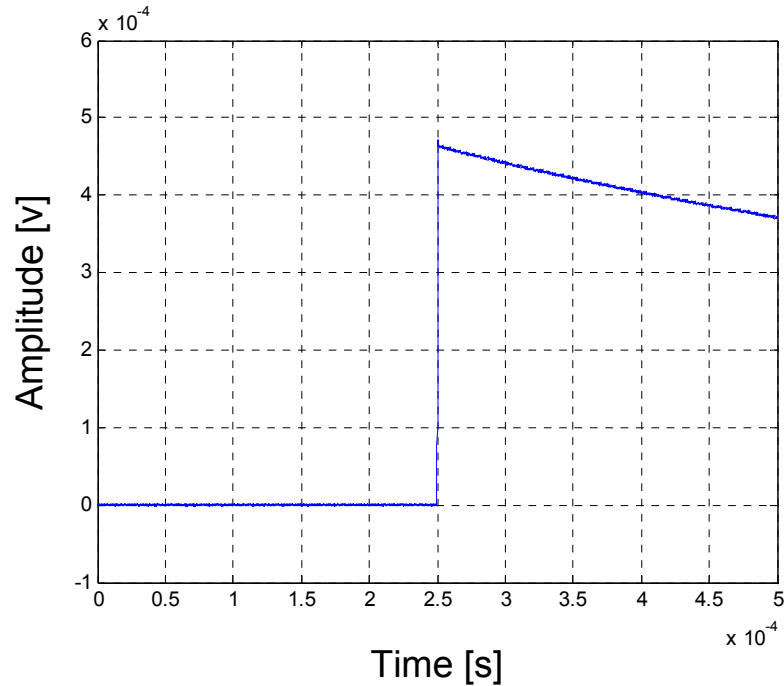
Pulse amplitude ≈ 1 Mev in Ge

50 Ohm load after 4 meters of 50 Ohm coaxial cable
Rise time ≈ 24 ns (27 ns for 2 v, maximum pulse amplitude)
Dynamic range ≈ 40 Mev in Ge
Fall time ≈ 1.2 ms (C_f ≈ 1.2 pF; R_f ≈ 1 Gohm)

Noise analysis

PRE+DLD signal shaping: how to?

Acquisition system based on
continuously running FLASH ADCs (100 Ms/s)

Analog shapers

Just to preliminarly check
the noise performance:
260 e rms @ 12us shaping time

Digital shaping technique to fully exploit the potential of PRE+DLD;
DAQ systems advantages and drawbacks must be taken into account

Standard digital processing:
e.g. moving window deconvolution,
trapezoidal shaping

Experiment customized
digital processing:
e.g. optimum shaping

PRE+DLD signal shaping: how to?

Filter synthesis by

DPLMS *
Digital
Penalized
Least
Mean
Squares

+

PRE+DLD signal

+

PRE+DLD noise

+

CONSTRAINTS

PRE+DLD signal

DIGITAL SHAPER

PRE+DLD SHAPED signal
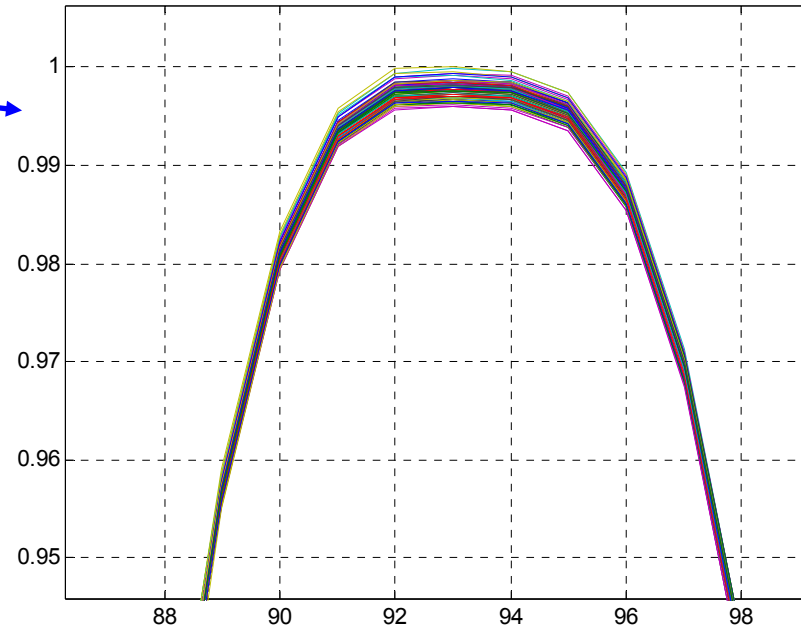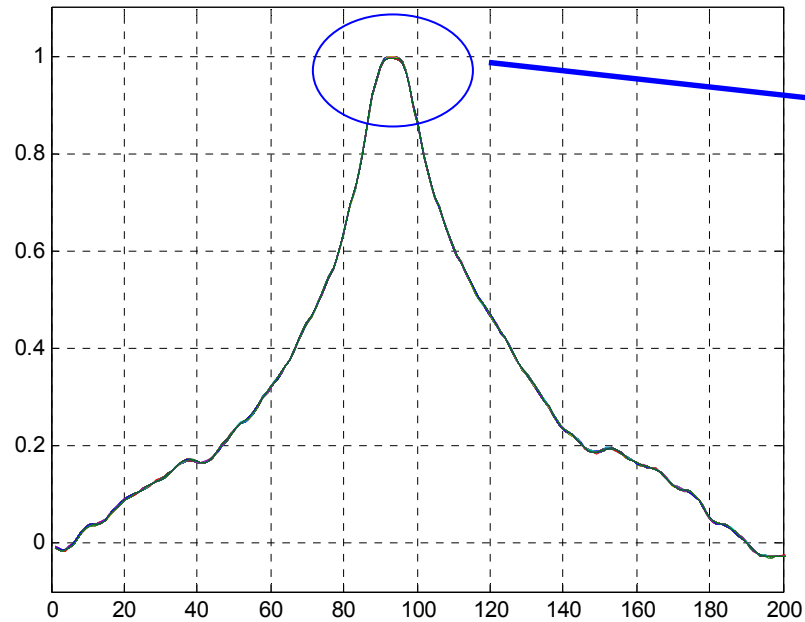
* A new method for LMS synthesis of optimum finite impulse response
(FIR) filters with arbitrary time and frequency constraints and noises. IEEE TNS, 2003

PRE+DLD SHAPED signal

Characteristics of shaped signals:
(1000 pulses with amplitude ≈ 1 Mev in Ge shown)

- Evidence of TRUE FLAT TOP (3 samples large, as required)
- FINITE DURATION (200 samples, as required)
- Evidence of $1/(f)^n$ NOISE (cusp-like shaped signal)

Preliminary noise estimation
of PRE+DLD SHAPED signals
vs SHAPING time

PRE+DLD SHAPED signal noise

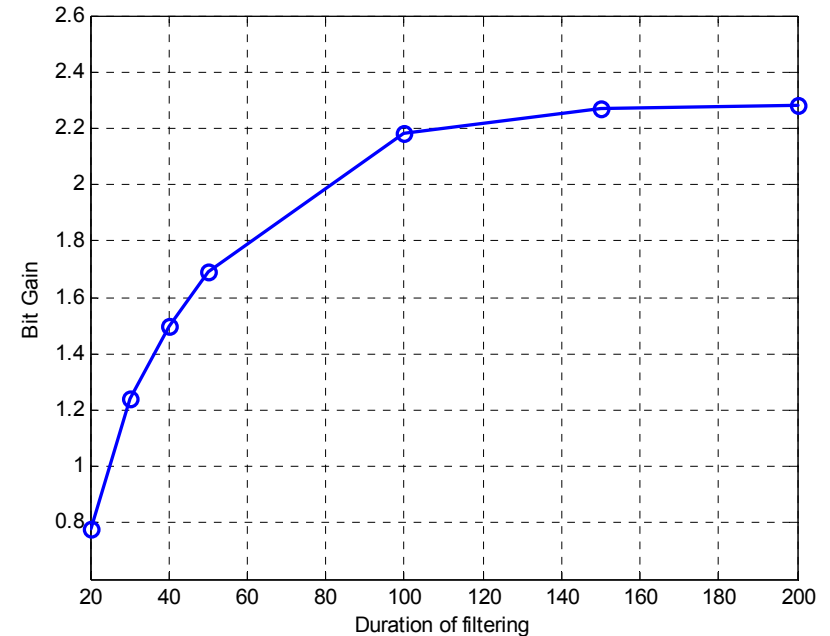

BIT GAIN of DPLMS shaping filter
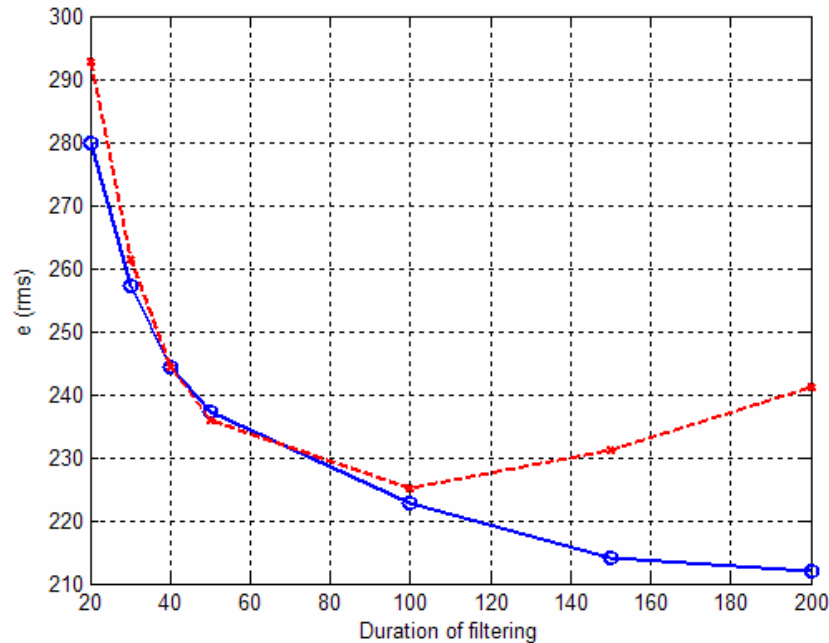
BLUE marker: shaping filter by DPLMS

compared to

RED marker: standard digital filter with
trapezoidal shape
(shows evidence of $1/(f)^n$ noise)

Quantization error by FLASH ADCs is reduced by the digital shaper according to the BIT GAIN value.
BIT GAIN = - 0.5 $\log_2$ (sum(x^2))

The effective n.of bits after shaping becomes: e.g. 14 (FLASH ADC) + 2 (BIT GAIN) = 16

Planned activity

- Manufacturing of the prototype board (2 layer PCB)
  (Suitable also for operation @ T=77K)   6 W

- Characterization of PRE+DLD with Rf and Pulsed Reset
                                                            4 W

- Charact. of PRE+DLD with Rf and Pulsed Reset @77K
                                                            4 W

Thank you!