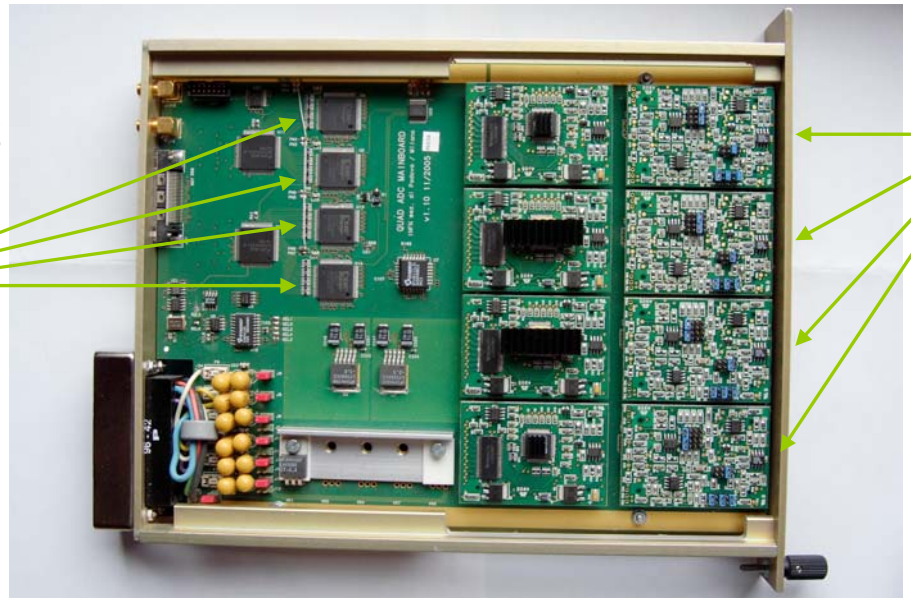
DAQ System for Gerda Phase I

Offset Adjustment

Single Ended or Differential Input

Main Characteristics of DAQ System are:

- 4 Channels per NIM Module
- 14 bit, 100 MSamples/s Free Running ADC per Channel
- Low Noise Front-End Electronics with Adjustable Gain
- Fully Differential Design for Improved Noise Immunity
- Fast transmission link to PCI boards into user PC



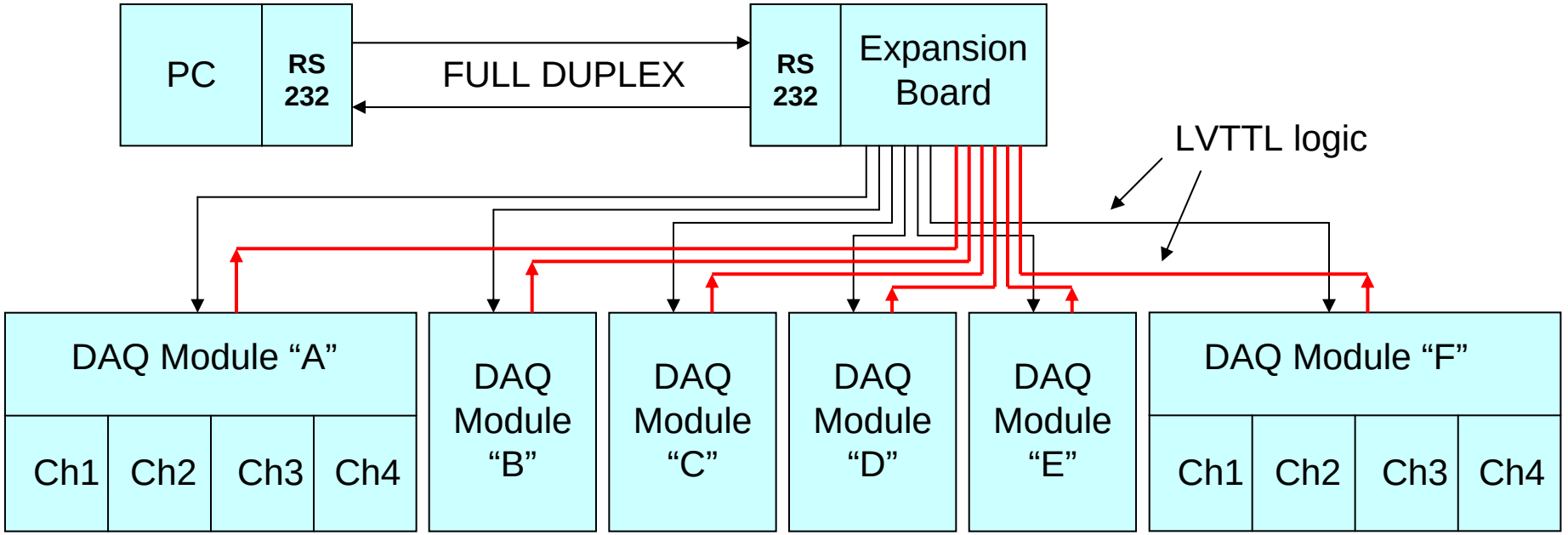
FPGAs

Modular Design

This is the original system but the Gerda experiment required several improvements…

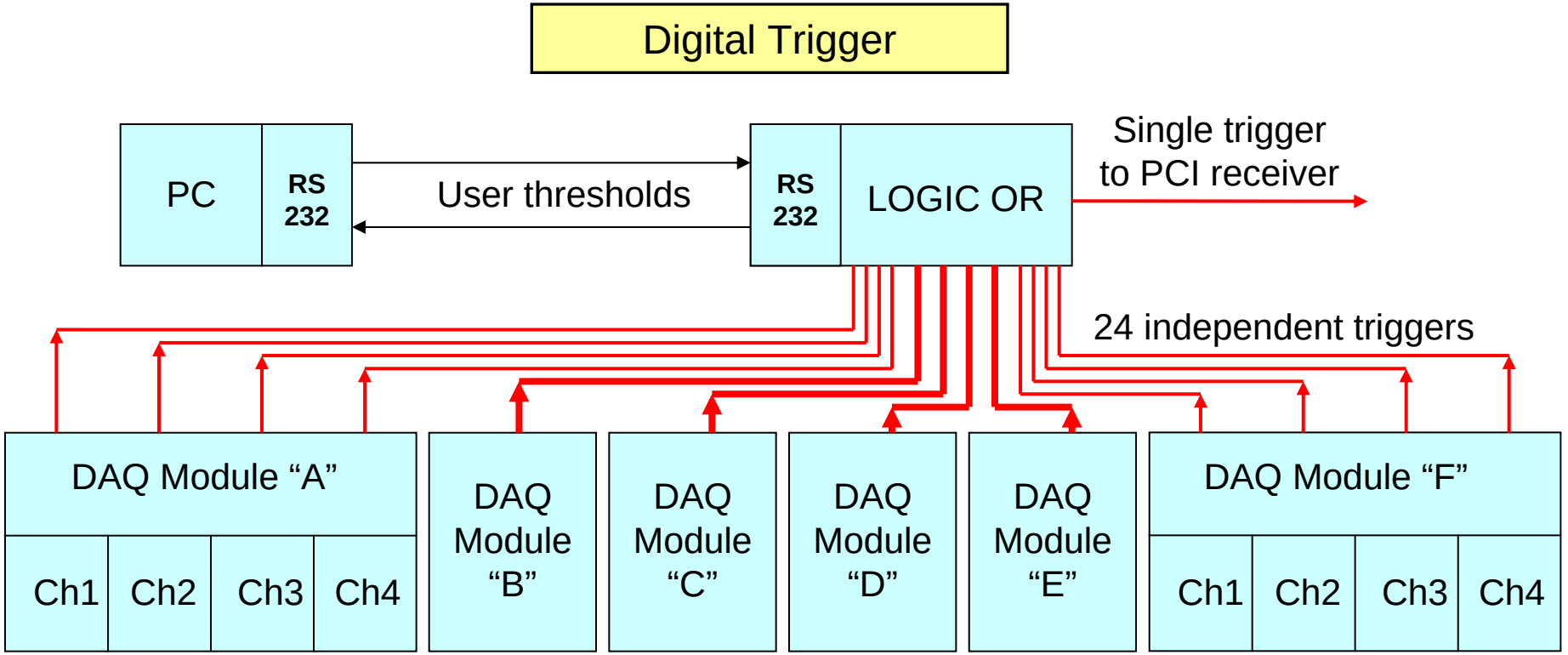
The New Features

Slow control of multiple DAQ modules through a single PC user interface



- RS232 interface implemented in Xilinx Spartan3 FPGA with dedicated VHDL code (38400 bit/s custom and efficient protocol with CRC implementation)
- 16 byte-long user register available for each DAQ channel
- Each one of the DAQ channels is specifically addressable through the expansion board
- Diagnostic of defective channels implemented at expansion board level

The New Features



- Digital trigger has high sensitivity and low time-to-amplitude walk
- Trigger is implemented with resource-saving techniques in FPGA
- Each DAQ channel can have independent trigger thresholds
- The expansion board provides logic OR-ing of all triggers from the DAQ channels

The New Features

Baseline estimation and rate-meter of events

- Baseline level is important to verify the functionality of the front-end electronics and also to get useful information about the amount of leakage current flowing through the detector
- Baseline is estimated independently for each DAQ channel in the associated FPGA
- Baseline is estimated through a dedicated algorithm, trigger-less and adaptive, which provides confident results also with moderate-to-high rate of events (< 10k/s)
- Baseline estimation can be read by the PC user interface through 3 dedicated user registers
- This functionality has been realistically simulated in Matlab but not implemented yet (1 week)

- The rate-meter of events is implemented for all DAQ channels in the expansion board FPGA
- The main purpose to calculate and collect this information is to get useful diagnostic insight about the functionality of the whole system (detector, high voltage, front-end electronics, DAQ system, radioactive source used for calibration, etc.)
- This functionality has not been implemented yet (1 week)