TG3: Analog Electronics for Ge detectors

Goal of Task Group: Delivery of

- Front-end (FE) circuts for Ge det. read-out
- Cables from FE to FADC
- HV-PS, LV-PS, Pulser
- Slow-control of operational parameters of digital and analog electronics.

Status of TG3 works: FE not ASIC cryogenic circuits

	Status / meet specs	Date	Notes
Test of FE Circuit 1 (AGATA, discrete components)	**Achieved**	09/05	Discrete components. Warm outside LN bath with cold FET
Test of FE Circuit 2 (IPA4 – monolithic JFET+ polarizing components)	**Achieved**	02/2005	Semi-integrated. Polarizing components, CF,RF not integrated.
Production of 20 FE channels for Ge prototypes at LNGS and MU	**Achieved**	05/2006	
Test of produced channels	**To be done**	07/2006	
Test of FE circuit 3 (AMPTEK- A250)	√	12/2005	Ibrid can work at cryo-T.

Status of TG3 works: ASIC FE cryogenic circuits

MI- ASIC – CMOS FE			Integrated but not CF,RF
Test	**Achieved**	06/2005	
Test of chips	**Achieved**	12/2005	
2nd run (fine tuning)	**To be done**	10/2006	
Production	**To be done**	2007	
MI- ASIC – CMOS FE			Fully Integrated but not RF, with possible active reset
Test run	**Submitted**	07/2006	
Test of chips	**TBA**	09/2006	
2nd run (tuning)	**TBA**	10/2006	
Packaging	**Candidate**	04/2006	
Hd ASIC-CMOS			Fully integrated
Test run	**Done**	02/2006	
Test of chips	**TBA**	?	
2nd run	**TBA**	?	
Production	**TBA**	2007	

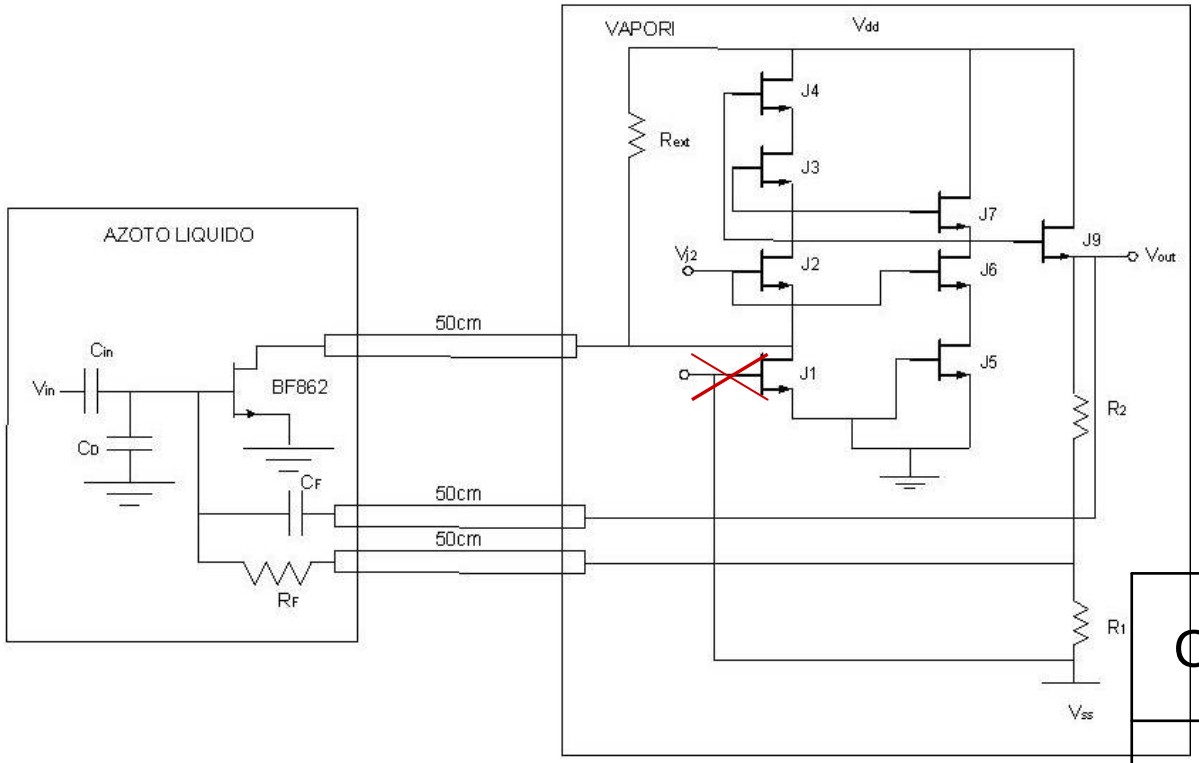
Status of TG3 works : Cables (Phase I) and LV,HV PS

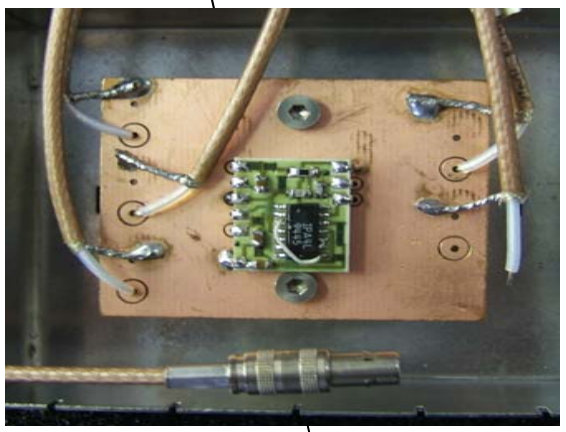
	Status / meet specs	Date	Notes
HV for Ge detector Caburn Kapton 8 kV 0,25 mm diam	**Achieved**	06/05	Measured by M.Laubenstein < 10 mBq/kg both for U and Th. (30 g/ 6 m)
Signal (from FE to FADC) and LV PS (picocoax-Axon) (siltem coax) (Tekdata woven)	**X Ongoing, candidates exists**	12/2005 05/2006	To be measured γ-spectrometry
LV PS	**Candidate**	07/2006	INFN-PD design and production
HV PS	**Candidate**		
Pulser	**X**	12/2006	

Possible problems

Too high radioactivity of components, as the junction box has to be put nearest the top of the crystal string compared to the showed solution (see talk of B.Majorovits)

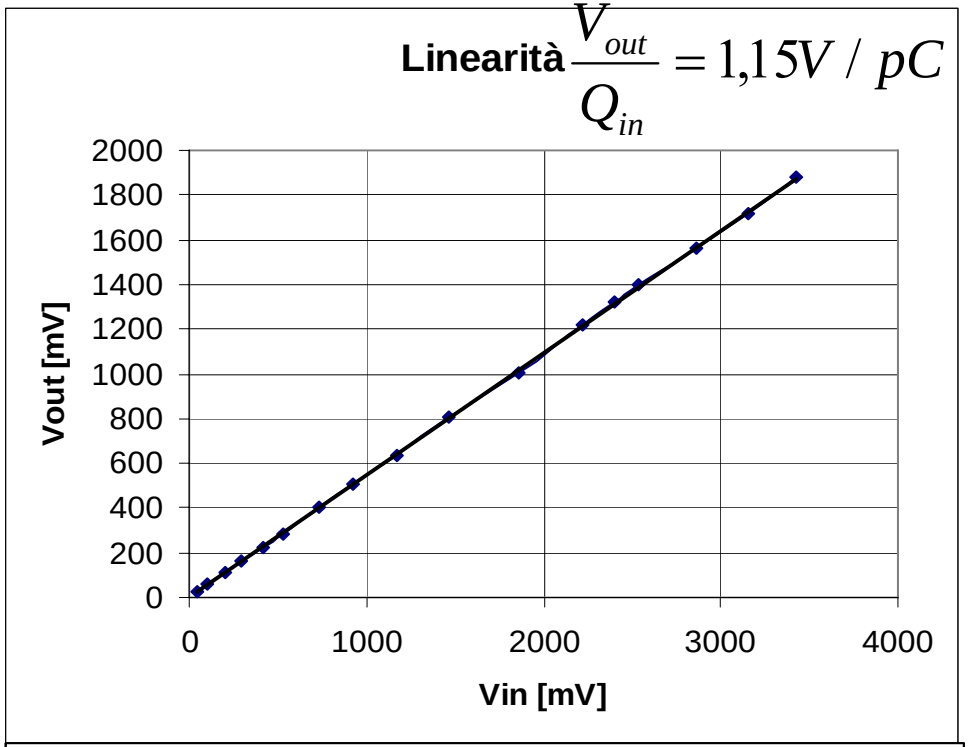
IPA4+external FET BF862: Why?

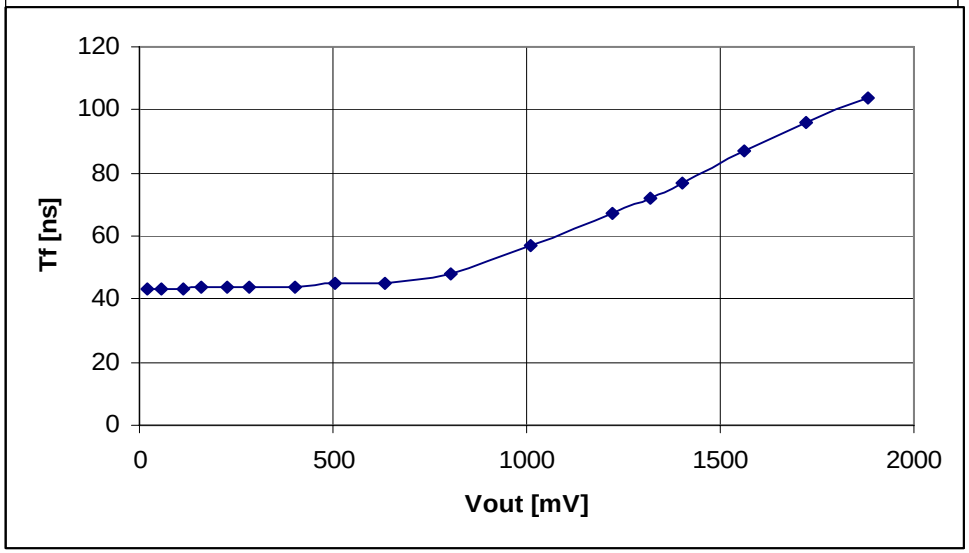


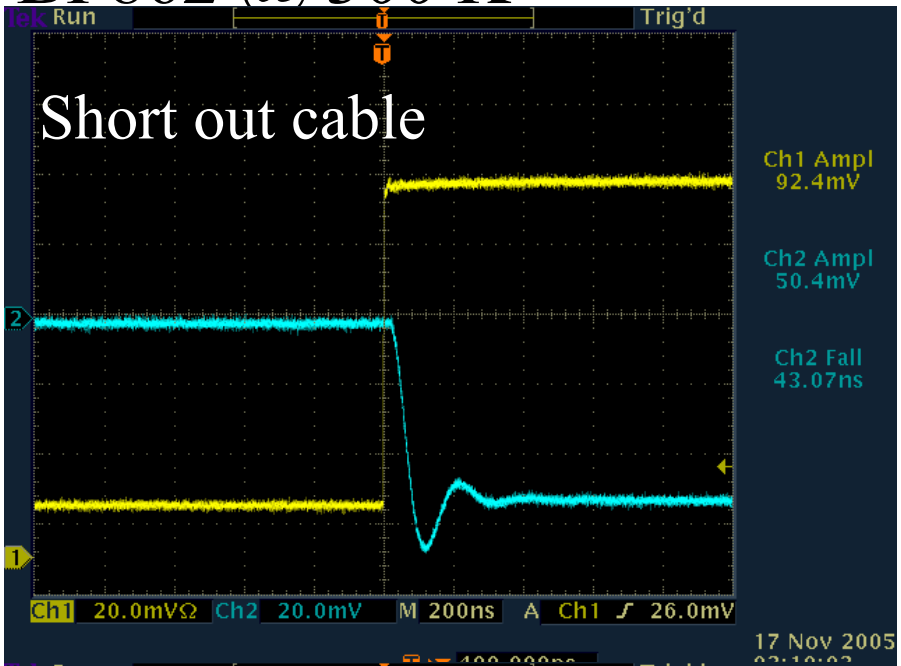


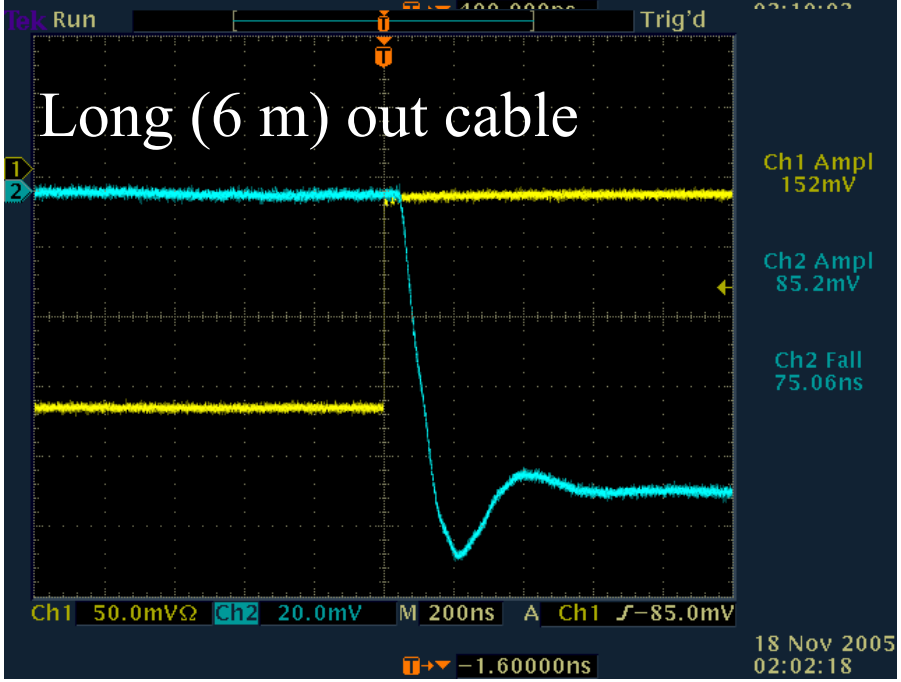
CD [pF]	τf [ns] (BF862)	τf [ns] (J1)
0	27	110
15	36	140
27	44	155

IPA4+external FET BF862 @ 300 K

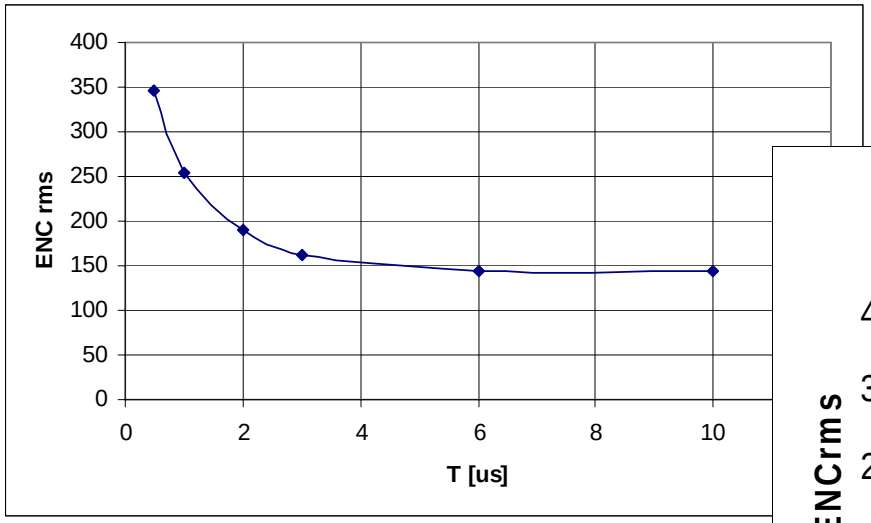




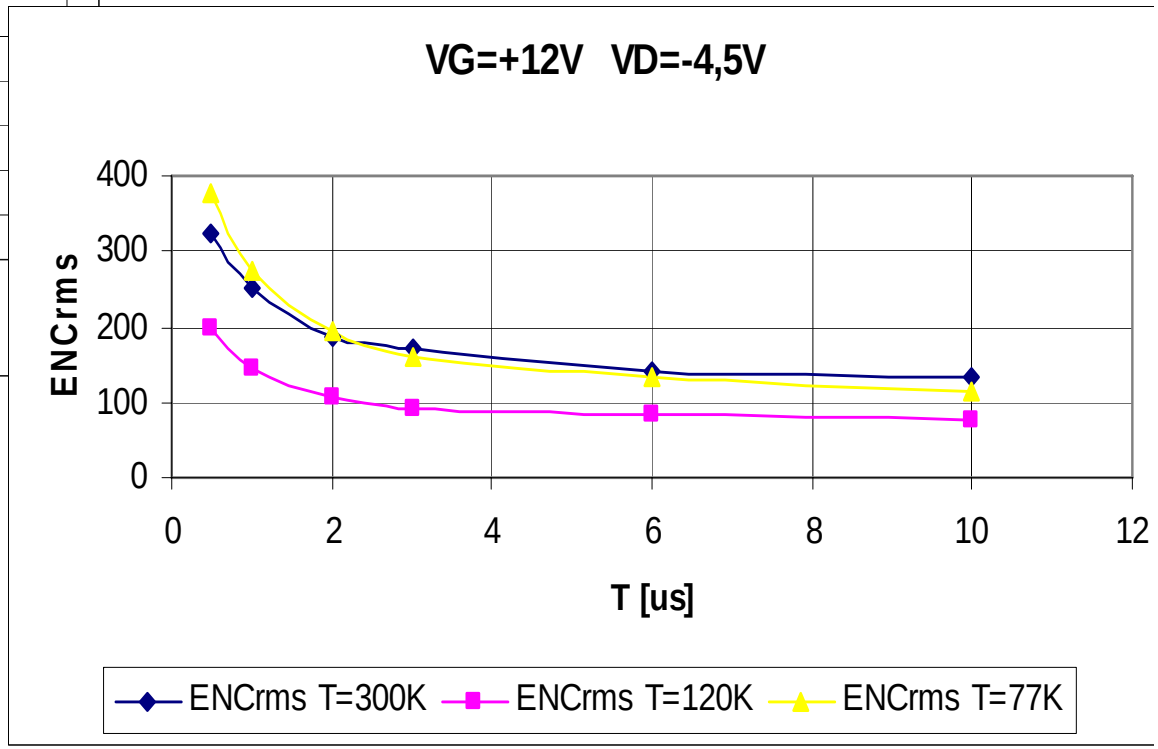




IPA4+BF862$_{ext}$ @ LN

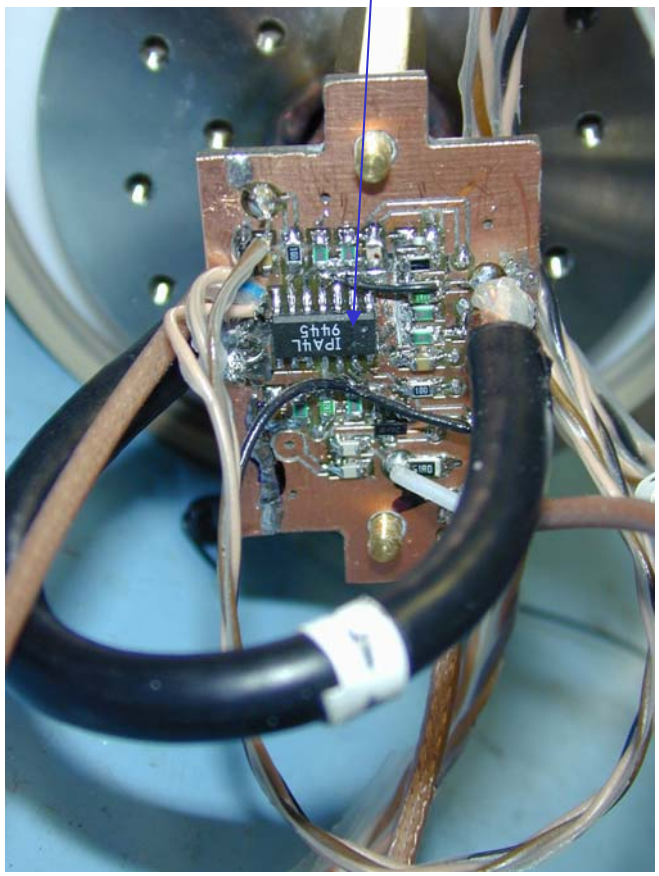


IPA4+J1$_{int}$

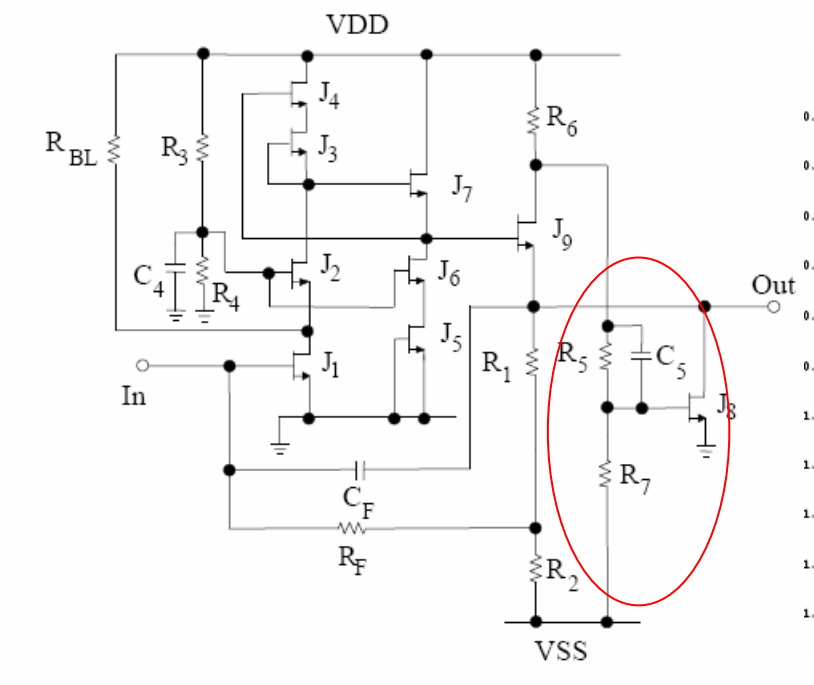


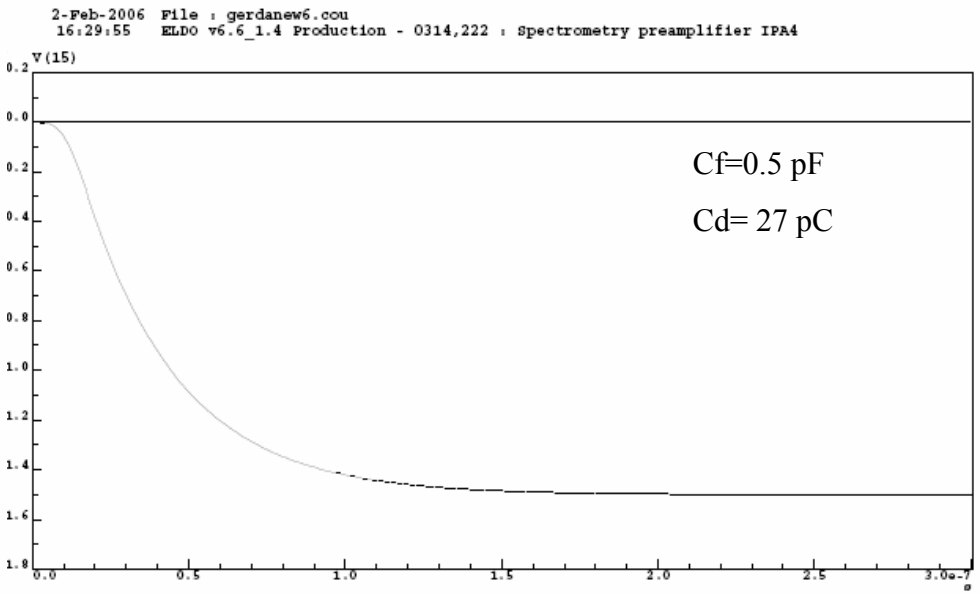
IPA4 + $J1_{ext}$ + 100 Ω Out stage: the new test board

New setup for LN measurements



IPA4 + $J1_{ext}$ + 100 Out stage: simulated pulse 50 ns fall time (@ 300 K).

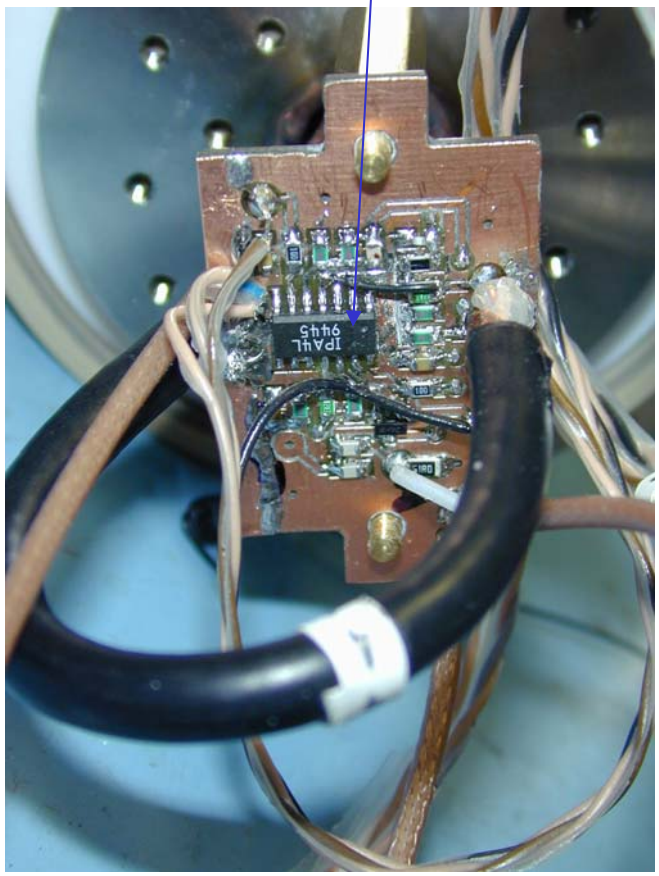




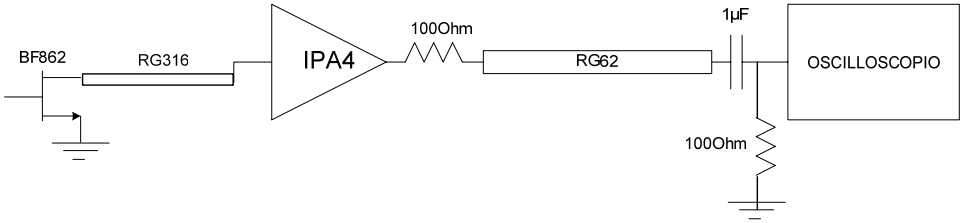
Swing to -1.5 V

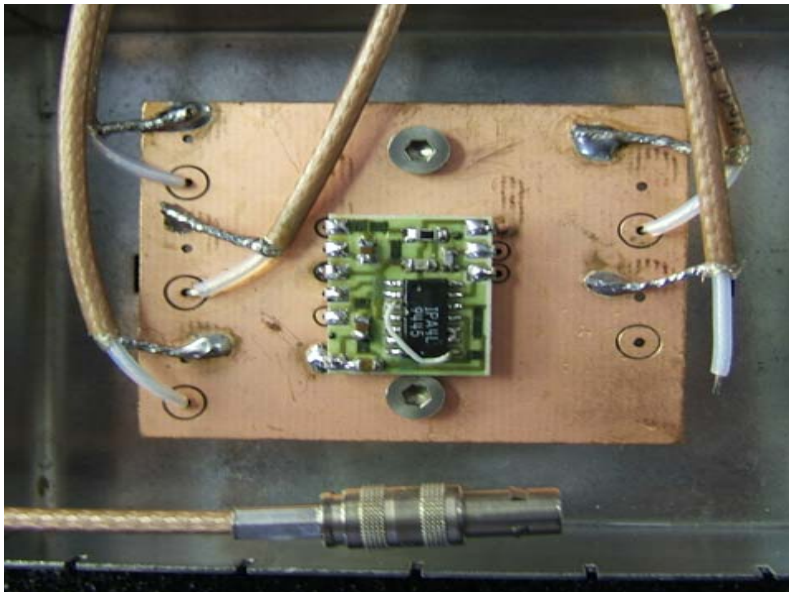
IPA4 + $J1_{ext}$ + 100 Ω Out stage: the new test board

New setup for LN measurements



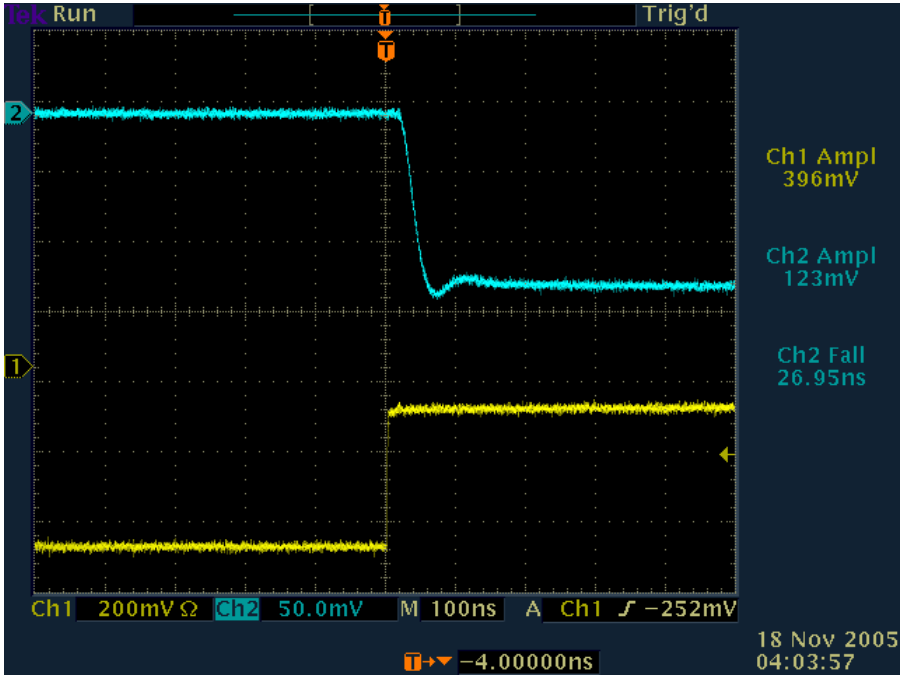
Back to 1 kΩ out stage, better pulse shape





Measured pulse fall time for IPA4 preamp. Operated with integrated J1 or external BF862, at T =LN.

CD [pF]	τf [ns] (BF862)	τf [ns] (J1)
0	27	110
15	36	140
27	44	155



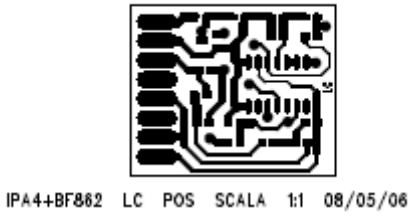
Production of 20 FE cryogenics circuits (based on IPA4 JFET monolithic circuit) for MU 18 fold segmented prototype, and for LNGS Phase I detector tests

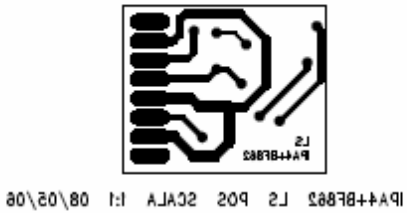
Production of PCB: 23 june at AREL, without 100 Ω output stage: Lowest dissipation and not perfect shape

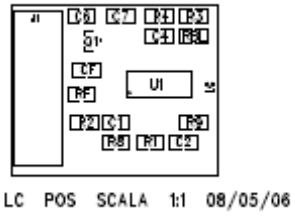
Mounting of components: this week (end 30 june provided I send components).

For LNGS test: 2-3 channels

For MU 18-fold crystal: test and mount circuits on mother board to host 20 preamps and signal-in signal-out. Ready to work end-july.







S. Riboldi, A. Pullia, F. Zocca, C. Cattadori

Charge Preamplifier and Fully Differential Line Driver Integrated in AMS CMOS 0.8um CXZ Tech. for the GERDA Experiment

Milan University and I.N.F.N.

Input transistor

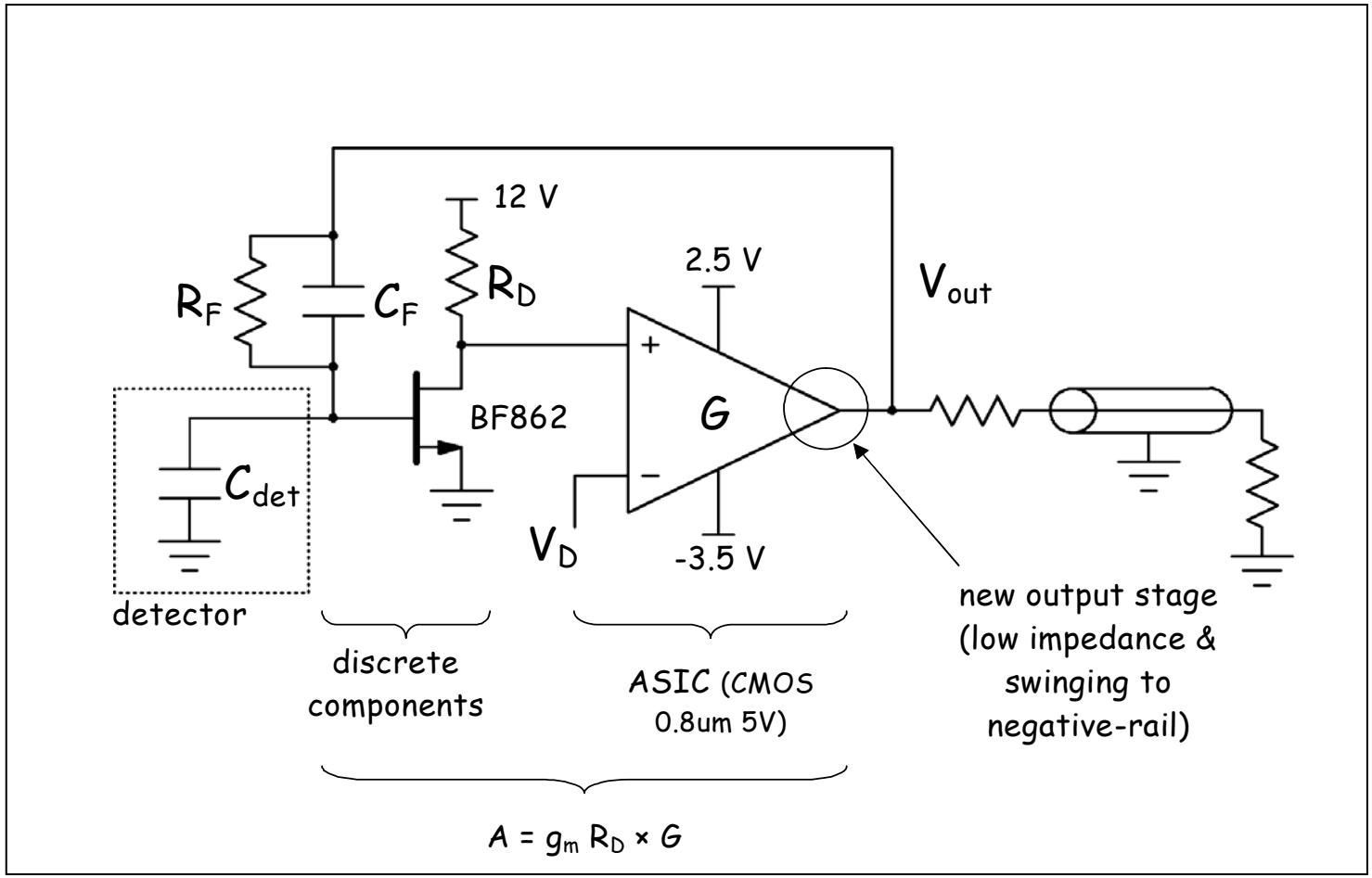
External (JFET e.g. BF862)

- Noise is adequate
- Bandwidth is adequate
- Transistor can be replaced
- Can work at V_{GS} = 0 V which helps zeroing the output offset
- Power consumption is high

Integrated (p-MOSFET)

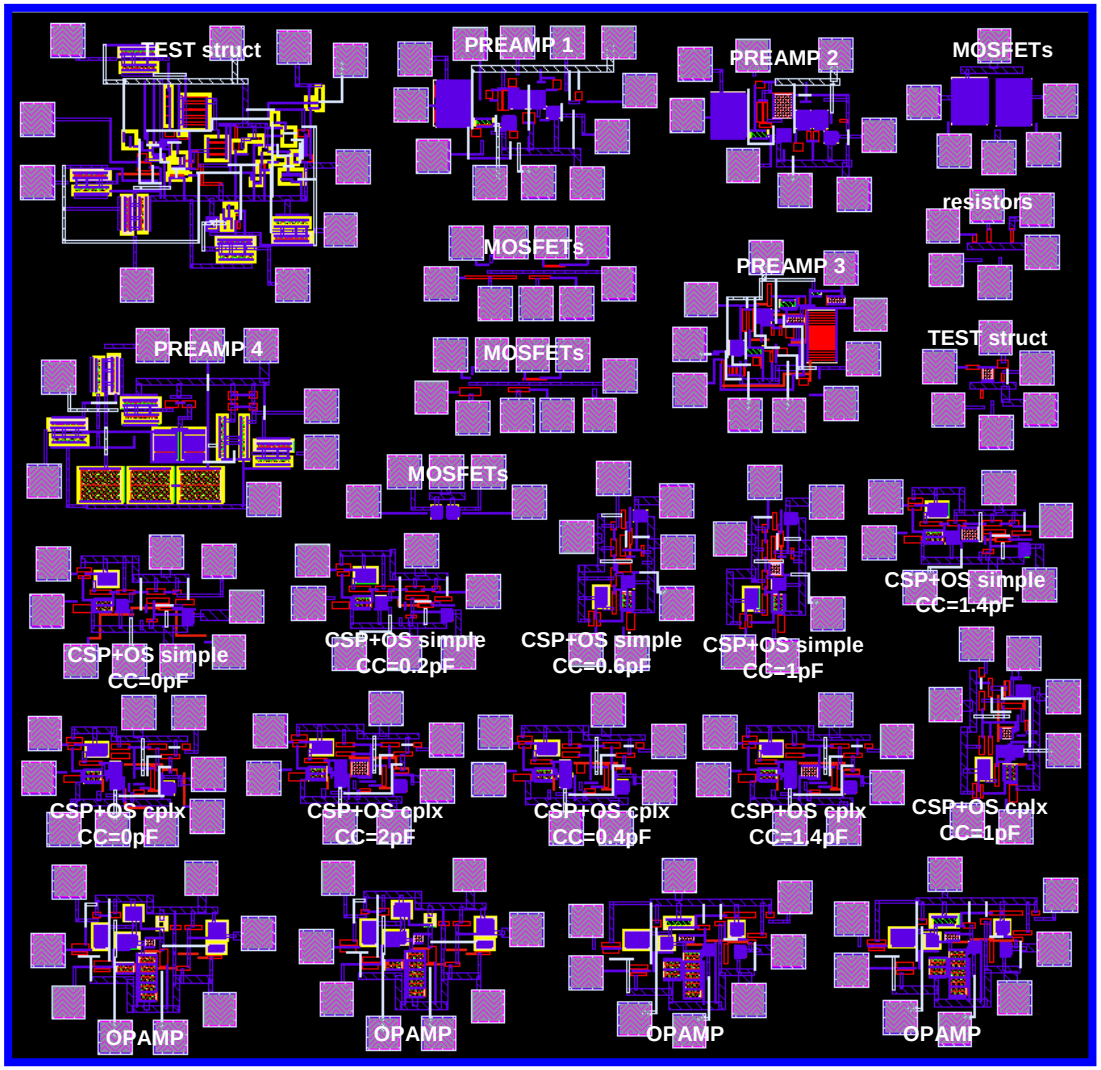
- Noise could be adequate
- Bandwidth is adequate
- Transistor cannot be replaced
- Transistor cannot work at V_{GS} = 0 V
- Power consumption of p-MOSFET could be lower

Proposed circuit structure (from J. Gal*)



*J. Gal et al. "Realization of charge sensitive preamplifiers using current feedback operational amplifier", Nucl. Instrum. And Meth., Vol. A366, pp. 145-147, 1995

Test chip



PREAMP 1
pMOS + ext R_F + ext bias
Vmax = 550mV (50 Ohm)

PREAMP 2
pMOS + ext R_F + int bias
Vmax = 550mV (50 Ohm)

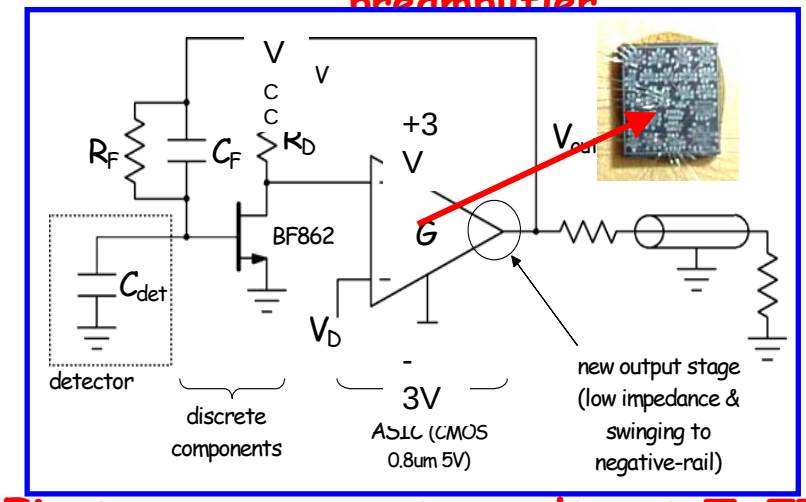
PREAMP 3
pMOS + reset pMOS + shaper

PREAMP 4
pMOS + ext R_F + ext bias
Vmax = 2V (1 kOhm)
HIGH VOLTAGE comp's

CSP + OS simple
CSP with new rail-to-rail output stage. Various comp cap's

CSP + OS cplx
CSP with new rail-to-rail output stage. Various comp cap's

Tested circuit structure: external BF862 JFET + 0.8μm 5V CMOS single-ended preamplifier



First measurement results at T=77°K

(C_F = 0.15pF, R_F= 1GΩ, C_{det} = 15pF)

Negative output voltage swing: ~ 2.4 V

Energy sensitivity (C_F = 0.15 pF) : ~ 185 mV/MeV after 50 Ω termination

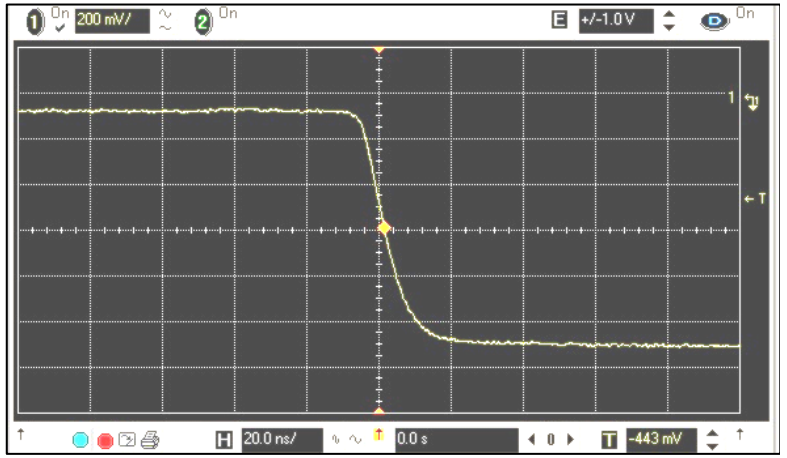
Input dynamic range: ~ 6.5 MeV

Rise time: ~ 15 ns driving 10m cable

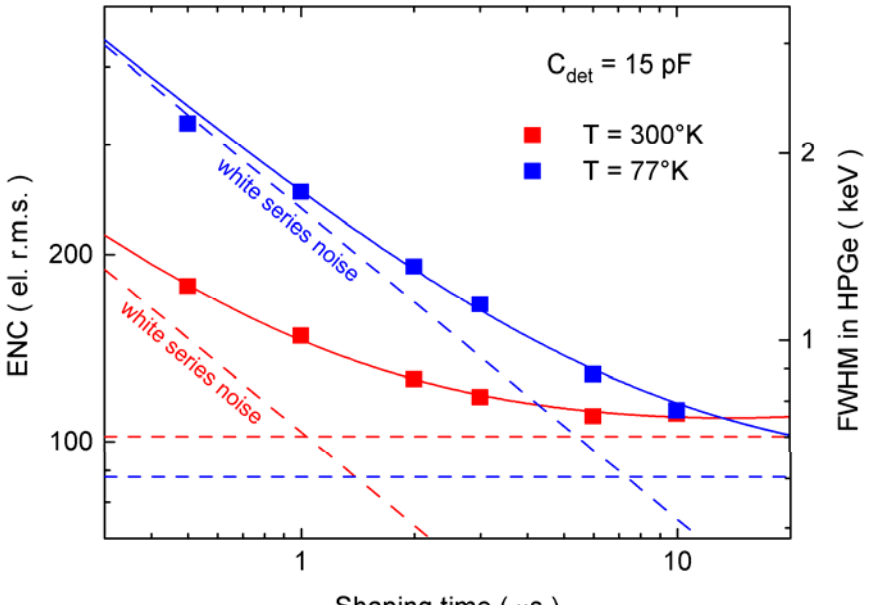
Minimum ENC (C_{det}= 15pF) : 112 e^- at τ_{shap}=10μs

Total power consumption: ~ 25 mW

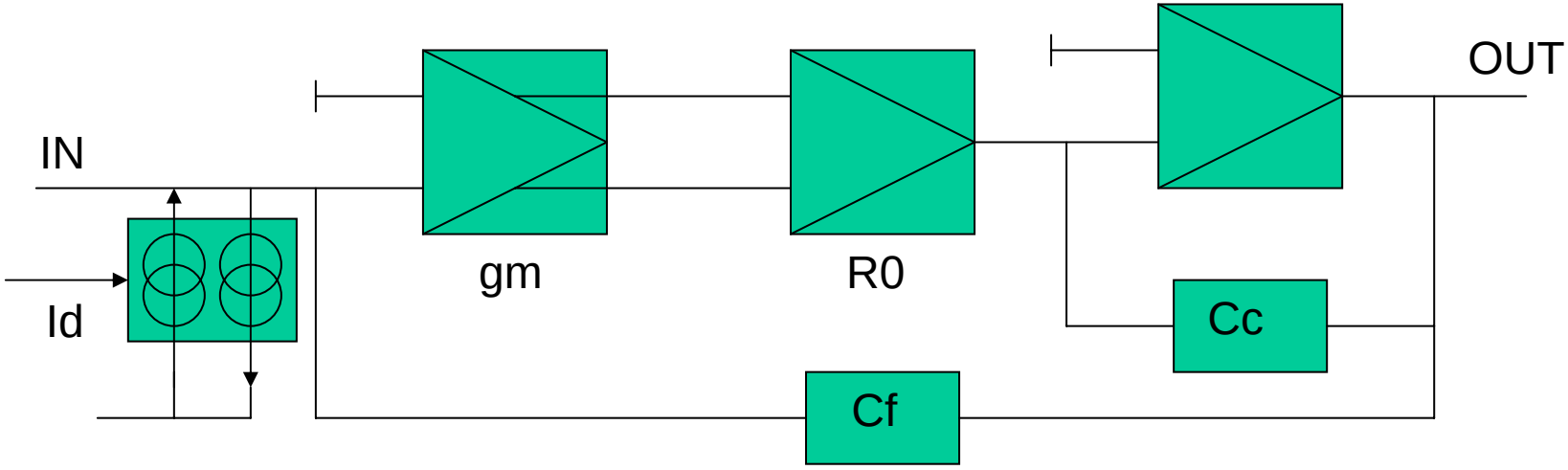
Acquired output signal driving a 50 Ω coaxial cable of ~ 10 m : rise time of ~ 15 ns



Comparison between noise measured at room temperature (T=300°K) and in LN (T=77°K)

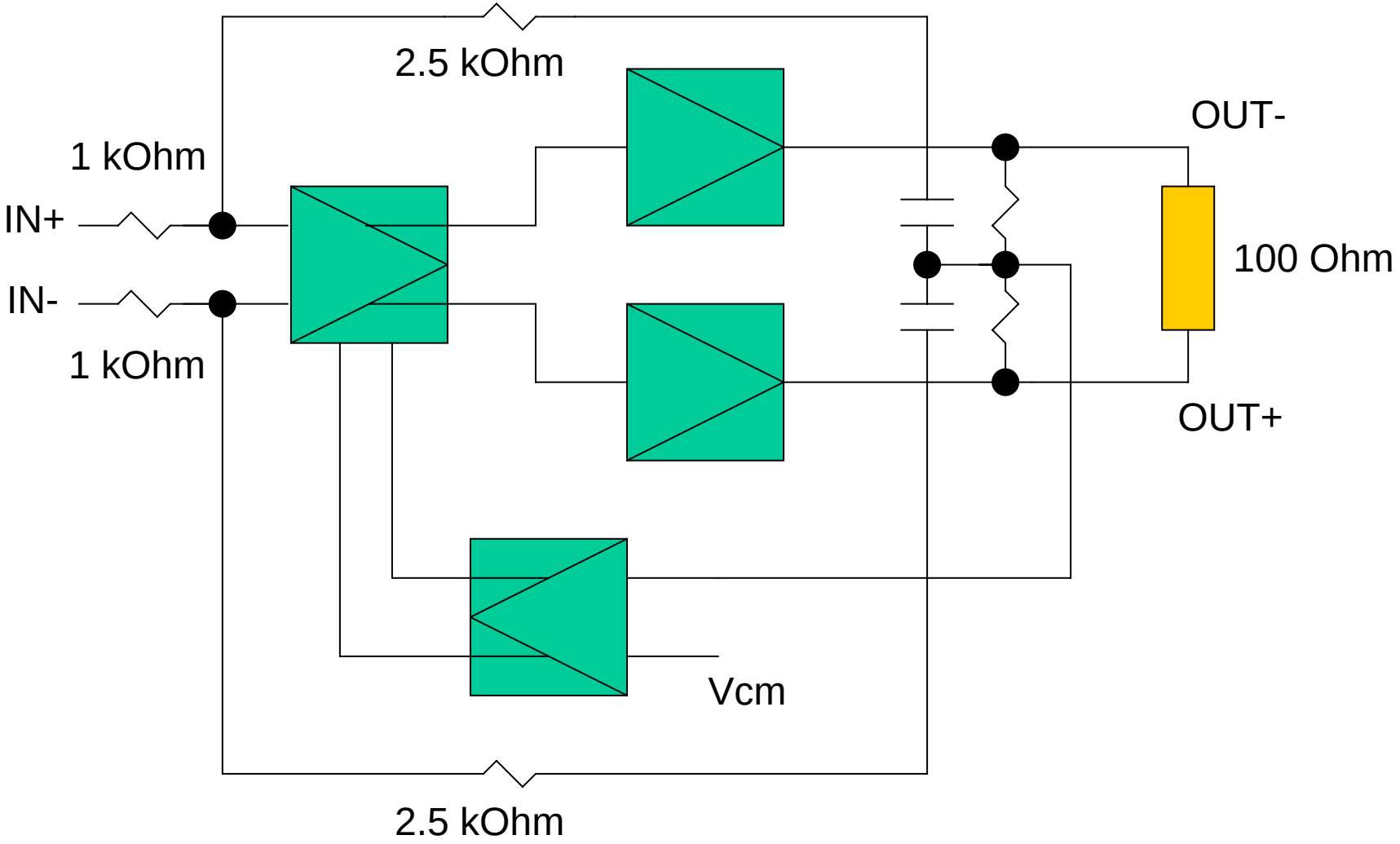


Integrated Preamplifier



- Tunable system (variable gm and R0 by a factor of 10)
- Noise, bandwidth according to specifications
- Dual Power Supply (+2.5v / -2.5v) / No additional Vrefs required
- Fully Bipolar Output Swing (+1.6v / -1.6v) @ Rload = 1 Kohm
- Non linearity < 1/1000 @ (-1.6v < Output Swing < +1.6v)
- Can operate with continuous reset (external R) or pulsed reset (bipolar Id)

Fully Differential Line Driver



Fully Differential Line Driver

- Dual Power Supply (+2.5v/-2.5v)
- No additional Vrefs required
- Fully Differential Signal Path inside the OpAmp
- Fully Bipolar Output Swing (+2v/-2v) @ Rload = 100 Ohm
- Large Differential Output Swing (8v) @ Rload = 100 Ohm
- Bandwidth according to specifications
- Tunable system
- Variable Power Consumption:
  (from 3 mA @ Low Power up to 6 mA @ Full Bandwidth)

Low Voltage Low Noise PS designed at PD –INFN workshop
V=+12 V, V=+5 V, V=-5 V, I = 0.7 A each)

If test OK then can be adopted for GERDA