TG3: progress report on front-end electronics

C. Cattadori on behalf of A.Pullia, F.Zocca, S.Del Re, B. Schwingenheuer……

Choice of FET and preamps

Strategy for Phase I is to pursue three solutions:

1. cold FET and $R_f C_f$ and warm hybrid preamps outside the LN bath in the proximity of the manifold (PCB board preferable or just outside manifold).
   pro: now ready solution.
   cons: problems from long cables (~ 5- 6 m) → stabilization of amplifying stage, reduced bandwith due to ad-hoc compensating capacitance inside preamps, noise slightly increase, noise pick up (serious), increased possibility of cross talk between channels, microfonic noise etc.

Choise of FET and preamps

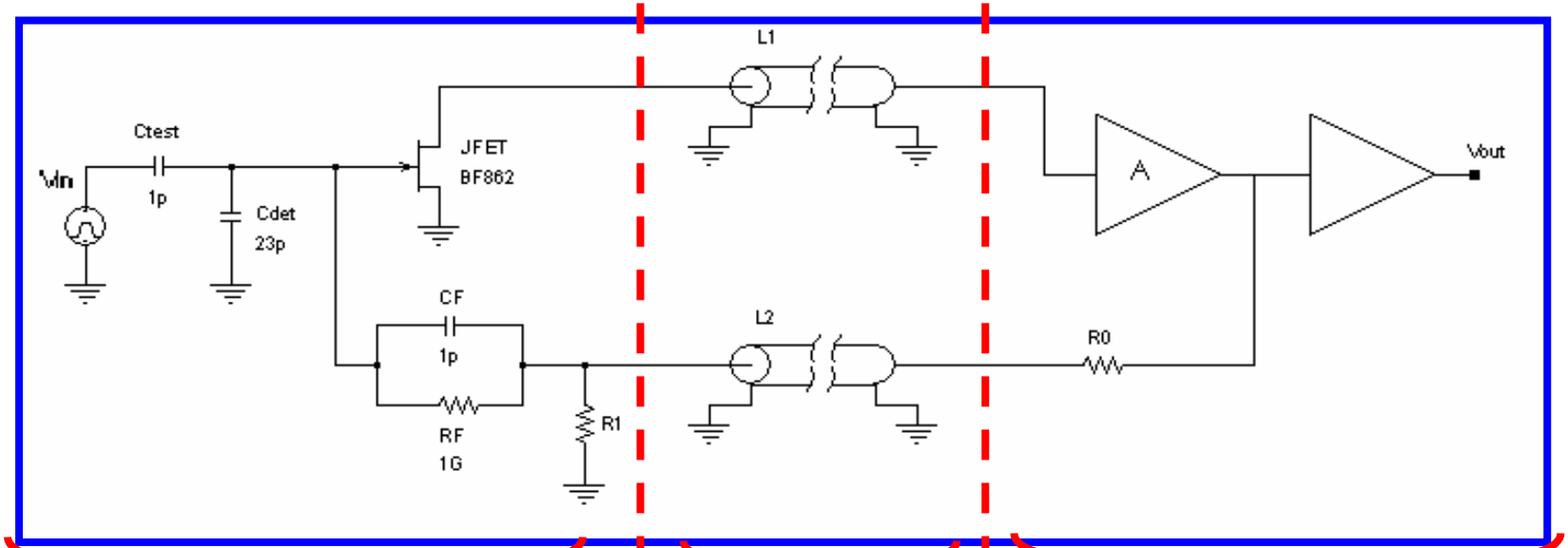
- 2 possible FET
  - InterFET IF1331 — tested in HD and MI
  - Philips BF862 — tested in MI

- 2 Hybrid preamp
  - EURYSIS preamp PSC823C
  - MARS preamp developed by INFN Milano

Experimental Set-up (Sol.1)

(Experimental results obtained in Milano by A.Pullia, F. Zocca, C. Cattadori)

measurements performed { at the test bench
at room temperature (300°K)



- Philips BF862 JFET
- C_F = 1pF , R_F = 1GΩ
- C_{det} = 23pF , C_{test} = 1pF
- R1 (& R0) = termination resistances

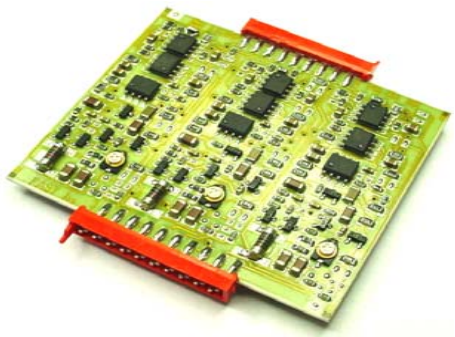
Coaxial cables :

RG62 (93 Ω)

or

RG58 (50Ω)

AGATA preamplifier mod. PB-B1



Agata Analog electronics performances

TABLE II
PREAMPLIFIER'S PERFORMANCE

Performance	BF862	BF861B
Integral nonlinearity	±0.04 %	±0.04 %
Energy sensitivity	150 mV/MeV	150mV/MeV
Rise time	4ns	4ns
Decay time	250 μs	250 μs
Power requirements	±12 V	±12 V
Power consumption (single ended)	220 mW	175 mW
Typical noise at 0 pF (3μs shaping time)	0.750 keV FWHM	0.800 keV FWHM
Slope (20 to 60 pF range)	8.5 eV/pF	15 eV/pF
Board dimensions	18x38 mm²	18x38 mm²

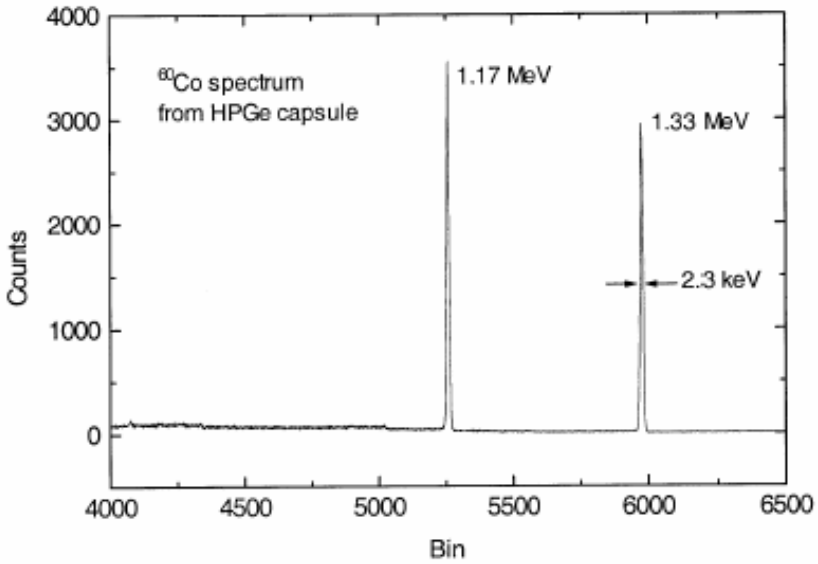


Fig. 7. ^{60}Co spectrum obtained with a cryogenic HPGe capsule biased at 2.5 kV. The temperature of the FET and the feedback resistor is 120 K.

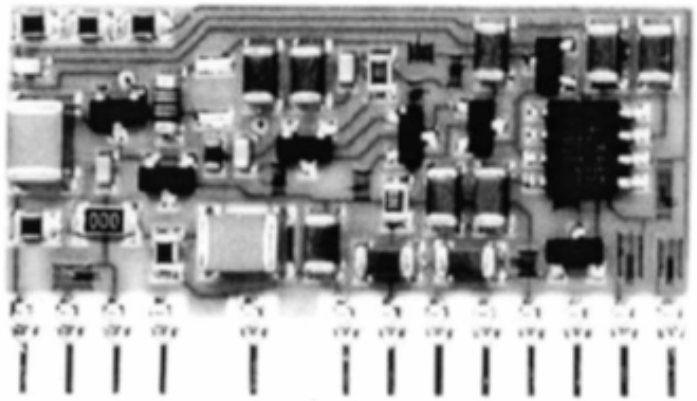


Fig. 8. Photograph of the hybrid preamplifier PA3.1.

on the spectral line at 1.33 MeV. This is to be compared with 2.4-keV FWHM obtained with the charge sensitive preamplifier PSC 821 by Eurisys. These measurements have been performed biasing the HPGe detector at 2.5 kV. A photograph of the realized hybrid is shown in Fig. 8.

V. CONCLUSION

A hybrid charge amplifier using a new low-noise continuous-reset mechanism has been realized and tested with an HPGe detector. A functional characterization of the prototype has been carried out which proves the effectiveness of the design philosophy. An excellent spectroscopic resolution as well as fast rise times have been obtained.

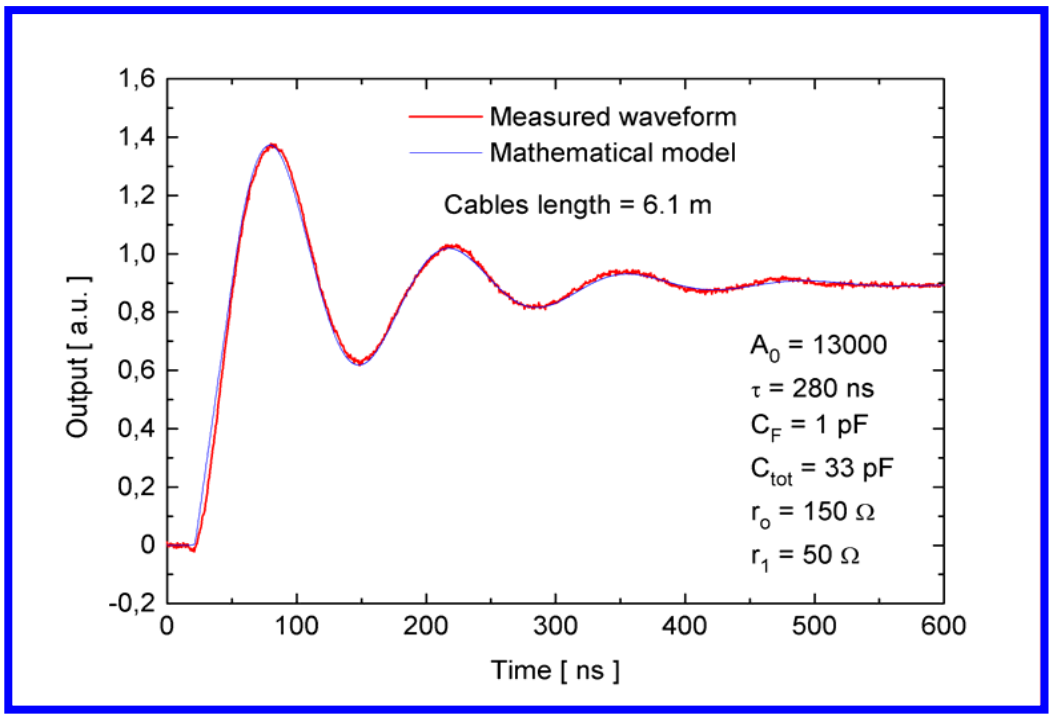
ACKNOWLEDGMENT

The authors would like to thank M. Pignanelli, A. Bracco,

Oscillating response

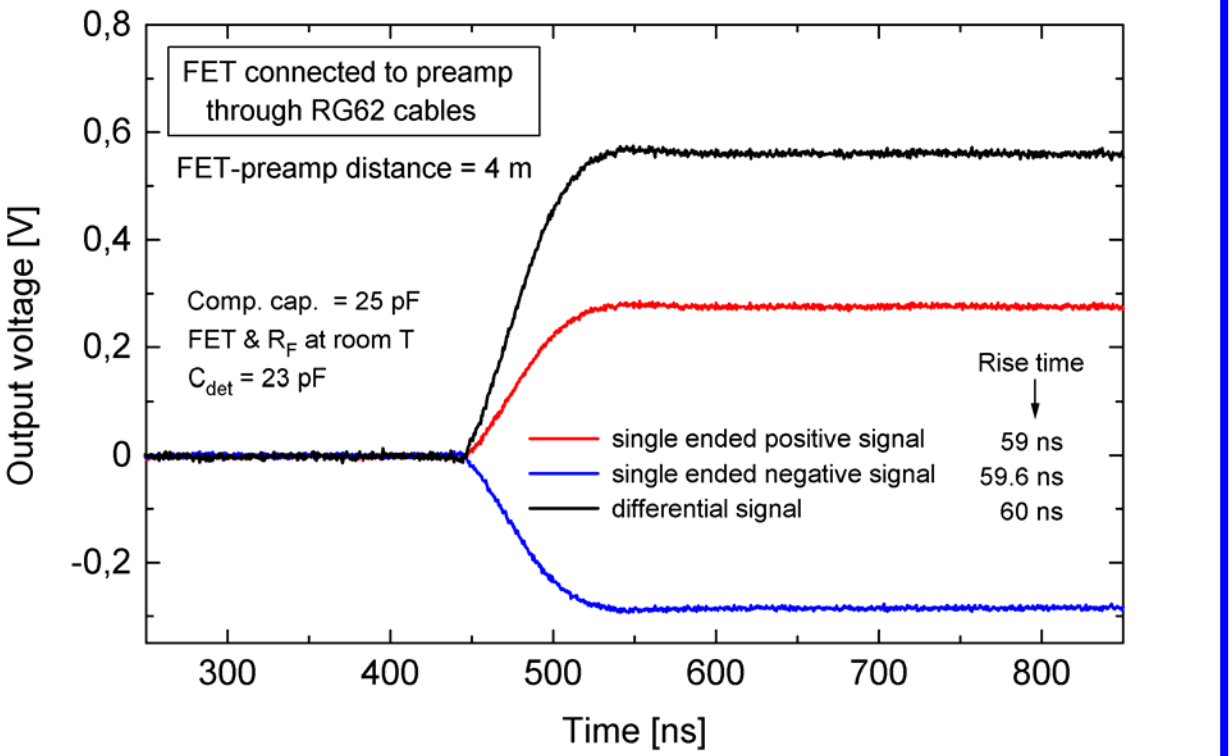
NO compensation capacitance

JFET-preamp distance: ~ 3m ➡ total length of the delay lines: ~ 6m



Comparison between the waveform observed at the circuit output and the mathematical model based only on the time delay introduced in the feedback loop

RG62 cables (93 ohm impedance): stabilized output response



Single cable length (FET-preamp distance): ~ 4m

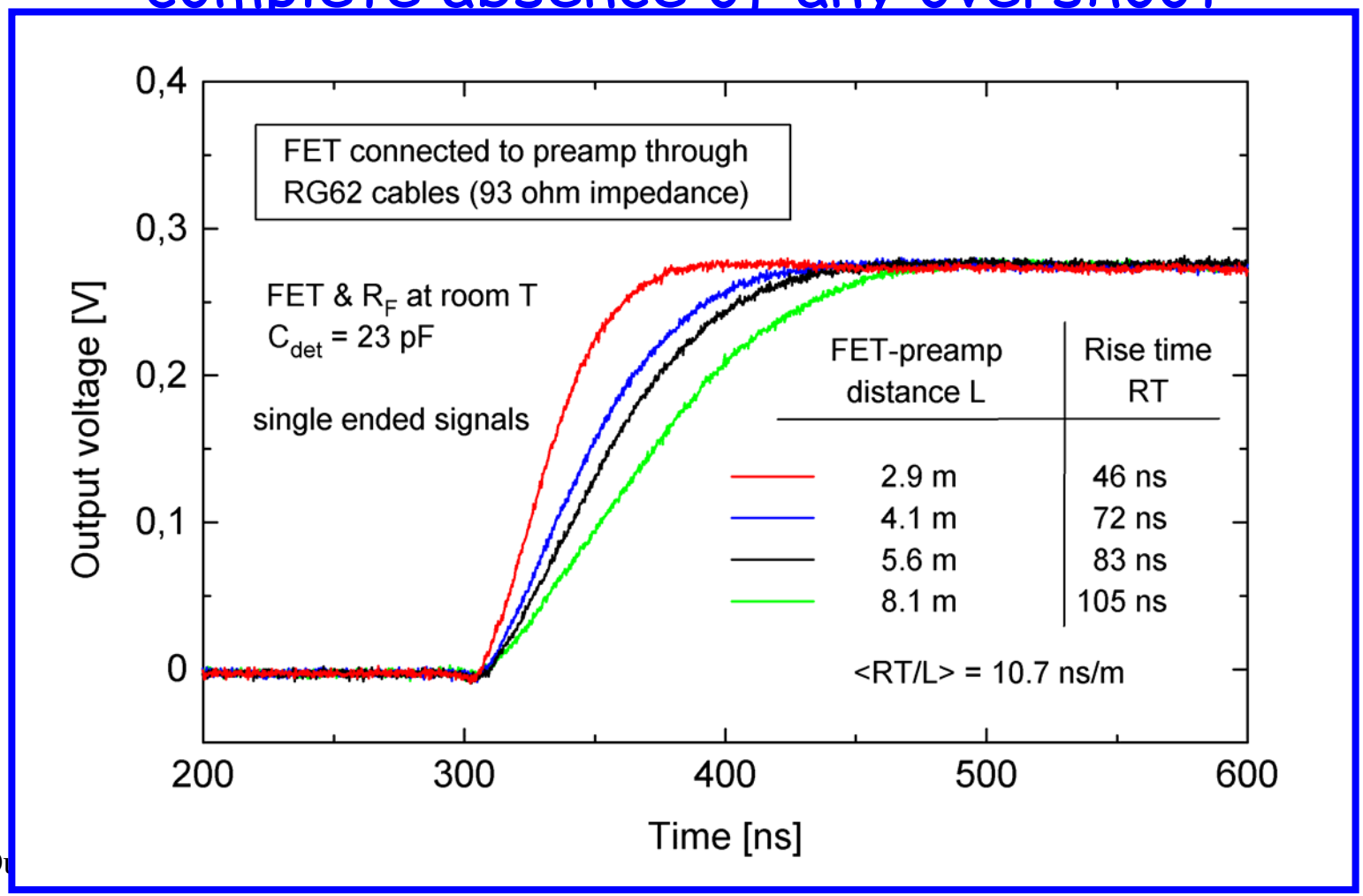
A compensation capacitance of 25pF allows to stabilize the output signals, but we have to accept a little overshoot (~1%).

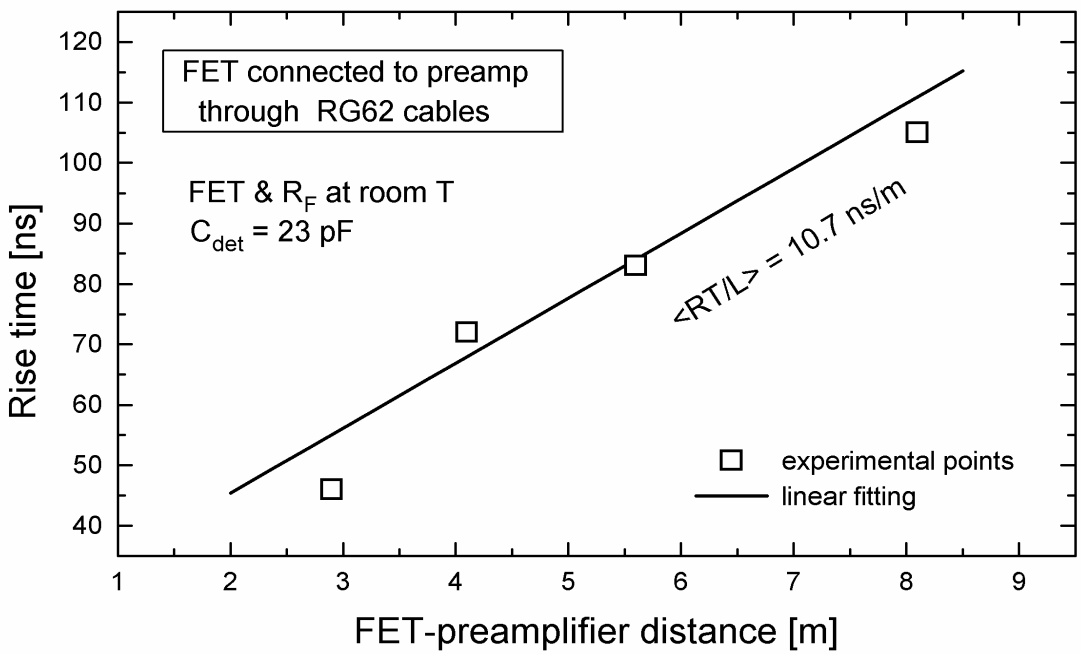
The rise-time obtained is of ~ 60ns

If we want to COMPLETELY eliminate any overshoot, we have to reduce the bandwidth and accept a LONGER rise time.

RG62 cables (93 ohm):

Rise Time vs. FET-preamp distance in complete absence of any overshoot



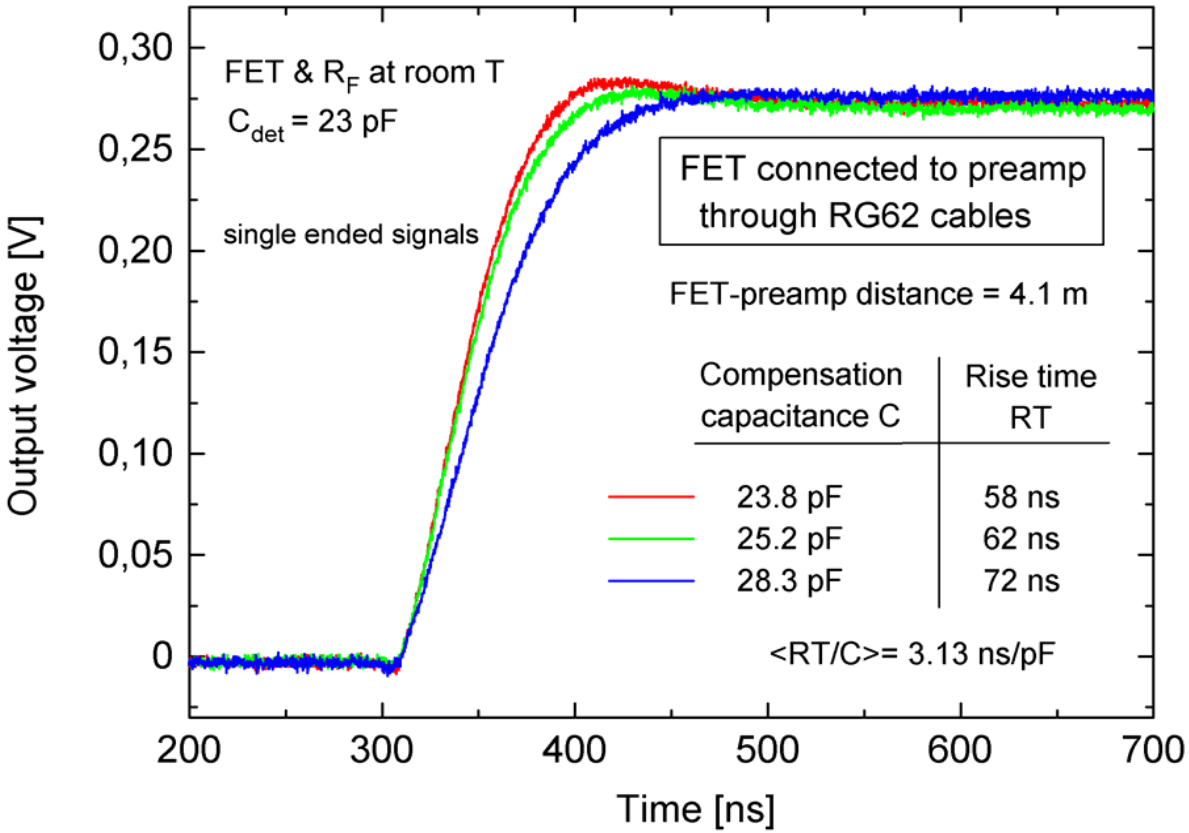


RG62 cables (93 ohm)

Extrapolated results:

FET-preamp distance	Rise time with no overshoot
≈ 3m	≈ 55ns
≈ 4m	≈ 65ns
≈ 5m	≈ 75ns
≈ 6m	≈ 85ns

RG62 cables (93 ohm): effect of the compensation capacitance for a fixed FET-preamp distance

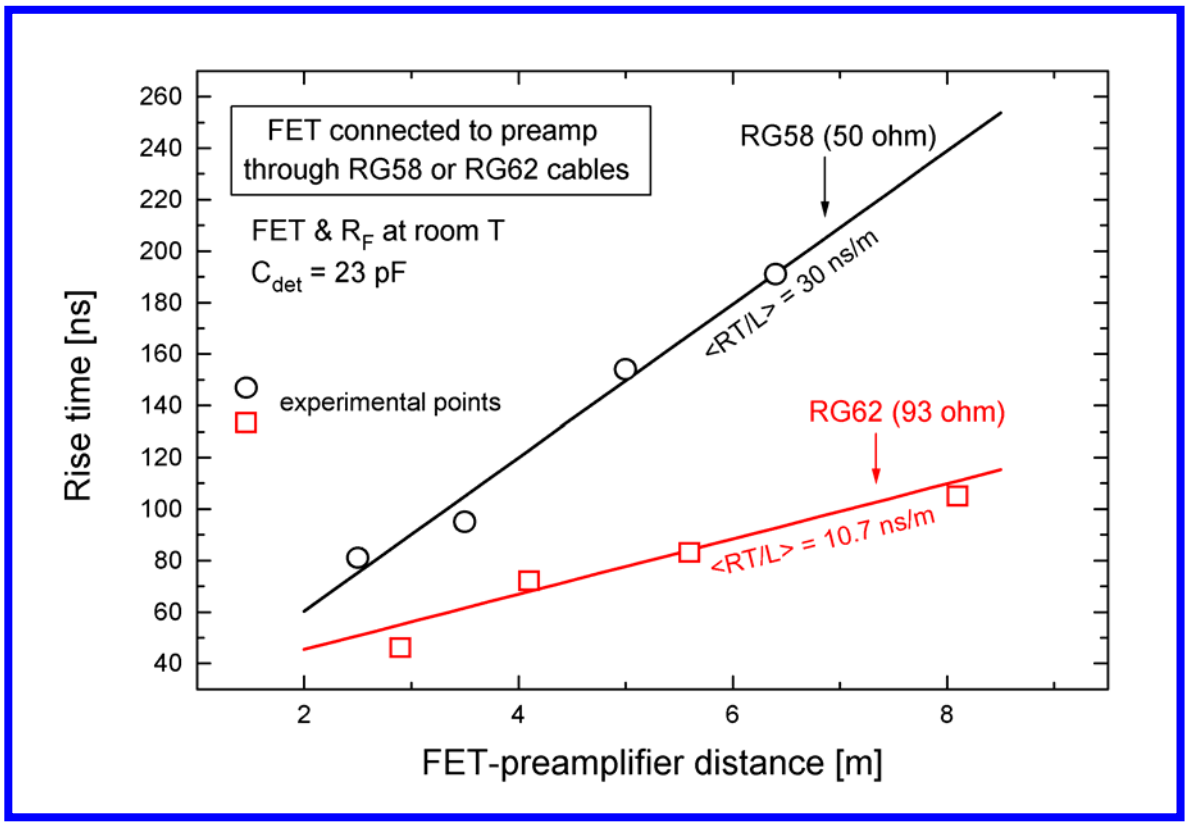


By decreasing the compensation capacitance, the rise time gets improved with a slope of ≈ 3ns/pF

BUT we have to accept some overshoot !

RG58 cables (50 ohm impedance): comparison with RG62

Rise time values vs. different FET-preamp distances in complete absence of any overshoot



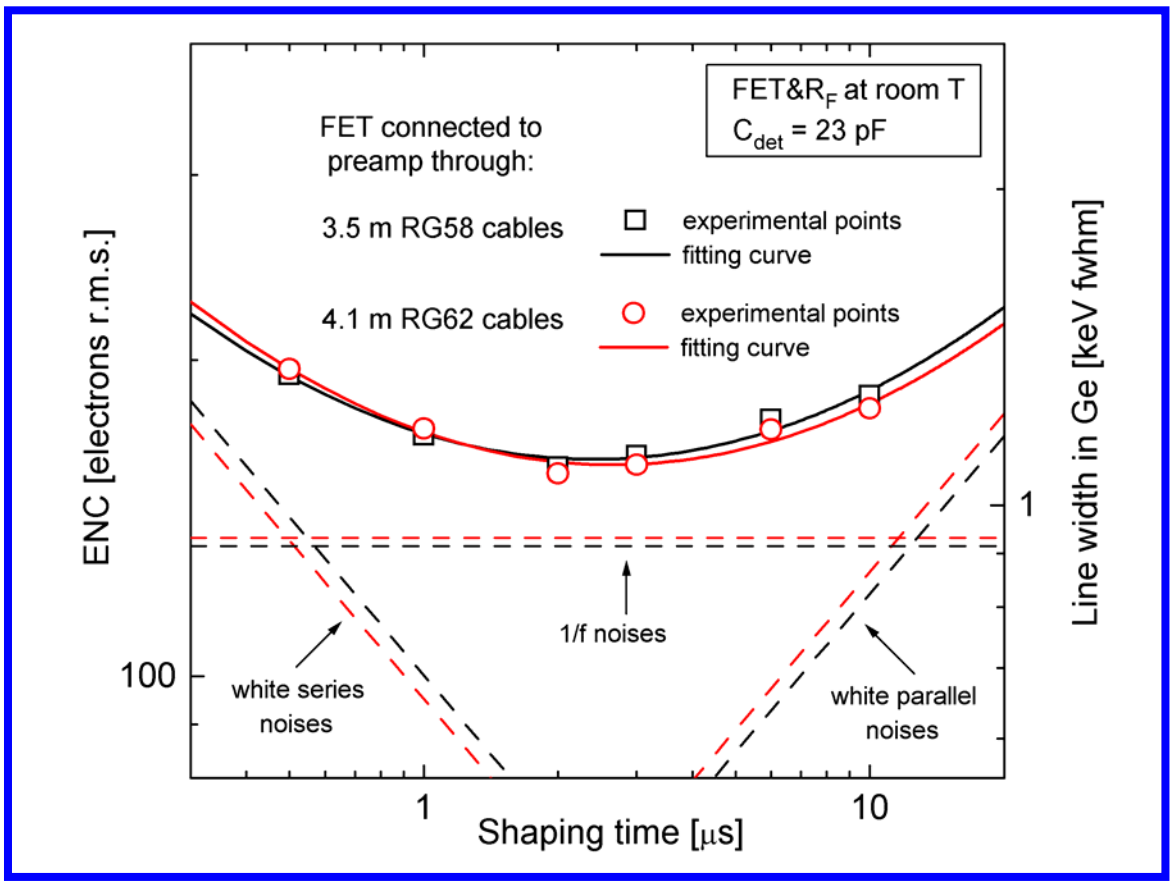
Better performance of RG62 (93 ohm) cables !

The main cause is the difference in the time delay they introduced in the signal transmission:

RG62: ≈ 4 ns/m

RG58: ≈ 5 ns/m

Noise measurements
(at the test bench, JFET at room temperature)



- FET at room temperature
- C_{det} = 23 pF
- semi-Gaussian shaper amplifier (Ortec mod.572)

Minimum at 2 μs shaping time:

156 electrons r.m.s. = 1.07 keV fwhm in HPGe

Noise turns out to be almost independent from the cable length or type

Measurements with Liquid Nitrogen

Istituto Nazionale di Fisica Nucleare

JFET and feedback components sinked in LN (77°K) and connected to the warm AGATA preamplifier (300°K) through ~ 4m RG62 cables

→ The bias point of BF862 JFET must change:

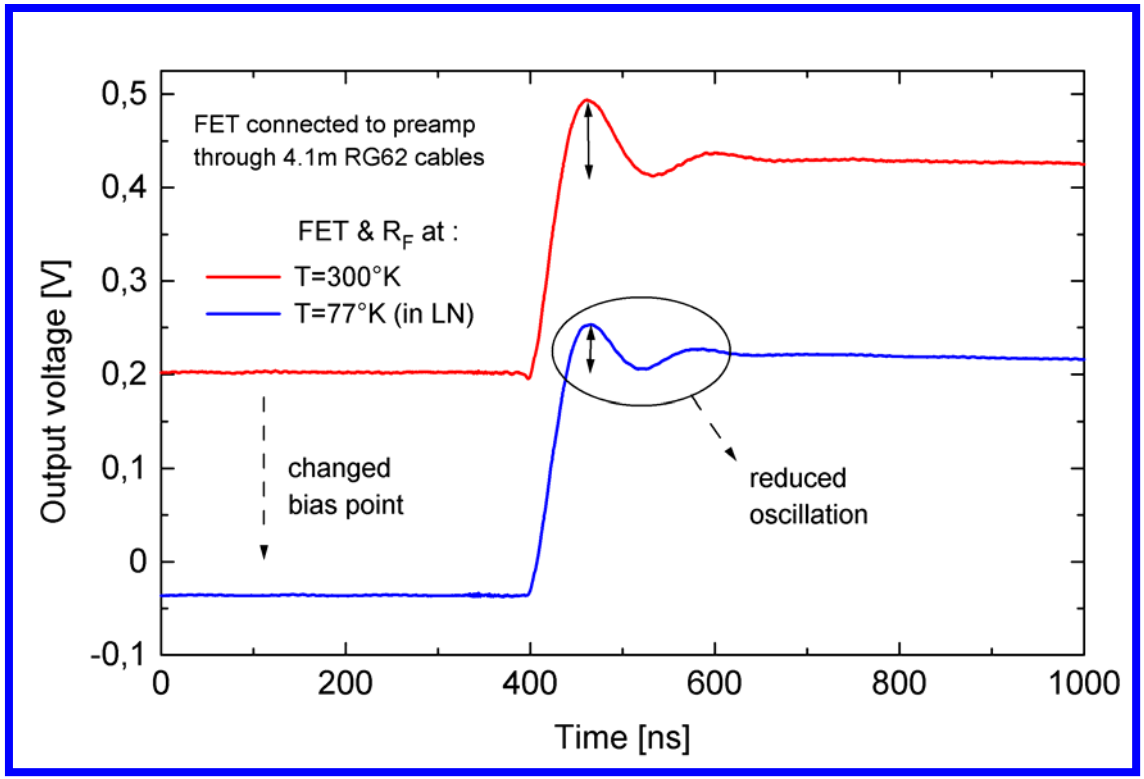
with a gate-source voltage (V_{GS}) of ~ 0V, the drain saturation current (I_{DSS}) decreases by a factor of 3 at the temperature of liquid nitrogen (77°K).

We had to reduce the drain current from ~ 10mA to ~ 3mA in order to let the JFET operate in LN.

↓

JFET transconductance g_m grows up with decreasing temperature until it reaches a maximum value at ~ 120°K BUT it strongly drops when we further decrease temperature from 120°K to 77°K

Bandwidth measurements

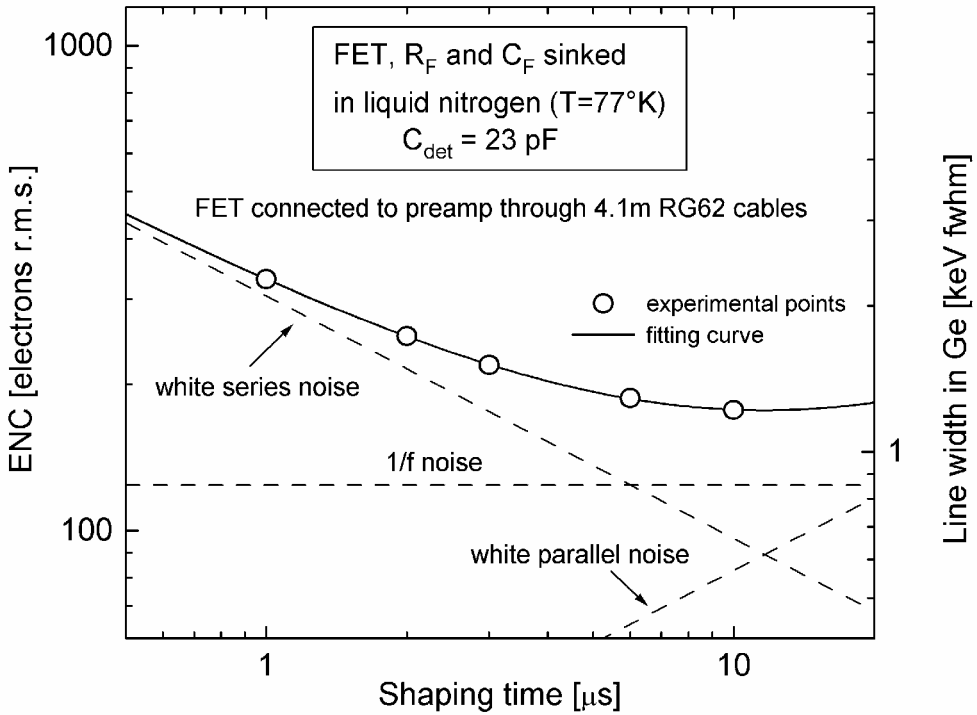


The reduced g_m causes a decrease in the charge loop gain and so a reduced bandwidth of the circuit

This decrease is not sufficient to eliminate oscillations but it only helps to partially stabilize the circuit, so that the needed compensation capacitance will have a lower value

Rise time values obtained after complete compensation (with no oscillation or overshoot) are of the same order of those measured at room temperature

Noise measurements
(at the test bench, JFET in LN)



- C_{det} = 23 pF
- semi-Gaussian shaper amplifier (Ortec mod.572)

JFET in LN (T=77°K):
minimum at 10 μs shaping time
178 electrons r.m.s. = 1.2 keV fwhm in HPGe

Remember :

JFET at room T (300°K):
minimum at 2 μs shaping time
156 electrons r.m.s. = 1.07 keV fwhm in HPGe

The reduced transconductance g_m causes a worse electronic noise !

Conclusions

In liquid nitrogen the JFET transconductance decreases: this fact helps to stabilize the circuit against the oscillations due to the delay lines in the charge loop BUT causes an increase in the electronic noise.

The performance would improve by warming the JFET a little bit.

We suggest the possibility that the JFET could warm up by itself if mounted into a vacuum box, which could also act as a shield.

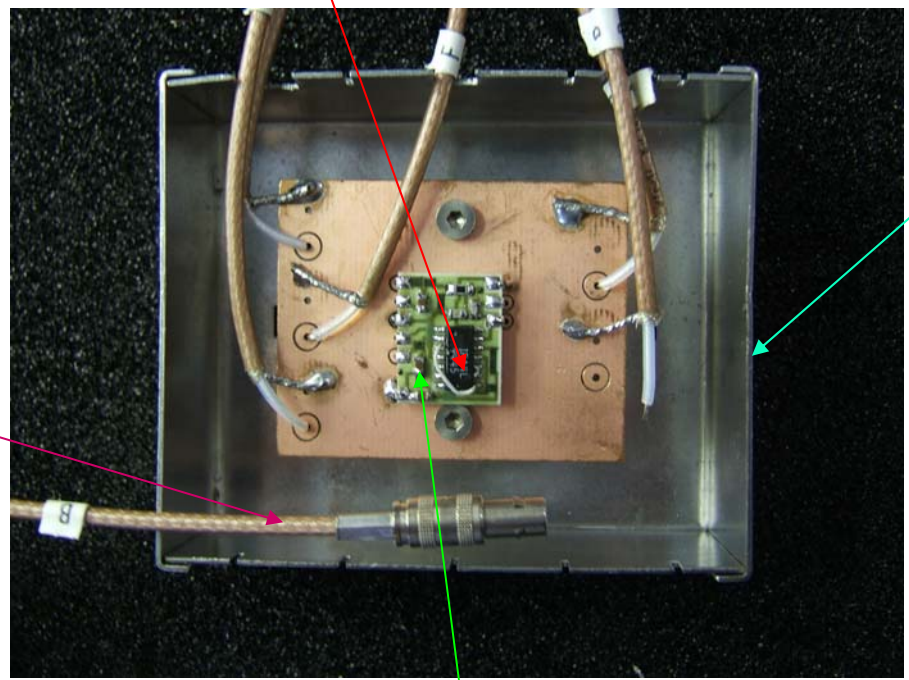
Choice of FET and preamps (2nd solution pursued)

2. Use JFET - monolithic preamps mod IPA4 developed by G.Manfredi, V. Speziali, V. Re in a INFN-MURST project, actually commercialized by InterFET co. This can be used cold! (But noise at LN never measured) → ongoing

Extremely low noise of the input JFET obtained thanks to buried layer technology and very high quality silicon.

ref. *Nucl Phys B(Proc. Suppl.) 44(1995)613-616*
NIMA 380 (1996) 308-311

The monolithic JFET preamplifier



LEMO RG58 cables

Shielding box

…… and its hybrid polarization circuit

The circuital layout of the IPA4 monolithic preamplifier

Istituto Nazionale

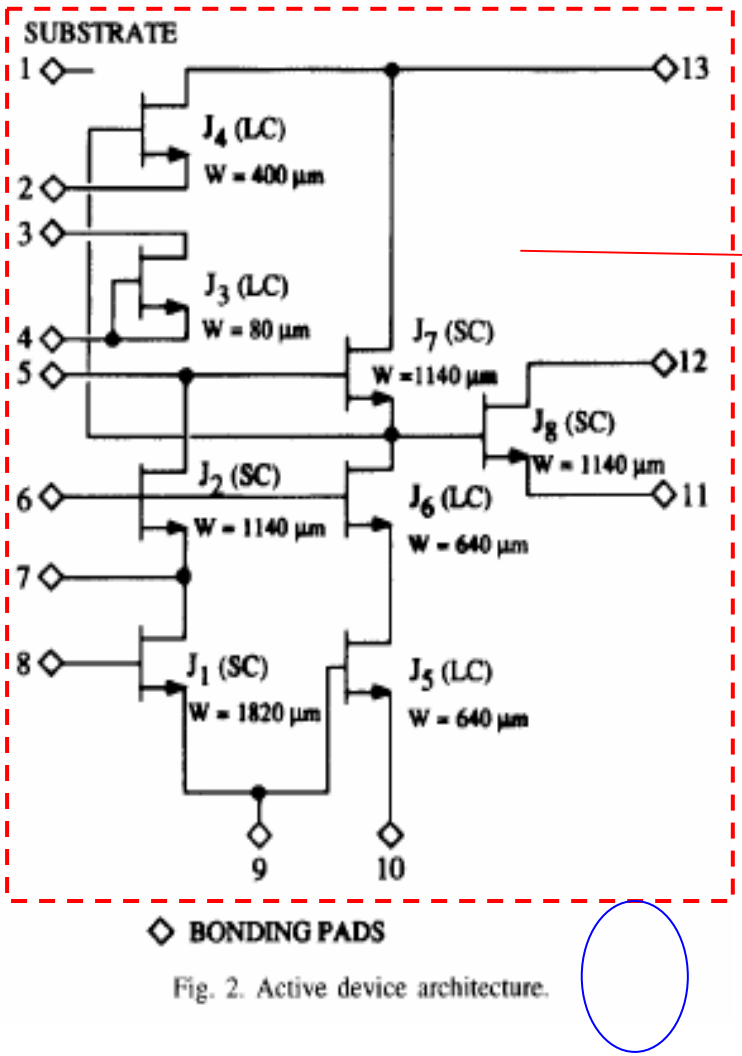
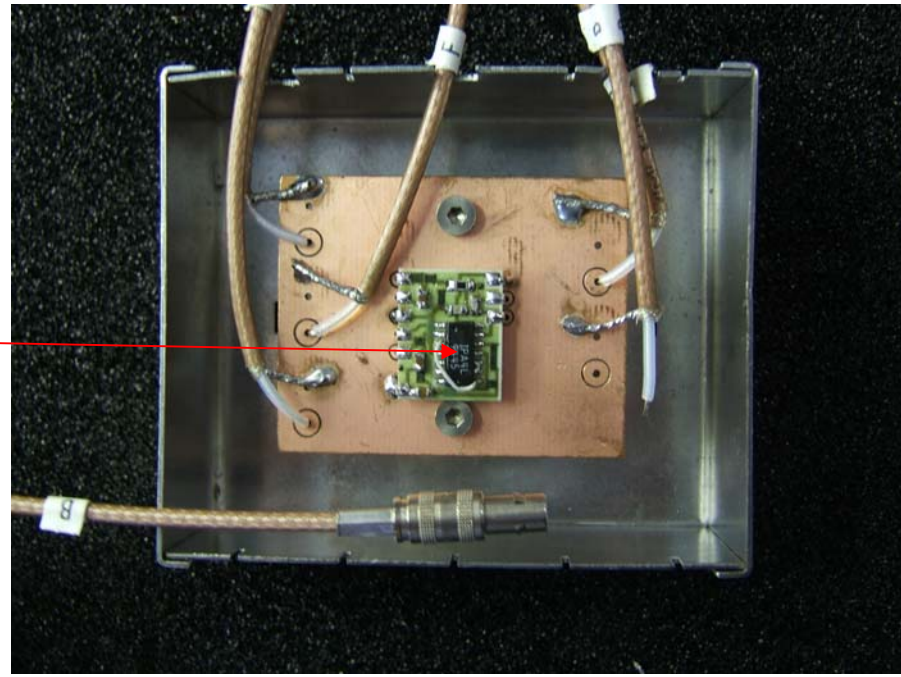
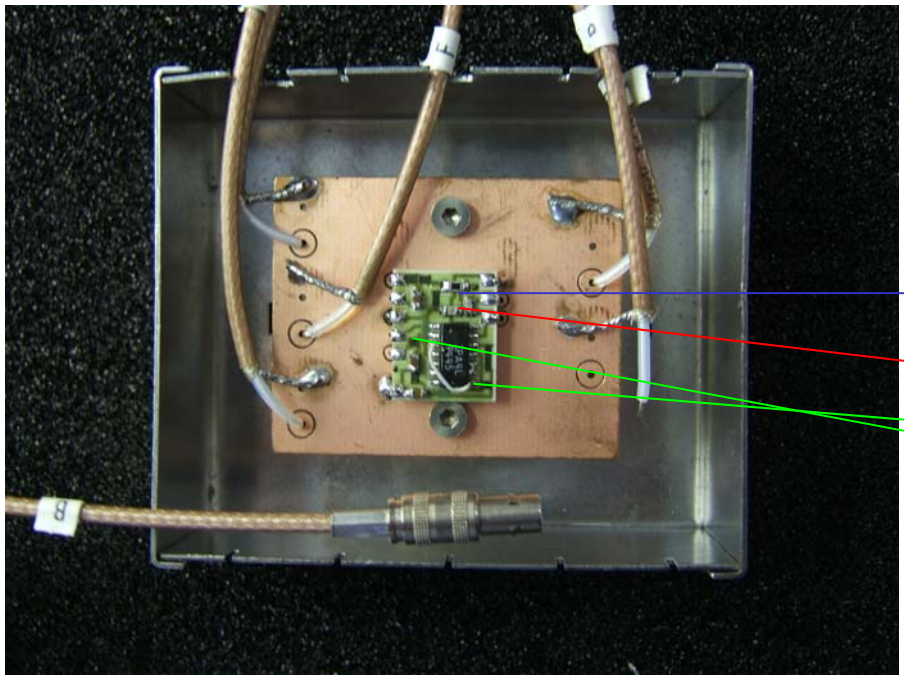


Fig. 2. Active device architecture.



The preamps is integrated, all JFET realized with buried-layer technology (better noise performances than CMOS but not faster technology, and developped for LAr for applications).

The IPA4 hybrid ciurcuit with C_fR_f and polarization components



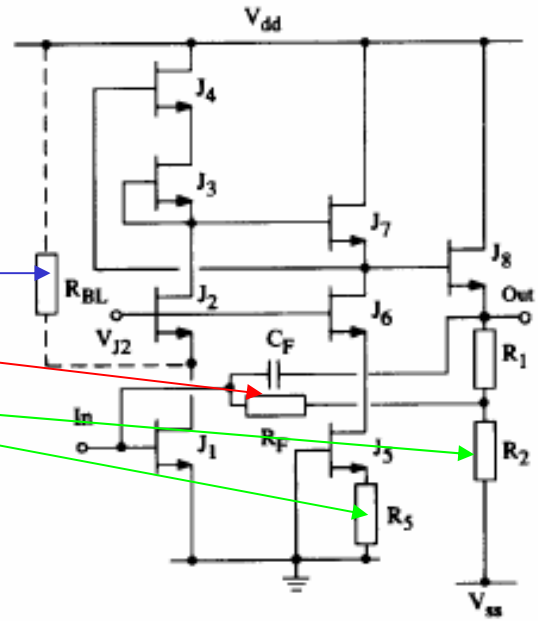


Fig. 3. A-type preamplifier configuration.

All polarization components are at present out of the preamp, to allow several preamp configurations, to fit the application. Once fixed we could ask to integrate them (but not recommended for R_F and C_F)

The IPA4 monolithic preamplifier main characteristics

Sensitivity	2 V/pC with C_f = 0.5 pF → 120 mV/1 MeV
A(f)	75 dB – 60 dB (depending on the adopted configuration)
gm_{J1}	9.7 mA/V
C_i	9 pF

Room temperature noise figure of J-FET monolithic integrated preamps.

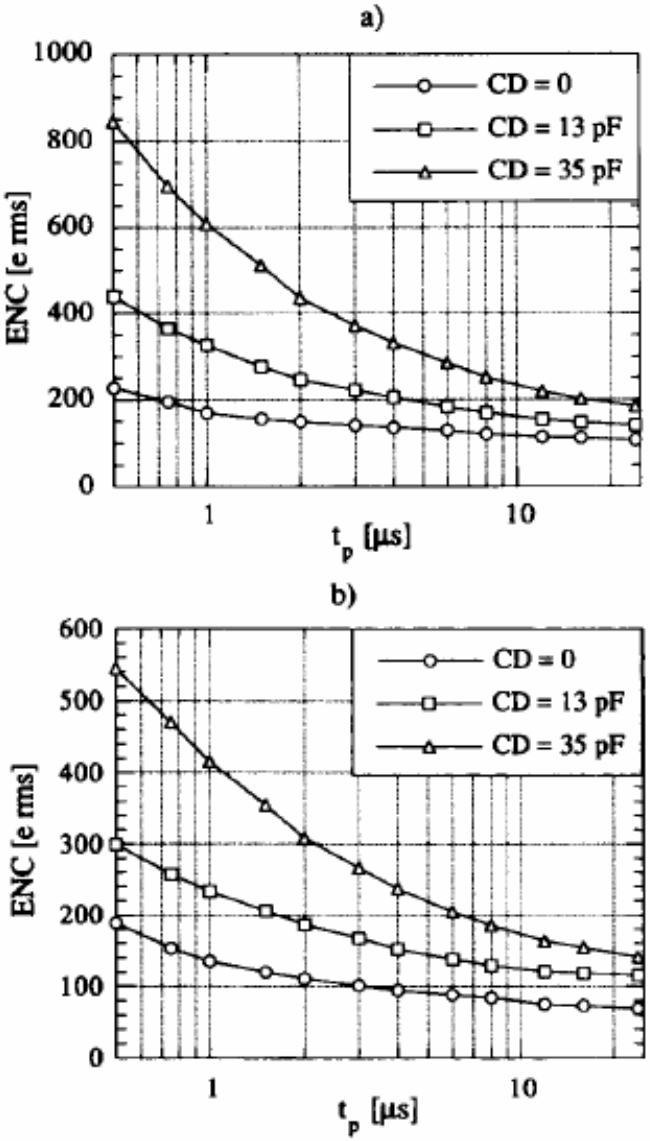


Fig. 7. ENC as a function of the peaking time t_p for the A-type preamplifier followed by a semigaussian unipolar shaper: (a) The standing current in J_1 is 0.6 mA; (b) The standing current in J_1 is 5 mA.

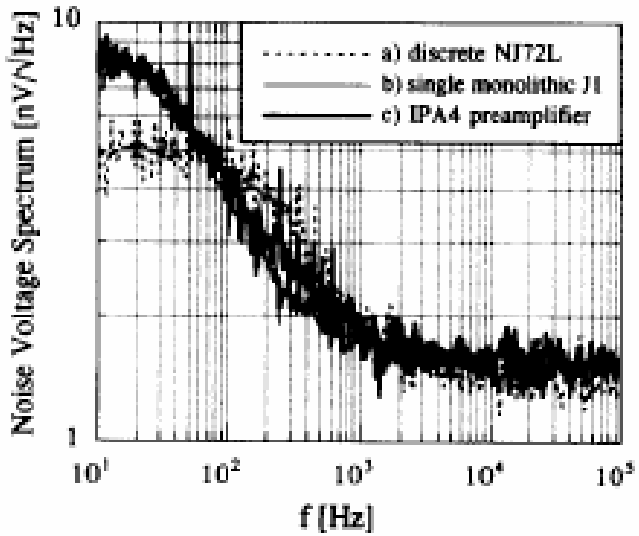
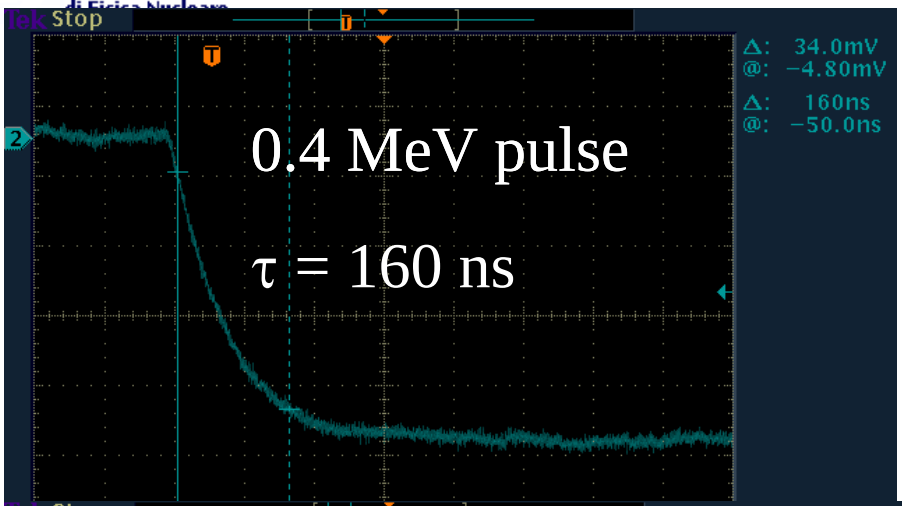
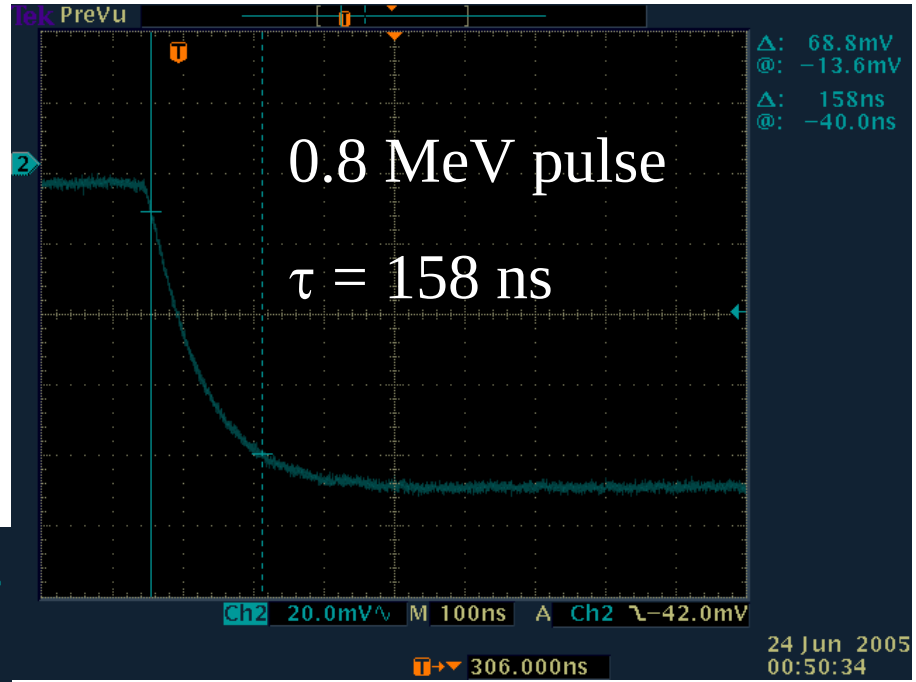
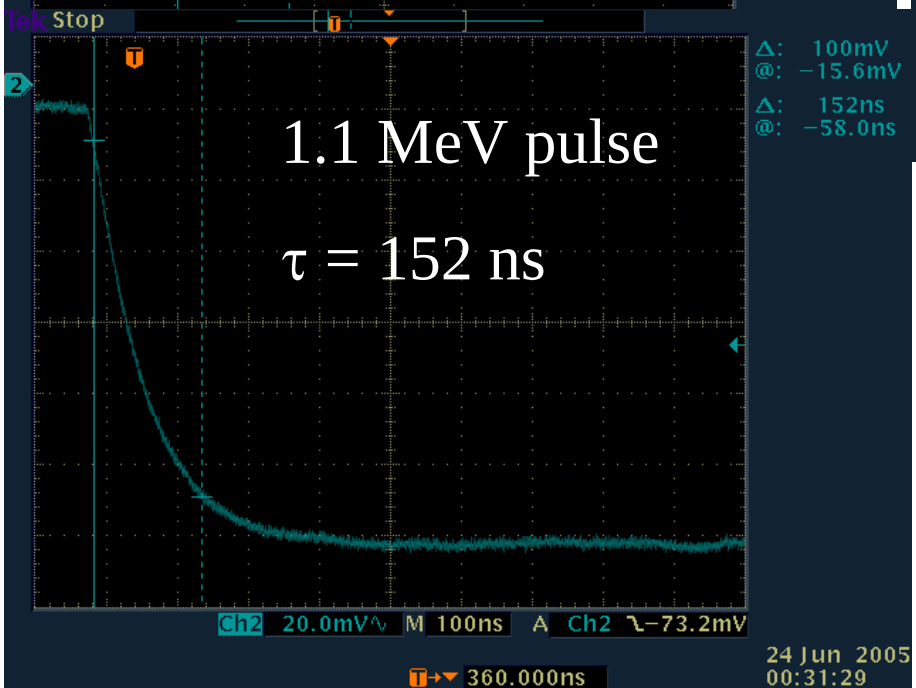


Fig. 6. Input-referred spectral densities of voltage noise as a function of frequency: (a) Discrete device with the same geometry as J_1; (b) J_1; (c) Complete preamplifier.

Measured pulses with IPA4 in LN
Vcc= (-4.9, +18 V)







Vin	Slew Rate
34 mV	0.21 mV/ns
65 mV	0.43 mV/ns
92 mV	0.66 mV/ns

→ SR limited in actual circuital configuration

Handles to Improve the Slew Rate

•Act on R_{BL} to increase the current flowing in $J_{1,}$, Replace J3 with a proper R to reduce the dynamic load of the full voltage gain node and increase Cf (but all this will reduce the gain). All polarization components are at present out of the preamp, to allow several preamp configurations to fit the application.

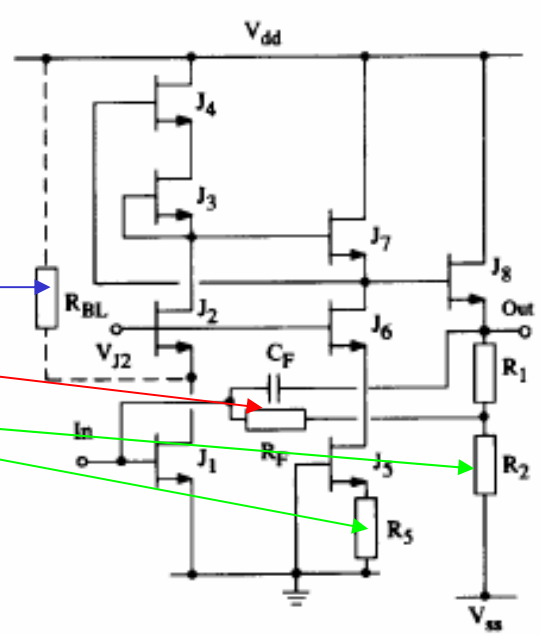


Fig. 3. A-type preamplifier configuration.

• act on the output stage to drive a low impedence load. (at the moment there is a V_{cc}^{out}= 7-9 V).

GERDA custom ASIC preamp development

- Milano: As announced on the 20th june we have submitted to Europractice (B) a circuital layout.

  AMS technology 0.8μ CMOS.

  Input FET is both integrated and not integrated.

  Cf and Rf are not integrated.

  Chips will be available October 2005.

- Hd: Starting a contract to design an ASIC circuit for GERDA . CMOS 0.6μ technology.

  Cf ad Rf will be integrated. Input FET will be integrated. Planned to submit the layout in November 2005.

Conclusions

- Present available+working solution is the discrete JFET + hybrid preamps (AGATA).

  Cables (type and lenght) play a big role in the possibility to perform PSA.
- Work on integrated monolithic JFET preamp is ongoing and we have good hope it will be a possible candidate for phase I
- ASIC custom preamp for GERDA phase I submitted on 20th june at Europractice and chip will be delivered on October 2005. To respect our schedule (choise of preamps end of 2005), the chips from first run must be OK (low probability).
- Once preamps are fixed we can choose the cables, but work on cables has to start in parallel. Test with a long cryostat (ICARUS origin) on choice of cables for hybrid and integrated preamps will start at LNGS after summer break.