# SIS3301
# 65/100 MHz
# VME FADCs

# User Manual

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## Revision Table:

| Revision | Date | Modification |
|----------|------|--------------|
| 1.00 | 20.06.02 | Generation from V3.00 SIS3300/3301 manual |
| 1.10 | 17.11.04 | Delay locked loop for clock on SIS3301 and 14-bit design firmware version |
| 1.20 | 20.07.09 | Add Compress Event Readout Version: 0x33011115 |
| 1.21 | 03.08.09 | Compress Event Readout: documentation modified |
| 1.22 | 28.09.09 | Trigger Setup registers: documentation modified |
| 1.30 | 02.10.09 | ADC clock source:<br> - add External Clock (LEMO In) direct mode (Control register)<br> - add Reset External Clock DLL feature (Acquisition Control register) |

# -　**Table of contents**

# 1    Introduction

The SIS3300/3301 are eight channel ADC/digitizer boards with a sampling rate of up to 105 MHz (for the individual channel) and a resolution of 12/14-bit. The boards are single width 6U VME card, which has no special (i.e. non standard VME) voltage requirements.
Dual memory bank functionality in conjunction with multi event memory structure and a range of trigger options give the unit the flexibility to cover a variety of applications.

Applications comprise but are not limited to:
- digitization of "slow" detectors like calorimeters
- spectroscopy with Ge-detecors
- beam profile monitor readout
- serialized readout of μ-Strip detector data

This manual describes the filtering/trigger firmware version of the SIS3300. At present this design is not implemented for the SIS3301 yet, this can be done on request on short notice however. As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm.

## 1.1   Related documents

A list of available firmware designs can be retrieved from
http://www.struck.de/sis3300firm.htm
The JTAG firmware installation procedure is described in
http://www.struck.de/sis3300_jtagprog.pdf

## 2   Technical Properties/Features

### 2.1   Key functionality

Find below a list of key features of the SIS3300 and SIS3301 digitizers.

| | SIS3300 | SIS3301-65 | SIS3301-105 |
|---|---|---|---|
| Sampling rate per channel | 105 MHz | 65 MHz | 105 MHz |
| Minimum symmetric clock | 1 MHz | 15 MHz | 15 MHz |
| Resolution | 12-bit | 14-bit | 14-bit |
| Analog bandwidth | > 80 MHz | 35 MHz [1] | |
| Typical pedestal variance | 0.7 bit | 1.1 bit [2] | |
| Differential input version | - | X | X |
| 2 x 128 KSample default | X | X | X |
| 2 x 512 KSample option | - | X | X |

[1] limited for better resolution
[2] with symmetric input range

Common properties of all boards are:

- 8 channels
- special clock modes (clock prescaling, external "arbitrary" clock)
- channel to channel crosstalk below noise (i.e. invisible in Fourier spectrum)
- external/internal clock
- multi event mode
- Read on the fly (actual sample value)
- pre/post trigger option
- Two independent memory banks
- trigger generation
- 4 NIM control inputs/4 NIM control outputs
- A32 D32/BLT32/MBLT64/2eVME
- Geographical addressing mode (in conjunction with VME64x backplane)
- Hot swap (in conjunction with VME64x backplane)
- VME64x Connectors
- VME64x Front panel(EMC shielding on request)
- VME64x extractor handles (on request)
- F1002 compatible P2 row A/C assignment
- +5 V, +12V and –12 V VME standard voltages

**Note:** The SIS3300/1 shall not be operated on P2 row A/C extensions, like VSB e.g. due to the compatibility to the F1001 FADC modules clock and start/stop distribution scheme.

## 2.2 Module design

The SIS3300 consists of four identical groups of 2 ADC channels and a control section as shown in the simplified block diagram below.

```
┌──────────────┐          ┌────────────────────────┐        ▲
│   System     │─────────▶│                        │        │
│   Clock      │          │                        │        │
└──────────────┘          │    VME Interface       │        │
                          │        and             │  VMEBus│
┌──────────────┐          │    Control FPGA        │        │
│ Front Panel  │═════════▶│                        │        │
│ Control I/O  │◀─────────│                        │        ▼
└──────────────┘          │                        │
       ▲                  └────────────────────────┘
┌──────────────┐
│   Clock      │◀─────────
│ Distribution │
└──────────────┘
```

Dual Channel Group 4 (Channels 7 and 8)

Dual Channel Group 3 (Channels 5 and 6)

Dual Channel Group 2 (Channels 3 and 4)

Dual Channel Group 1 (Channels 1 and 2)
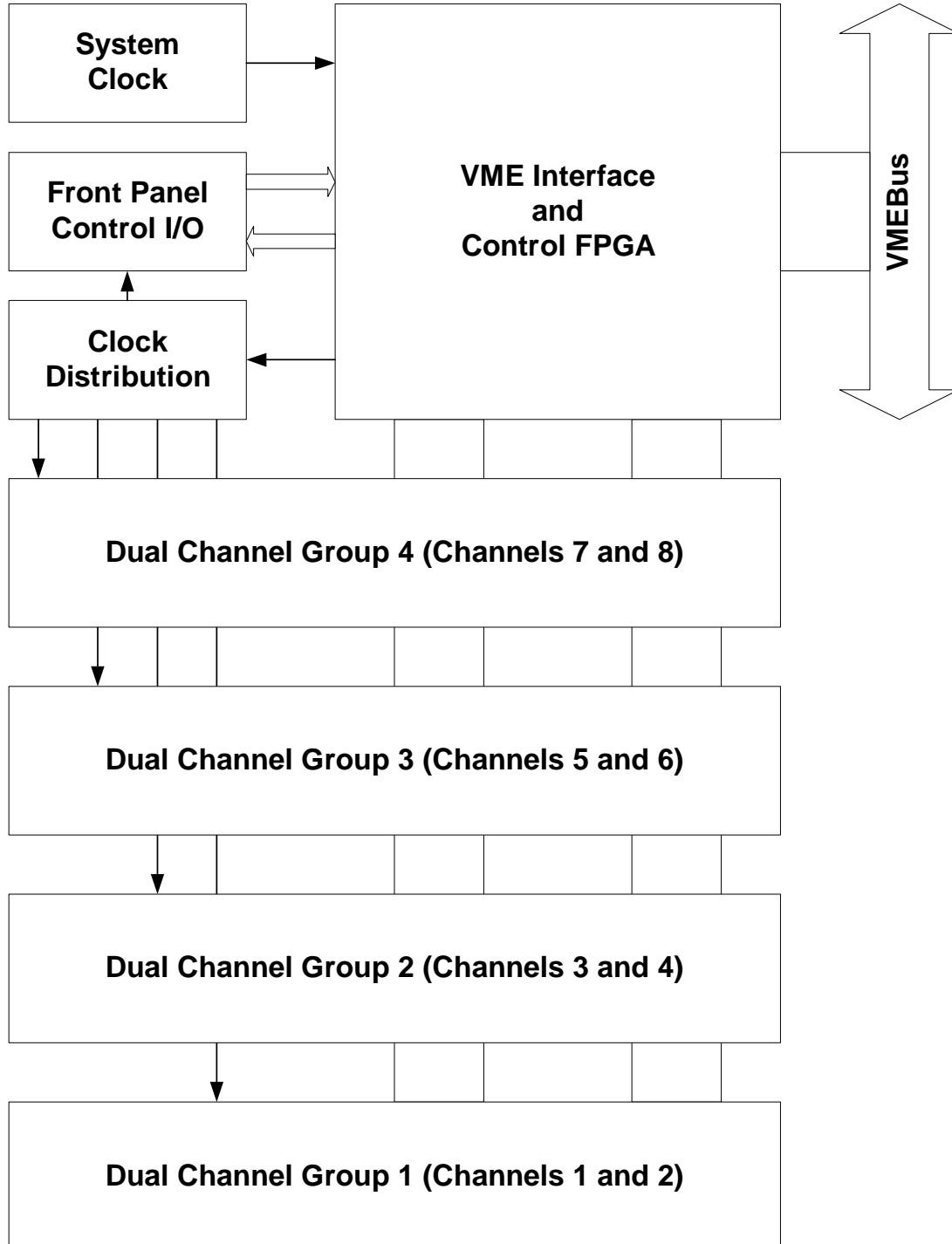
### 2.2.1 Dual channel group

Two ADC channels form a group, which memory is handled by one Field Programmable Gate Array (FPGA).
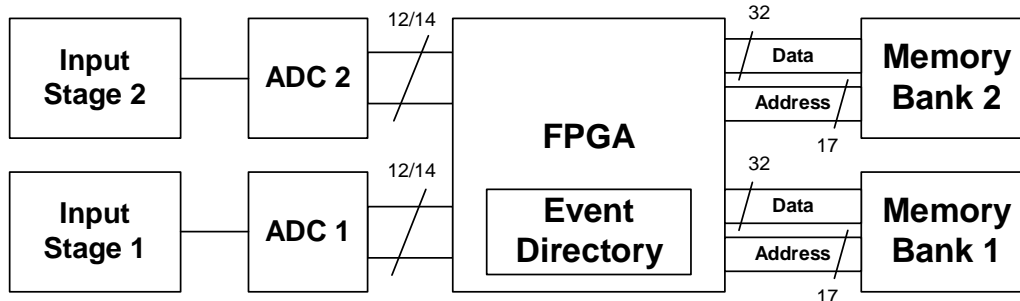


## 2.3 Modes of Operation

The SIS3300 was developed with maximum flexibility in mind. The FPGA based design of the card allows to meet the requirements of many readout applications with dedicated firmware designs in the future. The initial firmware is supposed to furnish you with an easy to use yet powerful high speed high resolution Flash Analog to Digital Converter (FADC) implementation, that covers many everyday analog to digital applications.

## 2.4 Memory management

The individual memory bank(s) can be used either as one contiguous memory or as a subdivided multi event memory. In addition memory depth can be limited in single event operation to match the requirements of the given application. The memory configuration is defined through the memory configuration register, while bank handling (on dual memory bank modules) is under control of the acquisition control register.

### 2.4.1 Single Event Mode

The full memory of 128 K Samples of the SIS3300/1 is used as one big circular buffer or as single shot memory in single event mode, unless memory size is limited by the event configuration register.

### 2.4.2 Multi Event Mode

The memory can be divided in up to 1024 pages or events to make the acquisition of shorter signals more efficient. The stop pointers for the individual page can be retrieved from the event directory. In auto start mode the ADC advances to the next page and starts sampling automatically.

### 2.4.3 Dual Bank Mode

Dual bank mode (Bank Switch mode) is available on cards (except SIS3300 V1 PCBs). The single/multi event selection will influence both memory banks in the same fashion. Data from the inactive bank can be readout, while the other bank is acquiring new data.

### 2.5 Clock sources

The SIS3300/3301 features 3 basic clock modes
- Internal clock
- External symmetric clock
- External random clock

### 2.5.1 Internal clock

The internal clock is generated from an on board 50 MHz quartz. It is either doubled by a delay locked loop to 100 MHz or divided down to lower clock frequencies. The table below lists the valid clock settings for the different SIS3300/3301 boards.

| Clock | SIS3300 | SIS3301-65 | SIS3301-105 |
|---|---|---|---|
| 100 MHz | X | - | X |
| 50 MHz | X | X | X |
| 25 MHz | X | X | X |
| 12.5 MHz | X | - | - |
| 6.25 MHz | X | - | - |
| 3.125 MHz | X | - | - |

### 2.5.2 External clock

A symmetric external clock (NIM level, ratio between 45:55 and 55:45) can be fed to the module through a LEMO00 connector. For optimum performance the clock frequency should be within the specified range for the given ADC chip.

| Module | Min. sym. clock | Max sym. clock |
|---|---|---|
| SIS3300 | 1 MHz | 105 MHz |
| SIS3301-65 | 15 MHz | 65 MHz |
| SIS3301-105 | 15 MHz | 105 MHz |

### 2.5.3 Random External Clock

Random external clock mode allows to operate the SIS3300/1 with basically arbitrary external clock pulse trains or slow external clocks. The module is clocked with the internal clock (typically at 100 MHz) and a data word will be stored to memory upon the next leading edge of the internal clock after a leading edge on the external clock input is detected. Internal pipelining has to be taken into account, the datum will precede the clock by 10 clock ticks (i.e. about 100 ns on a SIS3300 clocking at 100 MHz).

## 2.6 Trigger control (pre/post, start/stop and gate mode)

The SIS3300/1 features pre/post trigger capability as well as start/stop mode acquisition and a gate mode (in which start and stop are derived from the leading and trailing edge of a single control input signal).
The trigger behaviour is defined by the acquisition control register.

## 2.7 Internal Trigger generation

The trigger output of the SIS3300/1 can be either used to interact with external trigger logic or to base start/stop on a threshold (i.e. one individual threshold per ADC channel) of the digitized data. Trigger generation can be activated with two conditions:

- module armed (i.e. sample clock active, trigger can be used to start acquisition)
- module armed and started (trigger can be used to stop acquisition)

The user can select between triggering on the conditions above and below threshold

## 2.8 Time Stamp Memory

A 1024 x 24 bit Time Stamp Memory is implemented for each memory bank.
An internal counter starts with the first Stop trigger condition in multievent mode and it will be incremented with the sample clock or with the predivided sample clock (factor 1 to 256).
Each stop trigger condition (end of event) writes the counter value into Time Stamp Memory.

## 2.9 VME Interrupts

Two registers, the Interrupt configuration and the Interrupt control register, are implemented for interrupt setup and control.
Four Interrupt sources are implemented:

- External User Input (LEMO input 1)
- End of event
- End of last event in multievent mode
- Memory bank full in bank switch mode (Dual bank)

## 2.10 VME Readout Speed

The VME interface is optimized for readout speed. An internal FIFO/pipeline structure allows for high speed readout in block transfer mode (BLT32, MBLT64, 2eVME).

The timings below were measured with the SIS3100 (VME master) and the SIS3300/SIS3301 (VME Slave). The upper scope trace shows the VME signal DS1* (Data strobe, low active). The VME Master asserts the DS1* to request (read) data.

The lower signal shows the VME signal DTACK* (Data Acknowledge, low active). The VME Slave asserts the DTACK* to acknowledge. that the data is valid on VME.

SIS330x DS*  to DTACK* :  30-40ns

32bit every 120ns   -- >  **~ 33 MByte/sec**
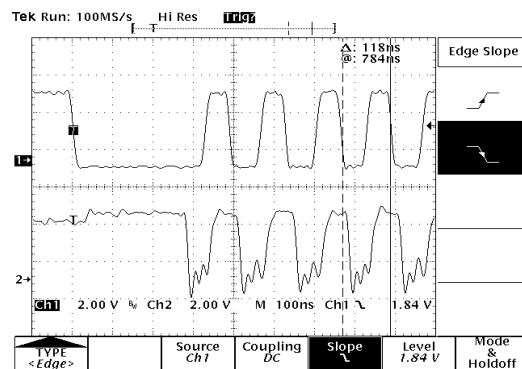


BLT32

SIS330x DS*  to DTACK* : 30-40ns

64bit every 125ns      -- >  **~ 64 MByte/sec**
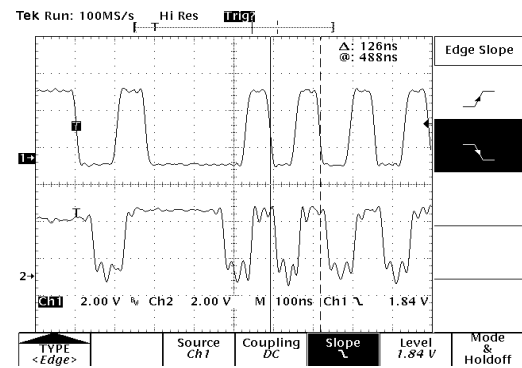


MBLT64

SIS330x DS*  to DTACK* :  50-60ns

128bit every 200ns    -->  **~ 80 MByte/sec**
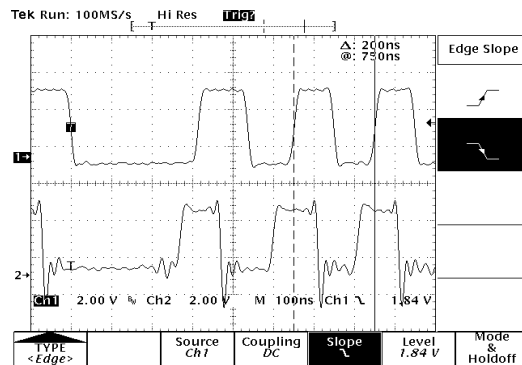


2eVME

# 3  VME Addressing

As the SIS3300 VME FADC features memory options with up to 2 banks of 4 times 128 K samples each, A32 addressing was implemented as the only option. Hence the module occupies an address space of 0xFFFFFF Bytes (i.e. 16 MBytes) are used by the module.

The SIS3300/1 firmware addressing concept is a pragmatic approach to combine standard rotary switch style settings with the use of VME64x backplane geographical addressing functionality.

The base address is defined by the selected addressing mode, which is defined by jumper array J1 and possibly SW1 and SW2 (in non geographical mode).

| | Function |
|---|---|
| | EN_A32 |
| J1 | EN_GEO |
| | EN_VIPA |
| | reserved |

The table below summarises the possible base address settings.

| J1 Setting | | | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| A32 | GEO | VIPA | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| x | | | SW1 | | | | SW2 | | | |
| x | x | | 0 | 0 | 0 | GA4 | GA3 | GA2 | GA1 | GA0 |
| | | x | Not implemented in this design | | | | | | | |

| Shorthand | Explanation |
|---|---|
| SW1/SW2 | Setting of rotary switch SW1 or SW2 respective |
| GA0-GA4 | Geographical address bit as defined by the VME64x(P) backplane |

**Notes:**
- This concept allows the use of the SIS3300/1 in standard VME as well as in VME64x environments, i.e. the user does not need to use a VME64x backplane.
- The factory default setting is EN_A32 closed, SW1=3, SW2=0 (i.e. the module will react to A32 addressing under address 0x30000000)
- Early SIS3300 boards (PCB SIS3300_V1) have a different base address scheme

## 3.1  Address Map

The SIS3300 resources and their locations are listed in the table below.
**Note:** Write access to a key address (KA)with arbitrary data invokes the respective action

| Offset | Size in Bytes | BLT | Access | Function |
|---|---|---|---|---|
| 0x00000000 | 4 | - | W/R | Control/Status Register (J-K register) |
| 0x00000004 | 4 | - | R | Module Id. and Firmware Revision register |
| 0x00000008 | 4 | - | R/W | Interrupt configuration register |
| 0x0000000C | 4 | - | R/W | Interrupt control register |
| 0x00000010 | 4 | - | R/W | Acquisition control/status register (J-K register) |
| 0x00000014 | 4 | - | R/W | Extern Start Delay register |
| 0x00000018 | 4 | - | R/W | Extern Stop Delay register |
| 0x0000001C | 4 | - | R/W | Time stamp predivider register |
| 0x00000020 | 4 | - | KA W | General Reset |
| 0x00000030 | 4 | - | KA W | VME Start sampling |
| 0x00000034 | 4 | - | KA W | VME Stop sampling |
| 0x00000040 | 4 | - | KA W | Start auto bank switch |
| 0x00000044 | 4 | - | KA W | Stop auto bank switch |
| 0x00000048 | 4 | - | KA W | Clear bank 1 memory full |
| 0x0000004C | 4 | - | KA W | Clear bank 2 memory full |
| | | | | |
| 0x00000050 | 4 | - | R/W | Start Compress Event Readout |
| 0x00000054 | 4 | - | R/W | Stop/Abort Compress Event Readout |
| 0x00001000 | 0x1000 | BLT32 | R | Event Time Stamp directory bank 1 |
| 0x00002000 | 0x1000 | BLT32 | R | Event Time Stamp directory bank 2 |
| | | | | |
| Event information all ADC groups | | | | |
| 0x00100000 | 4 | - | W only | Event configuration register (all ADCs) |
| 0x00100004 | 4 | | W only | Trigger Threshold register (all ADCs) |
| 0x0010001C | 4 | - | W only | Trigger Flag Clear Counter register (all ADCs) |
| 0x00100020 | 4 | | W only | Compress Event Readout configuration (all ADCs) |
| 0x00100028 | 4 | | W only | Trigger setup register (all ADCs) |
| 0x0010002C | 4 | | W only | Max. No of Events register (all ADCs) |
| 0x00101000 | 0x1000 | BLT32 | R | Event directory bank 1 (all ADCs) |
| 0x00102000 | 0x1000 | BLT32 | R | Eevent directory bank 2 (all ADCs) |
| | | | | |
| | | | | |
| 0x00180000 | 0x10000 | | R only | Compress Event Readout Fifo |
| | | | | |
| Event information ADC group 1 | | | | |
| 0x00200000 | 4 | - | R/W | Event configuration register (ADC1, ADC2) |
| 0x00200004 | 4 | | R/W | Trigger Threshold register (ADC1, ADC2) |
| 0x00200008 | 4 | - | R | Bank1 address counter  (ADC1, ADC2) |
| 0x0020000C | 4 | - | R | Bank2 address counter  (ADC1, ADC2) |
| 0x00200010 | 4 | - | R | Bank1 Event counter  (ADC1, ADC2) |
| 0x00200014 | 4 | - | R | Bank2 Event counter  (ADC1, ADC2) |
| 0x00200018 | 4 | - | R | Actual Sample Value  (ADC1, ADC2) |
| 0x0020001C | 4 | - | R/W | Trigger Flag Clear Counter register (ADC1, ADC2) |
| 0x00200020 | 4 | | R/W | Compress Event Readout configuration (ADC1, ADC2) |
| 0x00200028 | 4 | | R/W | Trigger setup register (ADC1, ADC2) |

| | | | | |
|---|---|---|---|---|
| 0x0020002C | 4 | | R/W | Max. No of Events register  (ADC1, ADC2) |
| 0x00201000 | 0x1000 | BLT32 | R | Event directory bank 1 (ADC1, ADC2) |
| 0x00202000 | 0x1000 | BLT32 | R | Event directory bank 2 (ADC1, ADC2) |
| | | | | |
| | | | | |
| Event information ADC group 2 | | | | |
| 0x00280000 | 4 | - | R/W | Event configuration register (ADC3, ADC4) |
| 0x00280004 | 4 | | R/W | Trigger Threshold register (ADC3, ADC4) |
| 0x00280008 | 4 | - | R | Bank1 address counter  (ADC3, ADC4) |
| 0x0028000C | 4 | - | R | Bank2 address counter  (ADC3, ADC4) |
| 0x00280010 | 4 | - | R | Bank1 Event counter  (ADC3, ADC4) |
| 0x00280014 | 4 | - | R | Bank2 Event counter  (ADC3, ADC4) |
| 0x00280018 | 4 | - | R | Actual Sample Value  (ADC3, ADC3) |
| 0x0028001C | 4 | - | R/W | Trigger Flag Clear Counter register (ADC3, ADC4) |
| 0x00280020 | 4 | | R/W | Compress Event Readout configuration (ADC3, ADC4) |
| 0x00280028 | 4 | | R/W | Trigger setup register (ADC3, ADC4) |
| 0x0028002C | 4 | | R/W | Max. No of Events register (ADC3, ADC4) |
| 0x00281000 | 0x1000 | BLT32 | R | Event directory bank 1 (ADC3, ADC4) |
| 0x00282000 | 0x1000 | BLT32 | R | Event directory bank 2 (ADC3, ADC4) |
| | | | | |
| | | | | |
| Event information ADC group 3 | | | | |
| 0x00300000 | 4 | - | R/W | Event configuration register (ADC5, ADC6) |
| 0x00300004 | 4 | | R/W | Trigger Threshold register (ADC5, ADC6) |
| 0x00300008 | 4 | - | R | Bank1 address counter  (ADC5, ADC6) |
| 0x0030000C | 4 | - | R | Bank2 address counter  (ADC5, ADC6) |
| 0x00300010 | 4 | - | R | Bank1 Event counter  (ADC5, ADC6) |
| 0x00300014 | 4 | - | R | Bank2 Event counter  (ADC5, ADC6) |
| 0x00300018 | 4 | - | R | Actual Sample Value  (ADC5, ADC6) |
| 0x0030001C | 4 | - | R/W | Trigger Flag Clear Counter register (ADC5, ADC6) |
| 0x00300020 | 4 | | R/W | Compress Event Readout configuration (ADC5, ADC6) |
| 0x00300028 | 4 | | R/W | Trigger setup register (ADC5, ADC6) |
| 0x0030002C | 4 | | R/W | Max. No of Events register (ADC5, ADC6) |
| 0x00301000 | 0x1000 | BLT32 | R | Event directory bank 1 (ADC5, ADC6) |
| 0x00302000 | 0x1000 | BLT32 | R | Event directory bank 2 (ADC5, ADC6) |
| | | | | |
| | | | | |
| Event information ADC group 4 | | | | |
| 0x00380000 | 4 | - | R/W | Event configuration Register (ADC7, ADC8) |
| 0x00380004 | 4 | | R/W | Trigger Threshold register (ADC7, ADC8) |
| 0x00380008 | 4 | - | R | Bank1 address counter  (ADC7, ADC8) |
| 0x0038000C | 4 | - | R | Bank2 address counter  (ADC7, ADC8) |
| 0x00380010 | 4 | - | R | Bank1 Event counter  (ADC7, ADC8) |
| 0x00380014 | 4 | - | R | Bank2 Event counter  (ADC7, ADC8) |
| 0x00380018 | 4 | - | R | Actual Sample Value  (ADC7, ADC8) |
| 0x0038001C | 4 | - | R/W | Trigger Flag Clear Counter register (ADC7, ADC8) |
| 0x00380020 | 4 | | R/W | Compress Event Readout configuration (ADC7, ADC8) |
| 0x00380028 | 4 | | R/W | Trigger setup register (ADC7, ADC8) |
| 0x0038002C | 4 | | R/W | Max. No of Events register (ADC7, ADC8) |
| 0x00381000 | 0x1000 | BLT32 | R | Event directory bank 1 (ADC7, ADC8) |
| 0x00382000 | 0x1000 | BLT32 | R | Event directory bank 2 (ADC7, ADC8) |
| | | | | |
| | | | | |
| Bank 1 memory | | | | |

| | | | | |
|---|---|---|---|---|
| `0x00400000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 1 memory (ADC1, ADC2) |
| `0x00480000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 1 memory (ADC3, ADC4) |
| `0x00500000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 1 memory (ADC5, ADC6) |
| `0x00580000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 1 memory (ADC7, ADC8) |
| | | | | |
| Bank 2 memory | | | | |
| `0x00600000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 2 memory (ADC1, ADC2) |
| `0x00680000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 2 memory (ADC3, ADC4) |
| `0x00700000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 2 memory (ADC5, ADC6) |
| `0x00780000` | 0x80000 | BLT32/MBLT64/2eVME | R/W* | Bank 2 memory (ADC7, ADC8) |

*W in D32 only (for memory test e.g.)

**Note 1:** The event information is identical for the four ADC groups (unless the module has a hardware problem), hence it will be sufficient for normal operation to retrieve the needed information from one group only.

**Note 2:** MBLT64  and 2eVME read access is supported from the memory banks only.

# 4 Register Description

The function of the individual registers is described in detail in this section.
The first line after the subsection header (in Courier font) like:

```
#define SIS3300_CONTROL_STATUS      0x0      /* read/write; D32 */
```

refers to the sis3300.h header file.

## 4.1 Control/Status Register(0x, write/read)

```
#define SIS3300_CONTROL_STATUS      0x0      /* read/write; D32 */
```

The control register is in charge of the control of basic properties of the SIS3300/1 board, like output signal assignment, in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

| Bit | write Function | read Function |
|---|---|---|
| 31 | Clear reserved 15 (*) | |
| 30 | Clear reserved 14 (*) | |
| 29 | Clear reserved 13 (*) | |
| 28 | Clear reserved 12 (*) | |
| 27 | Clear reserved 11 (*) | |
| 26 | clear bank full pulse to output 3 (*) | |
| 25 | clear bank full pulse to output 2 (*) | |
| 24 | clear bank full pulse to output 1 (*) | |
| 23 | Clear reserved 7 (*) | |
| 22 | Disable internal trigger routing (*) | |
| 21 | Activate trigger upon armed (*) | |
| 20 | Non inverted trigger output (*) | |
| 19 | Clear "Reset Delay Locked Loop" (DLL) for external clock (*) | Status P2_SAMPLE_IN |
| 18 | Enable user output/disable trigger output (*) | Status P2_RESET_IN |
| 17 | Clear user output (*) | Status P2_TEST_IN |
| 16 | Switch off user LED (*) | Status User Input |
| 15 | Set reserved 15 | Status Control 15 |
| 14 | Set reserved 14 | Status Control 14 |
| 13 | Set reserved 13 | Status Control 13 |
| 12 | Set reserved 12 | Status Control 12 |
| 11 | Set reserved 11 | Status Control 11 |
| 10 | set bank full pulse to output 3 | Status Bank full pulse on LEMO output 3 |
| 9 | set bank full pulse to output 2 | Status Bank full pulse on LEMO output 2 |
| 8 | set bank full pulse to output 1 | Status Bank full pulse on LEMO output 1 (highest priority) |
| 7 | Set reserved 7 | Status Control 7 |
| 6 | Enable internal trigger routing | Status trigger routing (1= to input, 0=don't route) |
| 5 | Activate trigger upon armed and started | Status trigger generation (1=armed and started, 0=armed) |
| 4 | Invert trigger output | Status trigger output inversion(1=inverted, 0=straight) |

| 3 | Set "Reset Delay Locked Loop" (DLL) for external clock (SIS3301 11 16 only) | Status Reset delay locked loop for external clock |
|---|---|---|
| 2 | Enable trigger output/disable user output | Status of user/trigger output (1=trigger output, 0=user output) |
| 1 | Set user output  (if bit 2 is not set) | Status User Output (1=output on, 0=output off) |
| 0 | Switch on user LED | Status User LED (1=LED on, 0=LED off) |

(*) denotes power up default setting

### 4.1.1  Trigger activation

Trigger generation can be activated for two states of the SIS3300/1. By default trigger generation is active as soon as the module is armed (i.e. a sample clock is active). In this mode the trigger can be used to start the digitizer (with stop condition end of event e.g.). Trigger generation upon armed and started (i.e. bit 6 of the control register set), the trigger is used to stop the module (what is a efficient mode of operation in conjunction with autostart e.g.).

### 4.1.2  Trigger routing

The trigger status is present on LEMO output 1 (with user output and multiplexer mode disabled). It can be used to form a general trigger decision with external trigger electronics, which is fed back to the corresponding input (start/stop) on the digitizer(s). The trigger is routed on board to the stop input with the internal trigger routing bit set.

### 4.1.3  Reset locked loop for external clock (SIS3301 11 16)

If this bit is set then the DLL for the external Clock (LEMO In) is in Reset state.
After clearing this bit, the DLL needs ~1000 clocks to work correctly.
The external clock for DLL has to be running continuously.
The external clock signal in the range 60-105 MHz (from a SIS3820 clock distributor e.g.) is used to drive a delay locked loop. The delay locked loop output is used as ADC clock.

### *4.2  Module Id. and Firmware Revision Register (0x4, read)*

```
#define SIS3300_MODID          0x4      /* read only; D32 */
```

This register reflects the module identification of the SIS3300/1 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

| Bit | Function | Reading |
|-----|----------|---------|
| 31 | Module Id. Bit 15 | 3 |
| 30 | Module Id. Bit 14 | |
| 29 | Module Id. Bit 13 | |
| 28 | Module Id. Bit 12 | |
| 27 | Module Id. Bit 11 | 3 |
| 26 | Module Id. Bit 10 | |
| 25 | Module Id. Bit 9 | |
| 24 | Module Id. Bit 8 | |
| 23 | Module Id. Bit 7 | 0 |
| 22 | Module Id. Bit 6 | |
| 21 | Module Id. Bit 5 | |
| 20 | Module Id. Bit 4 | |
| 19 | Module Id. Bit 3 | 0/1 |
| 18 | Module Id. Bit 2 | |
| 17 | Module Id. Bit 1 | |
| 16 | Module Id. Bit 0 | |
| 15 | Major Revision Bit 7 | 1 |
| 14 | Major Revision Bit 6 | |
| 13 | Major Revision Bit 5 | |
| 12 | Major Revision Bit 4 | |
| 11 | Major Revision Bit 3 | 1 |
| 10 | Major Revision Bit 2 | |
| 9 | Major Revision Bit 1 | |
| 8 | Major Revision Bit 0 | |
| 7 | Minor Revision Bit 7 | |
| 6 | Minor Revision Bit 6 | |
| 5 | Minor Revision Bit 5 | |
| 4 | Minor Revision Bit 4 | |
| 3 | Minor Revision Bit 3 | |
| 2 | Minor Revision Bit 2 | |
| 1 | Minor Revision Bit 1 | |
| 0 | Minor Revision Bit 0 | |

### 4.2.1  Major revision numbers

Find below a table with major revision numbers used to date

| Major revision number | Application/user |
|-----------------------|------------------|
| 0x01 to 0x0F | Generic designs |
| 0x10 | Amanda |
| 0x11 | Greta |

### *4.3 Interrupt configuration register (0x8)*

```
#define SIS3300_IRQ_CONFIG     0x8      /* read/write; D32 */
```

This read/write register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.
The interrupter type is DO8 .

### 4.3.1 IRQ mode

In RORA (release on register access) mode the interrupt will be pending until the IRQ source is cleared by specific access to the corresponding disable VME IRQ source bit. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.

In ROAK (release on acknowledge) mode , the interrupt condition will be cleared (and the IRQ source disabled) as soon as the interrupt is acknowledged by the CPU. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again. ROAK IRQ mode can be used in conjunction with the University of Bonn LINUX Tundra Universe II driver by Dr. Jürgen Hannappel on Intel based VME SBCs.

| Bit | Function | Default |
|---|---|---|
| 31 | | 0 |
| ... | | 0 |
| 16 | | 0 |
| 15 | | 0 |
| 14 | | 0 |
| 13 | | 0 |
| 12 | RORA/ROAK Mode (0: RORA; 1: ROAK) | 0 |
| 11 | VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled) | 0 |
| 10 | VME IRQ Level Bit 2 | 0 |
| 9 | VME IRQ Level Bit 1 | 0 |
| 8 | VME IRQ Level Bit 0 | 0 |
| 7 | IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle | 0 |
| 6 | IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle | 0 |
| 5 | IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle | 0 |
| 4 | IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle | 0 |
| 3 | IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle | 0 |
| 2 | IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle | 0 |
| 1 | IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle | 0 |
| 0 | IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle | 0 |

The power up default value reads 0x 00000000

## *4.4   Interrupt control register (0xC)*

```
#define SIS3300_IRQ_CONTROL        0xC       /* read/write; D32 */
```

This register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.

| Bit | Function (w) | (r) | Default |
|---|---|---|---|
| 31 | unused | Status IRQ source 3 (user input) | 0 |
| 30 | unused | Status IRQ source 2 (reserved) | 0 |
| 29 | unused | Status IRQ source 1 (end of last event, bank full) | 0 |
| 28 | unused | Status IRQ source 0 (end of event) | 0 |
| 27 | unused | Status VME IRQ | 0 |
| 26 | unused | Status internal  IRQ | 0 |
| 25 | unused | 0 | 0 |
| 24 | unused | 0 | 0 |
| 23 | Clear IRQ source 3 | Status flag source 3 | 0 |
| 22 | Clear IRQ source 2 | Status flag source 2 | 0 |
| 21 | Clear IRQ source 1 | Status flag source 1 | 0 |
| 20 | Clear IRQ source 0 | Status flag source 0 | 0 |
| 19 | Disable IRQ source 3 | 0 | 0 |
| 18 | Disable IRQ source 2 | 0 | 0 |
| 17 | Disable IRQ source 1 | 0 | 0 |
| 16 | Disable IRQ source 0 | 0 | 0 |
| 15 | unused | 0 | 0 |
| 14 | unused | 0 | 0 |
| 13 | unused | 0 | 0 |
| 12 | unused | 0 | 0 |
| 11 | unused | 0 | 0 |
| ... | ... | ... | 0 |
| 4 | unused | 0 | 0 |
| 3 | Enable IRQ source 3 | Status enable source 3 (read as 1 if enabled, 0 if disabled) | 0 |
| 2 | Enable IRQ source 2 | Status enable source 2 (read as 1 if enabled, 0 if disabled) | 0 |
| 1 | Enable IRQ source 1 | Status enable source 1 (read as 1 if enabled, 0 if disabled) | 0 |
| 0 | Enable IRQ source 0 | Status enable source 0 (read as 1 if enabled, 0 if disabled) | 0 |

The power up default value reads 0x 00000000

The generation of the status flags, the IRQ flags and the actual IRQ is illustrated with the schematic below:
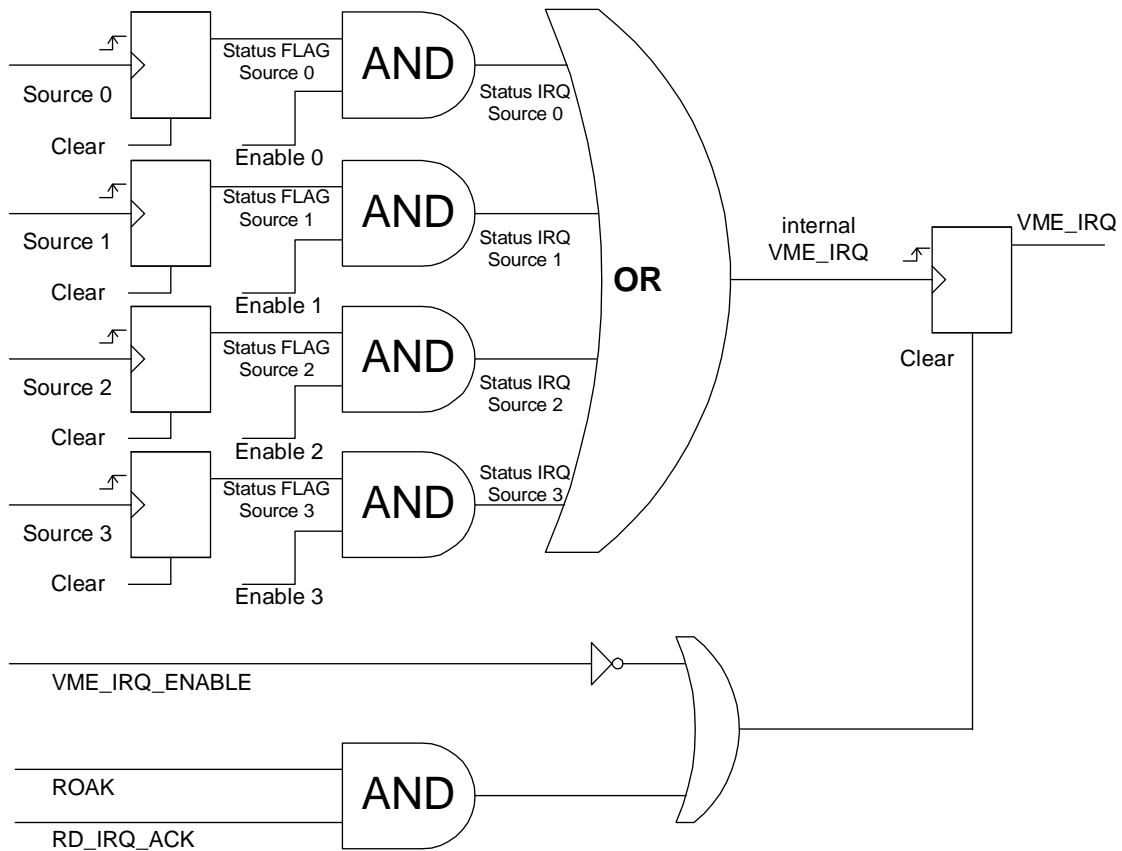
## 4.5  *Acquisition control register (0x10, read/write)*

```
#define SIS3300_ACQUISTION_CONTROL    0x10      /* read/write; D32 */
```

The acquisition control register is in charge of most of the settings related to the actual configuration of the digitization process.

Like the control register it is implemented in a J/K fashion.

| Bit | Write Function | Read |
|---|---|---|
| 31 | Clear reserved | 0 |
| 30 | Clear Clock Source Bit2 | 0 |
| 29 | Clear Clock Source Bit1 | 0 |
| 28 | Clear Clock Source Bit0 | 0 |
| 27 | Disable external clock random mode | 0 |
| 26 | Disable front panel gate mode (not start/stop) | 0 |
| 25 | Disable P2 Start/Stop logic | 0 |
| 24 | Disable front panel LEMO start/stop logic | 0 |
| 23 | Disable external stop delay | Bank 2 full |
| 22 | Disable external start delay | Bank 2 busy |
| 21 | Disable multi event mode<br>0 : Enable sample clock will be cleared with end of event<br>1 : Enable sample clock will be cleared at end of bank only<br>   (i.e. with last page of memory) | Bank 1 full |
| 20 | Disable Autostart (in multi event mode only ) | Bank 1 busy |
| 19 | Disable reserved | 0 |
| 18 | Disable auto bank switch mode | Bank switch busy |
| 17 | Disable sample clock for memory bank 2  (disarm sampling) | 0 |
| 16 | Disable sample clock for memory bank 1  (disarm sampling) | ADC_BUSY |
| 15 | Set reserved | 0 |
| 14 | Set clock source Bit 2 | Status clock source Bit 2 |
| 13 | Set clock source Bit 1 | Status clock source Bit 1 |
| 12 | Set clock source Bit 0 | Status clock source Bit 0 |
| 11 | Enable external clock random mode | Status external clock random mode |
| 10 | Enable front panel gate mode (not Start/Stop) | Status front panel gate mode |
| 9 | Enable P2 Start/Stop logic | Status P2 start/stop logic |
| 8 | Enable front panel Lemo Start/Stop logic | Status front panel start/stop logic |
| 7 | Enable stop delay (value defined by stop delay register) | Status stop delay |
| 6 | Enable start delay (value defined by start delay register) | Status start delay |
| 5 | Enable multi event mode<br>0 : Enable Sample Clock will be cleared with end of event<br>1 : Enable Sample Clock will be cleared at end of bank only<br>   (i.e. with last page of memory) | Status multi event mode |
| 4 | Enable Autostart (in multi event mode only ) | Status Autostart |
| 3 | Enable reserved | Status reserved |
| 2 | Enable auto bank switch mode | Status auto bank switch mode |
| 1 | Enable Sample Clock for Memory Bank 2  (arm for sampling) | Status sample clock bank 2 |
| 0 | Enable Sample Clock for Memory Bank 1  (arm for sampling) | Status sample clock bank 1 |

The power up default value reads 0x

Clock source bit setting table:

| Clock Source Bit2 | Clock Source Bit1 | Clock Source Bit0 | Clock Source |
|---|---|---|---|
| 0 | 0 | 0 | internal 100 MHz |
| 0 | 0 | 1 | internal 50 MHz |
| 0 | 1 | 0 | internal 25 MHz |
| 0 | 1 | 1 | internal 12.5 MHz |
| 1 | 0 | 0 | internal 6.25 MHz |
| 1 | 0 | 1 | internal 3.125 MHz |
| 1 | 1 | 0 | external clock (front panel LEMO IN 4)  via DLL |
| 1 | 1 | 1 | external clock (front panel LEMO IN 4)   direct |

Refer to the table in section 2.5.2for allowed clock speeds. Lower sampling rates into memory can be accomplished with a sampling clock within the specified range in combination with the clock predivider register in multiplexer mode or random external clock mode.

### 4.6   Start Delay register (0x14, read/write)

```
#define SIS3300_START_DELAY     0x14        /* read/write; D32 */
```

Pretrigger operation can be implemented via the start delay register in conjunction with front panel start/stop or gate mode operation. The external and autostart start signal (or leading edge of the gate) will be delayed by the value of the register+2 clocks if the external start delay is enabled in the acquisition control register.

| Bit | |
|-----|---|
| 31 | unused, read as 0 |
| ... | |
| 16 | unused, read as 0 |
| 15 | START_DELAY_BIT15 |
| .. | |
| .. | |
| 0 | START_DELAY_BIT0 |

The power up default value is 0

### 4.7   Stop Delay register (0x18, read/write)

```
#define SIS3300_STOP_DELAY      0x18        /* read/write; D32 */
```

Posttrigger operation can be implemented via the stop delay register in conjunction with front panel start/stop or gate mode operation. The external stop signal (or trailing edge of the gate) will be delayed by the value of the register+2 clocks if the stop delay is enabled in the acquisition control register.

| Bit | |
|-----|---|
| 31 | unused, read as 0 |
| ... | |
| 16 | unused, read as 0 |
| 15 | STOP_DELAY_BIT15 |
| .. | |
| .. | |
| 0 | STOP _DELAY_BIT0 |

The power up default value is 0

**Note:** The user can generate a gate of defined length (in clock ticks) by fanning a short pulse to the start and stop input with start/stop mode active, stop delay enabled and the stop delay register programmed to the desired gate width. Pipelining will have to be taken into account, i.e. the digitised signal is about 40 ns (with the module sampling at 100 MHz) ahead of the respective control signal, a fact that can be used in external trigger decisions.

For longer external trigger decisions one can consider to pipeline the ADC data in the FPGA in future firmware revisions before storing them to memory.

### 4.8   Time stamp predivider register (0x1C)

```
#define SIS3300_TIMESTAMP_PREDIVIDER   0x1C      /* read/write; D32 */
```

The (read/write) time stamp predivider register is used to define a prescale factor for the frequency of the time stamp counter. The time stamp counter counts at the clock rate with the time stamp predivider value of 0 and 1, a prescale factor of 2 ... 65535 is selected by writing the corresponding value to the register.

| Bit | |
|-----|--------------------------------|
| 31  | unused, read as 0 |
| ... | |
| 16  | unused, read as 0 |
| 15  | Time stamp predivider BIT15 |
| ..  | |
| ..  | |
| 0   | Time stamp predivider BIT0 |

The power up default value is 0

**Note:** A predivider value of 0 can not be used with firmware V201

## 4.9 Key address general reset (0x20, write)

```
#define SIS3300_KEY_RESET                    0x20   /* write only; D32 */
```

A write with arbitrary data to this register (key address) resets the SIS3300 to it's power up state.

## 4.10 Key address VME start sampling (0x30, write)

```
#define SIS3300_KEY_START                    0x30   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will initiate sampling on the active memory bank if a bank is armed for sampling.

## 4.11 Key address VME stop sampling (0x34, write)

```
#define SIS3300_KEY_STOP                     0x34   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will halt sampling on the active page. In Single Event Mode or during the last page the sampling this command will halt the the sampling.

To Abort a sampling in Multi Event / Multibank mode the following cycles have to be executed:

- issue "disable autostart" / issue KEY_STOP_AUTO_BANK_SWITCH
- issue SIS3300_KEY_STOP
- issue clear BX_ENABLE

### 4.12 Key address start Auto Bank Switch mode (0x40, write)

```
#define SIS3300_KEY_START_AUTO_BANK_SWITCH 0x40  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will start the auto bank switch mode.

### 4.13 Key address stop Auto Bank Switch mode (0x44, write)

```
#define SIS3300_KEY_STOP_AUTO_BANK_SWITCH  0x44  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will stop the auto bank switch mode.

### 4.14 Key address clear BANK1 FULL Flag  (0x48, write)

```
#define SIS3300_KEY_BANK1_FULL_FLAG        0x48  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will clear the BANK1 FULL Flag.

### 4.15 Key address clear BANK2 FULL Flag (0x4C, write)

```
#define SIS3300_KEY_BANK2_FULL_FLAG        0x4C  /* write only; D32 */
```

A write with arbitrary data to this register (key address) will clear the BANK2 FULL Flag.

## *4.16 Event Time Stamp directory bank 1 (0x1000-0x13fc, read only)*

```
#define SIS3300_EVENT_TIMESTAMP_DIR_BANK1    0x1000
                                /* read only; D32, BLT32; size: 0x400 */
```

The event time stamp directory can be used to measure time between triggers (stops) in multi event mode. A scaler counting the ADC clock is enabled with the first stop (hence the time stamp for the first event will read 0 always). The counter value (of the 24-bit wide) scaler is written to the corresponding location for subsequent events.

| offset address | Time Stamp (D23:D0) |
|----------------|---------------------|
| 0x0            | Time Stamp 0        |
| ..             |                     |
| 0x3fc          | Time Stamp 255      |

## *4.17 Event Time Stamp directory bank 2 (0x2000-0x2ffc, read only)*

```
#define SIS3300_EVENT_TIMESTAMP_DIR_BANK2    0x2000
                                /* read only; D32, BLT32; size: 0x400 */
```

As for bank 1.

| offset address | Time Stamp (D23:D0) |
|----------------|---------------------|
| 0x0            | Time Stamp 0        |
| ..             |                     |
| 0xffc          | Time Stamp 255      |

## 4.18 Event configuration registers (0x100000, 0x200000, 0x280000, 0x300000, 0x380000)

```
#define SIS3300_EVENT_CONFIG_ALL_ADC        0x100000    /* write only;D32 */


#define SIS3300_EVENT_CONFIG_ADC12          0x200000    /* read/write;D32 */
#define SIS3300_EVENT_CONFIG_ADC34          0x280000    /* read/write;D32 */
#define SIS3300_EVENT_CONFIG_ADC56          0x300000    /* read/write;D32 */
#define SIS3300_EVENT_CONFIG_ADC78          0x380000    /* read/write;D32 */
```

This register is implemented for each channel group and it has to be written with the same value, the best way is to make use of the address SIS3300_EVENT_CONFIG_ALL_ADC to write to the registers of all channel groups simultaneously.

The number of memory divisions (events) is defined by this register in multi event mode. The lowest three bits define the number of memory divisions as listed in the table below. On dual bank units both memory banks will be affected by the configuration of the event configuration register. The maximum number of events is defined by the size of the event directory, which has 256 entries. The maximum number of events is limited to 65535 in gate chaining mode to allow for shorter gates also.
.

| Bit | function |
|-----|----------|
| 31 | unused; read 0 |
| ... | ... |
| 20 | unused; read 0 |
| 19 | Event_CONF Bit 19 (reserved function) |
| 18 | Average Bit 2 |
| 17 | Average Bit 1 |
| 16 | Average Bit 0 |
| 15 | unused; read 0 |
| 14 | Event_CONF Bit 14 (reserved function) |
| 13 | Event_CONF Bit 13 (reserved function) |
| 12 | 1 (former enable trigger event directory) |
| 11 | EXTERNAL CLOCK RANDOM MODE |
| 10 | Event_CONF Bit 10 (reserved function) |
| 9 | Channel Group ID Bit 1 |
| 8 | Channel Group ID Bit 0 |
| 7 | Event_CONF Bit 7 (reserved function) |
| 6 | Event_CONF Bit 6 (reserved function) |
| 5 | Event_CONF Bit 5 (reserved function) |
| 4 | ENABLE_GATE_CHAINING_MODE |
| 3 | Enable Wrap around mode (no address auto stop) <br> 0 : Autostop at end of page <br> 1 : Wrap around page until STOP (External or KEY) |
| 2 | Page size Bit 2 |
| 1 | Page size Bit 1 |
| 0 | Page size Bit 0 |

The power up default values of the registers are

```
SIS3300_EVENT_CONFIG_ADC12:   0x00001000
SIS3300_EVENT_CONFIG_ADC34:   0x00001100
SIS3300_EVENT_CONFIG_ADC56:   0x00001200
SIS3300_EVENT_CONFIG_ADC78:   0x00001300
```

(i.e. the two channel group ID bits identify the four channel groups)

## 4.18.1 Gate chaining mode

Gate chaining mode was implemented to allow for effective acquisition of small events of arbitrary length.

Sampling in gate chaining mode will stop when:
- Maximum number of events (see 4.22.1 ) is reached
- End of bank is reached, the last event/gate may be incomplete in this case

The first data word of a gate is marked with a 1 in the G(ate) bit in memory (refer to the data format table in section 4.33). For up to 1024 events the information in the event directory is valid also. For gate chaining mode you have to

a.) enable multi event mode
b.) enable gate chaining mode

The deadtime between two gates is 8 clock ticks

**Note:** the page size (bits 2:0 of the event configuration) are ignored in gate chaining mode as the event size is defined by the gate length of the individual gate pulses (which does not have to be constant).

## 4.18.2 Averaging mode

Averaging mode is implemented to improve the signal to noise ratio in lower speed digitization applications. N consecutive samples are summed up in the FPGAs of the dual channel groups

Averaging mode is activated by specifying a non zero value for bits 18:16 of the event configuration register(s).

| Average Bit 2 | Average Bit 1 | Average Bit 0 | averaged samples |
|---|---|---|---|
| 0 | 0 | 0 | 1 (no average) |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | 32 |
| 1 | 1 | 0 | 64 |
| 1 | 1 | 1 | 128 |

### 4.18.3 EXTERNAL RANDOM CLOCK MODE

This mode allows for sampling at arbitrary low and non symmetric external clock. The digitizer is set up for internal clock and will strobe one datum to memory with the leading edge of the internal clock cycle that follows the leading edge of an external clock pulse as illustrated below. Pipelining between the actual analog input signal and the value stored to memory has to be taken into account. Both bit 11 of the acquisition control register and bit 11 of the event configuration register have to be set to acquire data in external random clock mode.
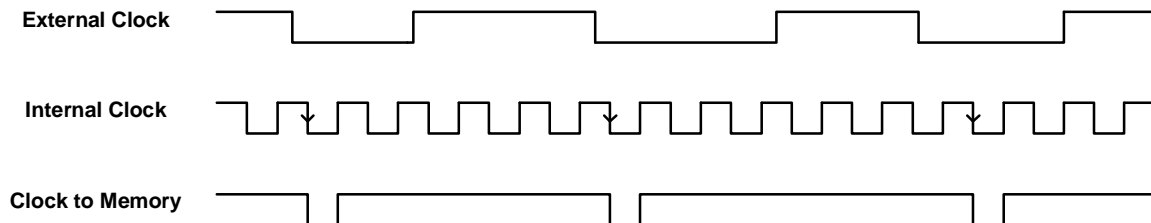


### 4.18.4 Page size

The page/event size is defined by the 3 page size bits as follows:

| Page size Bit 2 | Page size Bit 1 | Page size Bit 0 | Page size | Number of divisions (Events/Bank) |
|---|---|---|---|---|
| 0 | 0 | 0 | 128 K Samples | 1 |
| 0 | 0 | 1 | 16K Samples | 8 |
| 0 | 1 | 0 | 4 K Samples | 32 |
| 0 | 1 | 1 | 2 K Samples | 64 |
| 1 | 0 | 0 | 1 K Samples | 128 |
| 1 | 0 | 1 | 512 Samples | 256 |
| 1 | 1 | 0 | 512 Samples | 256 |
| 1 | 1 | 1 | 512 Samples | 256 |

### 4.19 Threshold registers (0x100004, 0x200004, 0x280004, 0x300004, 0x380004)

```
#define SIS3300_TRIGGER_THRESHOLD_ALL_ADC      0x100004   /* write only;D32 */
```

This register is implemented on the base of the individual channel group.
The address SIS3300_TRIGGER_THRESHOLD_ALL_ADC can be used to write the same value simultaneously to the registers of all channel groups.

```
#define SIS3300_TRIGGER_THRESHOLD_ADC12        0x200004   /* read/write;D32 */
#define SIS3300_TRIGGER_THRESHOLD_ADC34        0x280004   /* read/write;D32 */
#define SIS3300_TRIGGER_THRESHOLD_ADC56        0x300004   /* read/write;D32 */
#define SIS3300_TRIGGER_THRESHOLD_ADC78        0x380004   /* read/write;D32 */
```

These read/write registers hold the threshold values for the ADC channels 1/3/5/7 and 2/4/6/8.

| Bit | 31-16 | 15-0 |
|-----|-------|------|
| Function | threshold value ADC 1/3/5/7 | threshold value ADC 2/4/6/7 |

default after Reset:    0x0fff0fff  (disable Trigger)

## 4.20 Trigger Flag Clear Counter register (0x10001C, 0x20001C, 0x28001C, 0x3001C, 0x38001C)

```
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ALL_ADC 0x10001C  /* write only;D32 */


#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC12   0x20001C  /* read/write;D32 */
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC34   0x28001C  /* read/write;D32 */
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC56   0x30001C  /* read/write;D32 */
#define SIS3300_TRIGGER_FLAG_CLR_CNT_ADC78   0x38001C  /* read/write;D32 */
```

This register is implemented on the base of the channel group.
Use the address SIS3300_TRIGGER_FLAG_CLR_CNT_ALL_ADC to write to the registers of all channel groups simultaneously.


The Trigger Flag bit is set as soon as an ADC channel meets the trigger criterion. This flag remains latched until the next event start, i.e. it will not be cleared as new ADC data which do not meet the trigger criterion come in with Wrap mode active.
The Trigger Flag Clear Counter register allows you to define a number of samples after which the Trigger Flag bit will be cleared unless a new trigger occurred. A counter (for the given ADC channel) is preloaded with the value of the Trigger Flag Clear counter register when the trigger criterion for this channel is met. Consecutive sampling clocks will decrement the counter and the Trigger Flag bit will be cleared as soon as the counter reaches 0. If a new trigger occurs before the counter has reached 0, it will be reloaded with the value from the register (retrigger).


**Note:** typically the user may want to set the value of the Trigger Flag Clear counter register to the memory page size, but this is not mandatory.


The Trigger Flag Clear Logic is disabled if the counter is loaded with 0 (power up default).


| Bit | 31-16 | 15-0 |
|---|---|---|
| Function | unused, read back as 0 | Trigger Flag Clear counter register |

The power up default value is 0

## 4.21 No_Of_Sample register (0x100024, 0x200024, 0x280024, 0x300024, 0x380024)

```
#define SIS3300_NO_OF_SAMPLE_ALL_ADC          0x100024  /* write only;D32 */


#define SIS3300_NO_OF_SAMPLE_ADC12            0x200024  /* read/write;D32 */
#define SIS3300_NO_OF_SAMPLE_ADC34            0x280024  /* read/write;D32 */
#define SIS3300_NO_OF_SAMPLE_ADC56            0x300024  /* read/write;D32 */
#define SIS3300_NO_OF_SAMPLE_ADC78            0x380024  /* read/write;D32 */
```

This register is implemented for each channel group and it has to be written with the same value.

Use the address SIS3300_NO_OF_SAMPLE_ALL_ADC to write to the registers of all channel groups simultaneously.

The No_of_Sample factor (max. 255; 0xff)  is defined by this register. It is used in MULTIPEXER mode only.

| Bit | Function | Default |
|---|---|---|
| 31 | Unused; read 0 | 0 |
| .. | .. | |
| 8 | Unused; read 0 | 0 |
| 7 | No_Of_Sample bit 7 (MSB) | 0 |
| .. | .. | |
| 0 | No_Of_Sample bit 0 (LSB) | 0 |

The power up default value reads 0x 00000000

**Note:** The value of these registers (Clock Predivider , No_of_Sample) is copied autonomously to the 4 ADC groups. As the register is write only, the user will have to read back the value from one of the ADC groups in case read back functionality is desired.

### 4.22 Trigger setup registers (0x100028, 0x200028, 0x280028, 0x300028, 0x380028)

```
#define SIS3300_TRIGGER_SETUP_ALL_ADC         0x100028  /* write only;D32 */


#define SIS3300_TRIGGER_SETUP_ADC12           0x200028  /* read/write;D32 */
#define SIS3300_TRIGGER_SETUP_ADC34           0x280028  /* read/write;D32 */
#define SIS3300_TRIGGER_SETUP_ADC56           0x300028  /* read/write;D32 */
#define SIS3300_TRIGGER_SETUP_ADC78           0x380028  /* read/write;D32 */
```

This bit register is implemented on the channel group, the register
SIS3300_TRIGGER_SETUP_ALL_ADC is used to write to the registers of all channel groups
simultaneously.

| Bit | | |
|-----|---|---|
| 31 | reserved | |
| 30 | reserved; read 0 | |
| 29 | reserved; read 0 | |
| 28 | enable pulse mode | |
| 27 | Trigger mode ADC2 of group GT | |
| 26 | Trigger mode ADC2 of group LT | |
| 25 | Trigger mode ADC1 of group GT | |
| 24 | Trigger mode ADC1 of group LT | |
| 23 | reserved; read 0 | |
| 22 | reserved; read 0 | |
| 21 | Enable FIR test mode | |
| 20 | Test even ADC (0: ADC1 FIR data stored to ADC2 memory | |
| 19 | P bit 3 | |
| 18 | P bit 2 | Puls length P |
| 17 | P bit 1 | |
| 16 | P bit 0 | |
| 15 | G bit 7 | |
| 14 | G bit 6 | |
| 13 | G bit 5 | |
| 12 | G bit 4 | |
| 11 | G bit 3 | Gap time G |
| 10 | G bit 2 | |
| 9 | G bit 1 | |
| 8 | G bit 0 | |
| 7 | P bit 7 | |
| 6 | P bit 6 | |
| 5 | P bit 5 | |
| 4 | P bit 4 | |
| 3 | P bit 3 | Peaking time P |
| 2 | P bit 2 | |
| 1 | P bit 1 | |
| 0 | P bit 0 | |

The power up default value reads 0x 00000000

## 4.22.1 FIR Trigger

A trapezoidal FIR filter was implemented in major firmware revision 0x11 according to the document „description of a FIR filter to be implemented in the SIS3300 board" by Kai Vetter of LLNL

### 4.22.1.1      Activation/setup

FIR triggering has to be disabled before setting the peaking time, gap time and pulse length parameters.. The proper procedure is:

- disable FIR trigger (clear bit31 of trigger setup register)
- set peaking time
- set gap time
- set pulse length
- enable FIR trigger

**Note: parameter changes with FIR triggering being active**

### 4.22.1.2      Test mode

FIR filter output data can be stored to memory with FIR test mode enabled. The output data of one ADC of the dual channel group are stored to the memory of the other ADC while the ADC raw data are stored to the channels own memory portion. FIR test mode is enabled by setting bit 21 of the trigger setup register for the corresponding dual channel group. With bit 20 set also (test even ADC) FIR data of ADC2 are stored to ADC1 memory, with bit 20 cleared ADC1 FIR data are stored to ADC2 memory.

### 4.22.1.3　　Trigger generation

Trigger generation is implemented in the dual channel group FPGAs. The number of required bits for the sum depends on the peaking time. The running sum is build with the full accuracy before the result is stored to a 16-bit wide ring buffer.

P:　　　　Peaking time (number of values to sum)
G:　　　　Gap time (distance in clock ticks of the two running sums)

A setting for $P = 0$ and 1 is not valid and will be superseded with 2 automatically

## 12-bit units (SIS3300)

| | |
|---|---|
| if $P = 2$ to 7: | 16 bit (signless) add/sub; 16 bit to ring buffer [15:0] ; |
| if $P = 8$ to 15: | 17 bit (signless) add/sub; 16 bit to ring buffer [16:1] ;  shift right by 1 |
| if $P = 16$ to 31: | 18 bit (signless) add/sub; 16 bit to ring buffer [17:2] ;  shift right by 2 |
| if $P = 32$ to 63: | 19 bit (signless) add/sub; 16 bit to ring buffer [18:3] ;  shift right by 3 |
| if $P = 64$ to 127 : | 20 bit (signless) add/sub; 16 bit to ring buffer [19:4] ;  shift right by 4 |
| if $P = 128$ to 255: | 21 bit (signless) add/sub; 16 bit to ring buffer [20:5] ;  shift right by 5 |

## 14-bit units (SIS3301)

| | |
|---|---|
| if $P = 2$ to 7: | 16 bit (signless) add/sub; 16 bit to ring buffer [17:2] ;  shift right by 2 |
| if $P = 8$ to 15: | 17 bit (signless) add/sub; 16 bit to ring buffer [18:3] ;  shift right by 3 |
| if $P = 16$ to 31: | 18 bit (signless) add/sub; 16 bit to ring buffer [19:4] ;  shift right by 4 |
| if $P = 32$ to 63: | 19 bit (signless) add/sub; 16 bit to ring buffer [20:5] ;  shift right by 5 |
| if $P = 64$ to 127 : | 20 bit (signless) add/sub; 16 bit to ring buffer [21:6] ;  shift right by 6 |
| if $P = 128$ to 255: | 21 bit (signless) add/sub; 16 bit to ring buffer [22:7] ;  shift right by 7 |

SUM1  = 0 ;
for (i=G; i<(G+P); i++) SUM1 = SUM1  + adc_value[i]

SUM2  = 0 ;
for (i=0; i<P; i++)  SUM2 = SUM2  + adc_value[i]

Trigger sum:　　　　((SUM1 – SUM2) >> x   + 0x8000)　　　　x: see above

0xffff

　　　　if (SUM1 > SUM2)

0x8000　　　if  (SUM1 == SUM2)

　　　　if (SUM1 <  SUM2)

0x0

#### 4.22.1.4      Trigger example

The screenshot below shows a signal on ADC channel 1 and the resulting FIR value with test mode enabled. The trigger condition is set to LT, the hexadecimal threshold ist at 0x7E00, what results in a decimal threshold of –102 counts (0x7E00-0x8000=-0x200, this has to be shifted to the left by 1 bit as the peaking time p is in between of 8 and 15, the resulting 1024 has to be divided by the peaking time P 10 again. This mechanism is implemented in the example software also.
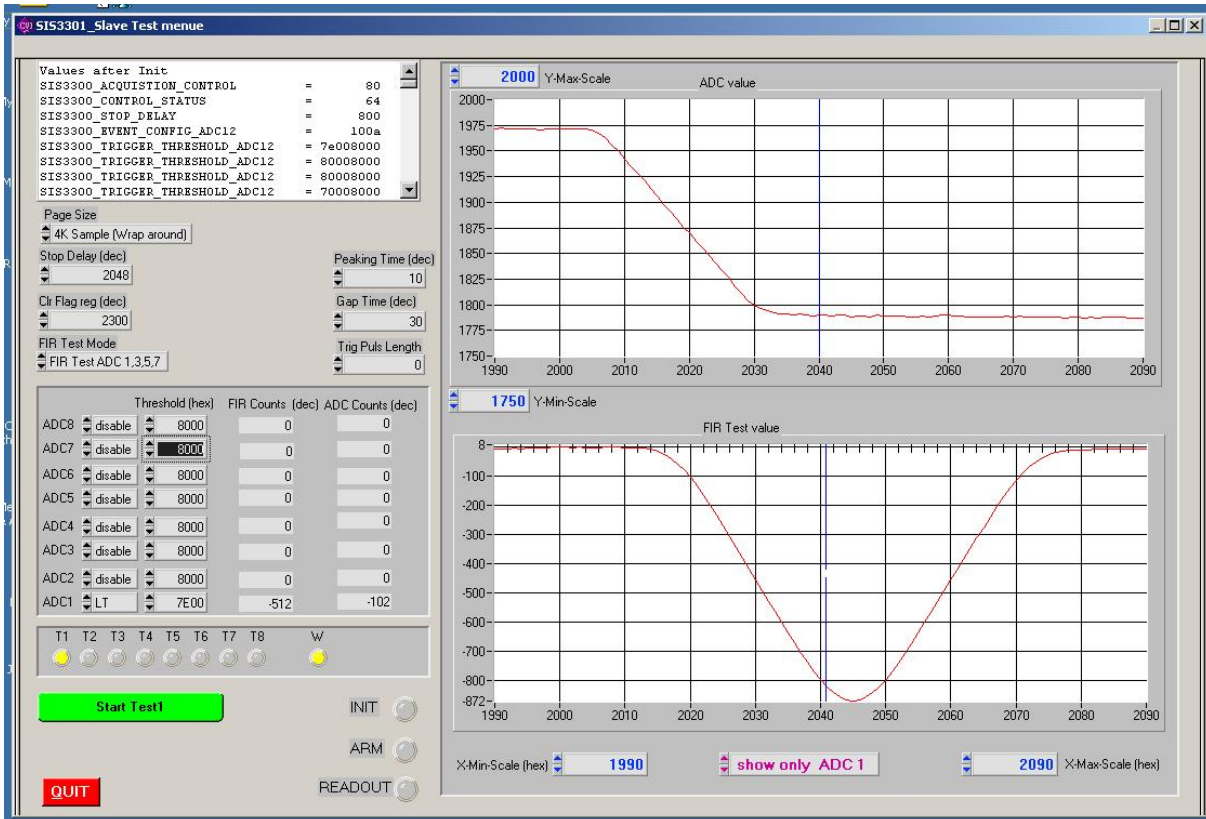
## 4.23 MAX No of Events registers *(0x10002C, 0x20002C, 0x28002C, 0x30002C, 0x38002C)*

```
#define SIS3300_MAX_NO_OF_EVENTS_ALL_ADC      0x10002C  /* write only;D32 */

#define SIS3300_ MAX_NO_OF_EVENTS_ADC12        0x20002C  /* read/write;D32 */
#define SIS3300_ MAX_NO_OF_EVENTS_ADC34        0x28002C  /* read/write;D32 */
#define SIS3300_ MAX_NO_OF_EVENTS_ADC56        0x30002C  /* read/write;D32 */
#define SIS3300_ MAX_NO_OF_EVENTS_ADC78        0x38002C  /* read/write;D32 */
```

This register is implemented for each channel group and it has to be configured to the same value in all groups, what is done most straightforward by writing to the address `SIS3300_MAX_NO_OF_EVENTS_ALL_ADC`.

This register is used in GATE Chaining / Multi Event Mode only.
It limits the number of Events in the GATE Chaining / Multi Event Mode.

ate chaining mode sampling will stop when
a.) the maximum number of events is reached or
b.) the end of bank is reached. In this case the last event/gate may be incomplete.

| Bit | 31-16 | 15-0 |
|---|---|---|
| Function | unused, read back as 0 | Max_No_Of_Events |

The power up default value is 0

## 4.24 Trigger event directory bank 1 (0x101000 – 0x101ffc)

```
#define SIS3300_EVENT_DIRECTORY_BANK1_ALL_ADC  0x101000
                                /* read only; D32, BLT32; size: 0x1000 */
```

This Trigger event directory holds the stop pointer(s) (i.e. end address+1) of memory bank 1. The directory is 32 bits wide, a wrap around bit (i.e. bit 19) will be set if the page was filled at least once (i.e. if the memory pointer has reached the end )

| offset address | (D31) | (D30) | (D29) | (D28) | (D27) | (D26) | (D25) | (D24) | (D23:20) | (D19) | (D18:D17) | Event Data End Address (D16:D0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | 0 | W | 0 | (End Address + 1) of Event 0 |
| .. | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | | ... |
| 0xffc | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | 0 | W | 0 | (End Address + 1) of Event 1023 |

W: wrap around bit
T1-T8 trigger information ADC 1 - ADC 8,
     1: ADC channel has met trigger criterion for this event
     0: ADC channel has not triggered for this event

## 4.25 Trigger event directory bank 2 (0x102000 – 0x102ffc)

```
#define SIS3300_EVENT_DIRECTORY_BANK2_ALL_ADC  0x102000
                                /* read only; D32, BLT32; size: 0x1000 */
```
Same as above, but for bank 2.

### *4.26 Event directories bank 1 ( 0x201000 – 0x201ffc, 0x281000 – 0x281ffc, 0x301000 – 0x301ffc, 0x381000 – 0x381ffc)*

```
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC12    0x201000
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC34    0x281000
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC56    0x301000
#define SIS3300_EVENT_DIRECTORY_BANK1_ADC78    0x381000
                              /* read only; D32, BLT32; size: 0x1000 */
```

These arrays are redundant and not used in standard operation, use the trigger event directory instead.

The event directories hold the stop pointer(s) (i.e. end address+1) of each channel group of memory bank 1.

The directories are 32 bits wide, a wrap around bit (i.e. bit 19) will be set if the page was filled at least once (i.e. if the memory pointer has reached the end )

### 4.26.1 Bank1_ADC12 (0x2001000)

| offset address | (D31) | (D30) | (D29) | (D28) | (D27) | (D26) | (D25) | (D24) | (D23:20) | (D19) | (D18:D17) | Event Data End Address (D16:D0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0 | T1 | T2 | | | | | | | 0 | W | 0 | (End Address + 1) of Event 0 |
| .. | ... | | | | | | | | ... | ... | | ... |
| 0xffc | T1 | T2 | | | | | | | 0 | W | 0 | (End Address + 1) of Event 1023 |

W: wrap around bit
T1, T2 trigger information ADC 1 and ADC 2

### 4.26.2 Bank1_ADC12 (0x2801000)

| offset address | (D31) | (D30) | (D29) | (D28) | (D27) | (D26) | (D25) | (D24) | (D23:20) | (D19) | (D18:D17) | Event Data End Address (D16:D0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0 | | | T3 | T4 | | | | | 0 | W | 0 | (End Address + 1) of Event 0 |
| .. | ... | | | | | | | | ... | ... | | ... |
| 0xffc | | | T3 | T4 | | | | | 0 | W | 0 | (End Address + 1) of Event 1023 |

W: wrap around bit
T3, T4 trigger information ADC 3 and ADC 4

### 4.26.3 Bank1_ADC56 (0x3001000)

| offset address | (D31) | (D30) | (D29) | (D28) | (D27) | (D26) | (D25) | (D24) | (D23:20) | (D19) | (D18:D17) | Event Data End Address (D16:D0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0 | | | | | T5 | T6 | | | 0 | W | 0 | (End Address + 1) of Event 0 |
| .. | ... | | | | | | | | ... | ... | | ... |
| 0xffc | | | | | T5 | T6 | | | 0 | W | 0 | (End Address + 1) of Event 1023 |

W: wrap around bit
T5, T6 trigger information ADC 5 and ADC 6

### 4.26.4 Bank1_ADC78 (0x3801000)

| offset address | (D31) | (D30) | (D29) | (D28) | (D27) | (D26) | (D25) | (D24) | (D23:20) | (D19) | (D18:D17) | Event Data End Address (D16:D0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0 | | | | | | | T7 | T8 | 0 | W | 0 | (End Address + 1) of Event 0 |
| .. | ... | | | | | | | | ... | ... | | ... |
| 0xffc | | | | | | | T7 | T8 | 0 | W | 0 | (End Address + 1) of Event 1023 |

W: wrap around bit
T7, T8 trigger information ADC 7 and ADC 8

### 4.27 Event directories bank 2 ( 0x202000 – 0x202ffc, 0x282000 – 0x282ffc, 0x302000 – 0x302ffc, 0x382000 – 0x382ffc)

```
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC12     0x202000
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC34     0x282000
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC56     0x302000
#define SIS3300_EVENT_DIRECTORY_BANK2_ADC78     0x382000
                            /* read only; D32, BLT32; size: 0x1000 */
```

Same as above, but for bank 2.

### 4.28 Bank 1 address counter (0x200008, 0x280008, 0x300008, 0x380008)

```
#define SIS3300_BANK1_ADDR_CNT_ADC12        0x200008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC34        0x280008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC56        0x300008   /* read only;D32 */
#define SIS3300_BANK1_ADDR_CNT_ADC78        0x380008   /* read only;D32 */
```

These read only registers hold the current bank 1 address counter for ADC group 1/2/3/4 and bank. The counter is 17 –bit wide. The counter will change while the ADC is sampling, after the ADC was stopped, the stop position can be retrieved (in multi event mode it will have to be read from the event directory). The address counter points to the next memory location that will be written to (see Trigger event directory also).

The register is implemented on the channel group base, but the information is redundant and in the standard readout case you will want to retrieve the information from one channel group only.

| Bit | 31-17 | 16-0[*] |
|---|---|---|
| Function | unused, read back as 0 | address counter |

The address counter is not in a defined state after power up or Key Reset

[*] Unused bits are not updated and may contain arbitrary data, i.e. only the number of bits that corresponds to the selected page size will hold significant data (example: the lowest 7 bits are valid for a page size of 128).

### 4.29 Bank 2 address counter (0x20000C, 0x28000C, 0x30000C, 0x38000C)

```
#define SIS3300_BANK2_ADDR_CNT_ADC12        0x20000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC34        0x28000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC56        0x30000C   /* read only;D32 */
#define SIS3300_BANK2_ADDR_CNT_ADC78        0x38000C   /* read only;D32 */
```

Same as bank 1 address counters, but for bank 2 of ADC groups 1/2/3/4.

### 4.30 Bank 1 event counter (0x200010, 0x280010, 0x300010, 0x380010)

```
#define SIS3300_BANK1_EVENT_CNT_ADC12      0x200010   /* read only;D32 */
#define SIS3300_BANK1_EVENT_CNT_ADC34      0x280010   /* read only;D32 */
#define SIS3300_BANK1_EVENT_CNT_ADC56      0x300010   /* read only;D32 */
#define SIS3300_BANK1_EVENT_CNT_ADC78      0x380010   /* read only;D32 */
```

This read only registers hold the current bank 1 event counter for ADC groups 1/2/3/4. The counter is 12–bit wide. The counter will change while the ADC is sampling (as events are coming in). The returned value is the current event number.

The register is implemented on the channel group base, but the information is redundant and in the standard readout case you will want to retrieve the information from one channel group only.

| Bit | 31-16 | 15-0 |
|---|---|---|
| Function | unused, read back as 0 | event counter |

The event counter is not in a defined state after power up or Key Reset

### 4.31 Bank 2 event counter (0x200014, 0x280014, 0x300014, 0x380014)

```
#define SIS3300_BANK2_EVENT_CNT_ADC12      0x200014   /* read only;D32 */
#define SIS3300_BANK2_EVENT_CNT_ADC34      0x280014   /* read only;D32 */
#define SIS3300_BANK2_EVENT_CNT_ADC56      0x300014   /* read only;D32 */
#define SIS3300_BANK2_EVENT_CNT_ADC78      0x380014   /* read only;D32 */
```

Same as bank 1 event counter, but for bank 2 of ADC groups 1-4.

### 4.32 Actual Sample registers (0x200018, 0x280018, 0x300018, 0x380018)

```
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC12   0x200018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC34   0x200018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC56   0x200018   /* read only;D32 */
#define SIS3300_ACTUAL_SAMPLE_VALUE_ADC78   0x200018   /* read only;D32 */
```

Read "on the fly" of the actual converted ADC values.
The registers are updated with every ADC clock, unless a concurrent VME read access is pending.
The register contents is refreshed and can be read any time (i.e. they are updated independent of the unarmed, armed, sampling state) as long as a sampling clock is distributed on the ADC board (internal clock or active/clocking external clock)

For SIS3300:

| ADC 1 / 3 / 5 / 7 | | | ADC 2 / 4 / 6 / 8 | | |
|---|---|---|---|---|---|
| D31:29 | D28 | D27:16 | D15:13 | D12 | D11:0 |
| 0 0 0 | OR  bit | 12-bit data | 0 0 0 | OR  bit | 12-bit data |

For SIS3301:

| ADC 1 / 3 / 5 / 7 | | | ADC 2 / 4 / 6 / 8 | | |
|---|---|---|---|---|---|
| D31 | D30 | D29:16 | D15 | D14 | D13:0 |
| 0 | OR  bit | 14-bit data | 0 | OR  bit | 14-bit data |

OR :   Out of range, set with over or underflow

### 4.33 Bank 1 memory  (0x400000 – 0x5ffffc)

```
#define SIS3300_MEMBASE_BANK1_ADC12              0x400000
#define SIS3300_MEMBASE_BANK1_ADC34              0x480000
#define SIS3300_MEMBASE_BANK1_ADC56              0x500000
#define SIS3300_MEMBASE_BANK1_ADC78              0x580000
        /* write D32; read D32, BLT32, MBL64, 2eVME; size: 0x80000 */
```

Bank1 memory is divided into 4 channel groups of 128 KSamples each (i.e. 512 KByte deep for every channel group, 2MByte in total). The 32-bit wide memory locations hold the data of 2 ADCs each. Readout can be done with D32, BLT32,  MBLT64 or 2eVME, for memory tests D32 write cycles only are supported.

**Notes:**
- "FIFO" block transfer cycles (i.e. readout from a constant VME address in block transfer) are supported from every channel group (internal 17-bit address counter, A18 to A2)
- 2eVME cycles have to start on a 0x100 boundary (0x0, 0x100, 0x200 ...)

Data format for SIS3300:

| offset address | ADC 1 / 3 / 5 / 7 | | | | ADC 2 / 4 / 6 / 8 | | | |
|---|---|---|---|---|---|---|---|---|
| | D31 | D30:29 | D28 | D27:16 | D15 | D14:13 | D12 | D11:0 |
| 0x0 | U | 0 0 | OR bit | 12-bit data | G | 0 0 | OR bit | 12-bit data |
| .. | | | | | | | | |
| 0x7fffc | U | 0 0 | OR bit | 12-bit data | G | 0 0 | OR bit | 12-bit data |

Data format for SIS3301:

| offset address | ADC 1 / 3 / 5 / 7 | | | ADC 2 / 4 / 6 / 8 | | |
|---|---|---|---|---|---|---|
| | D31 | D30 | D29:16 | D15 | D14 | D13:0 |
| 0x0 | U | OR  bit | 14-bit data | G | OR  bit | 14-bit data |
| .. | | | | | | |
| 0x7fffc | U | OR  bit | 14-bit data | G | OR  bit | 14-bit data |

| Shorthand | Explanation |
|---|---|
| U | status of user bit if enabled, 0 otherwise |
| OR | out of range, set with over or underflow, 0 otherwise |
| G | set on the first sample in "Gate Chaining Mode", 0 otherwise |

### 4.34 Bank 2 memory  (0x600000 – 0x7ffffc)

```
#define SIS3300_MEMBASE_BANK2_ADC12              0x600000
#define SIS3300_MEMBASE_BANK2_ADC34              0x680000
#define SIS3300_MEMBASE_BANK2_ADC56              0x700000
#define SIS3300_MEMBASE_BANK2_ADC78              0x780000
```
Bank 2 memory is installed to allow for parallel readout from one memory bank, while the other memory bank is acquiring data. The second memory bank has the same structure as bank 1.

# 5   Description of Start/Stop and Gate operation modi

## 5.1   Start/stop mode

Different start and stop conditions can be used in combination with start/stop mode (as illustrated in the start and stop logic summaries.

**Note:** [*] LEMO output 2 (ready for stop) reflects the phase in which the digitizer is sampling, unless the signal was assigned to reflect the bank full pulse (by setting bit 9 of the control register)
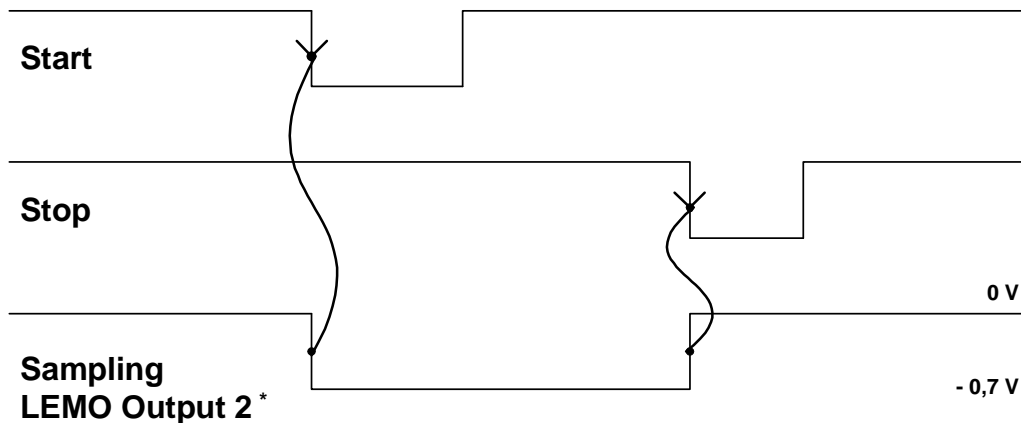


### 5.1.1   Front panel start/stop

One option to use start stop/mode is with NIM front panel start and stop signals. The width of the start and stop pulse has to exceed 2 sampling clocks. Following steps are part of the setup in this case.

- enable front panel start/stop logic (by setting bit 8 of acquisition control register)
- connect start to LEMO input 3
- connect stop to LEMO input 2

## 5.2   Gate mode

A single external signal is used to define sampling start and stop. The start signal (i.e. LEMO input 3) is used as gate input in this mode. The leading edge of the signal defines the start, the stop condition is given by the trailing edge as illustrated below. The width of the gate has to exceed 2 sample clocks.
Following steps are required to activate gate mode

- enable front panel start/stop logic (set bit 8 of acquisition control register)
- enable front panel gate mode (set bit 10 of acquisition control register)
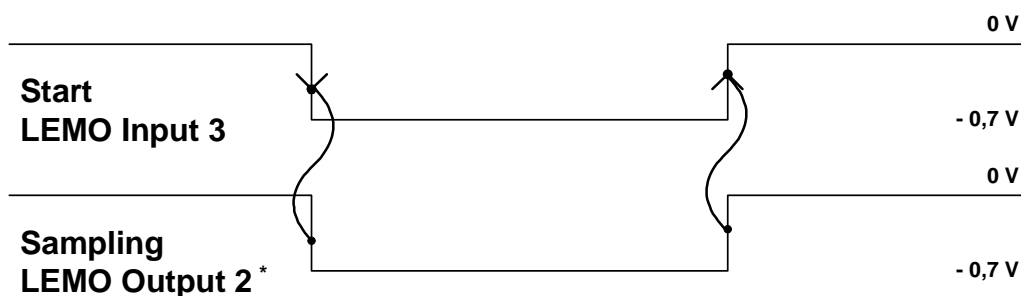
**Note:** [*] LEMO output 2 (ready for stop) reflects the phase in which the digitizer is sampling, unless the signal was assigned to reflect the bank full pulse (by setting bit 9 of the control register)

## 5.3 Start logic summary

The diagram below illustrates the implemented start conditions of the SIS3300/1,
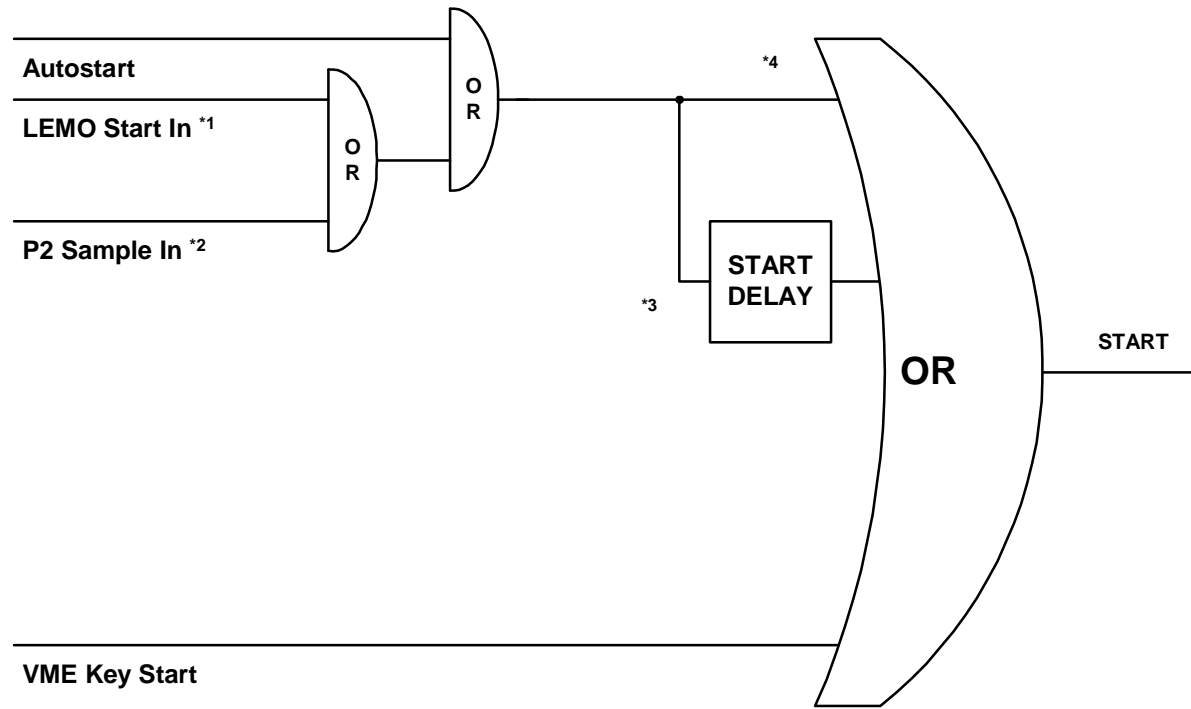


| Note | Condition | Register | Comment |
|------|-----------|----------|---------|
| *1 | `Bit 8 = 1` | Acquisition Control | Enable front panel start/stop logic |
| *2 | `Bit 9 = 1` | Acquisition Control | Enable P2 start/stop logic |
| *3 | `Bit 6 = 1` | Acquisition Control | Start delay enable |
| *4 | `Bit 6 = 0` | Acquisition Control | No start delay |

## 5.4  Stop logic summary

The diagram below illustrates the implemented stop conditions of the SIS3300/1,
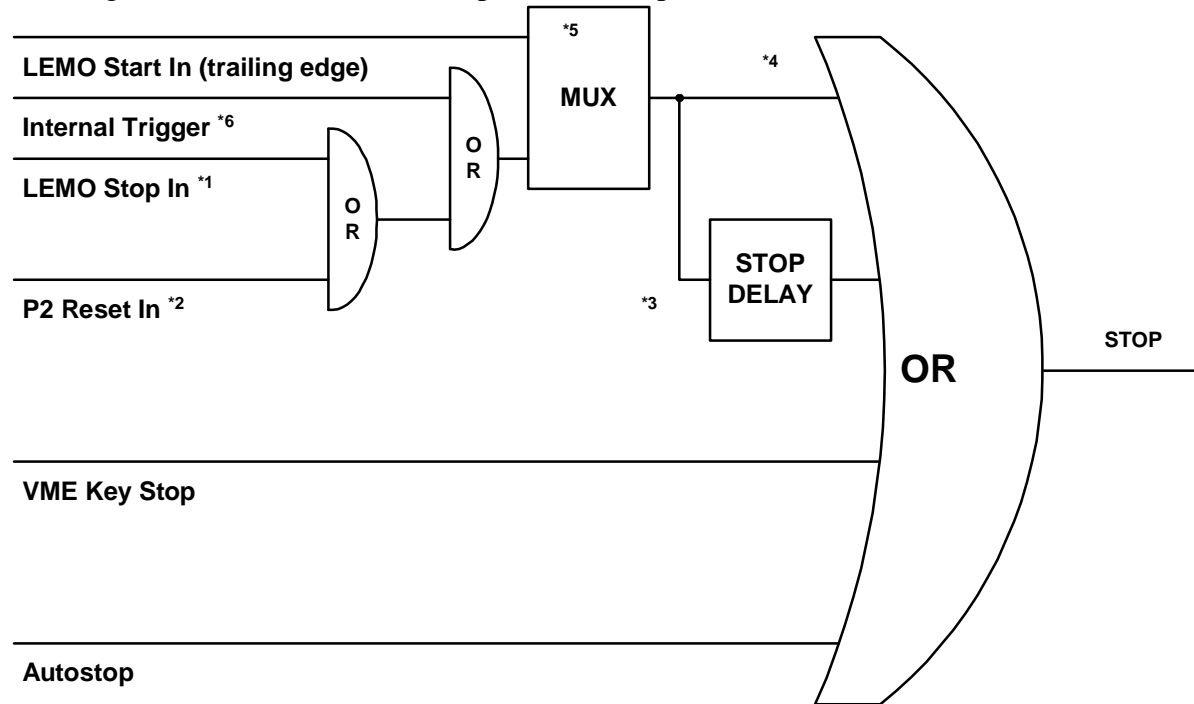


| Note | Condition | Register | Comment |
|------|-----------|----------|---------|
| *1 | `Bit  8 = 1` | Acquisition Control | Enable front panel start/stop logic |
| *2 | `Bit  9 = 1` | Acquisition Control | Enable P2 start/stop logic |
| *3 | `Bit  7 = 1` | Acquisition Control | Stop delay enable |
| *4 | `Bit  7 = 0` | Acquisition Control | No stop delay |
| *5 | `Bit 10 = 0`<br>`Bit 10 = 1` | Acquisition Control | use start/stop mode<br>use gate mode |
| *6 | `Bit  6 = 1` | Control | Route trigger |

## 6   Special Compress Event Readout Logic

The Compress Event Readout logic enables a vme compressed readout of one ADC Event inside a programmed wrap page.
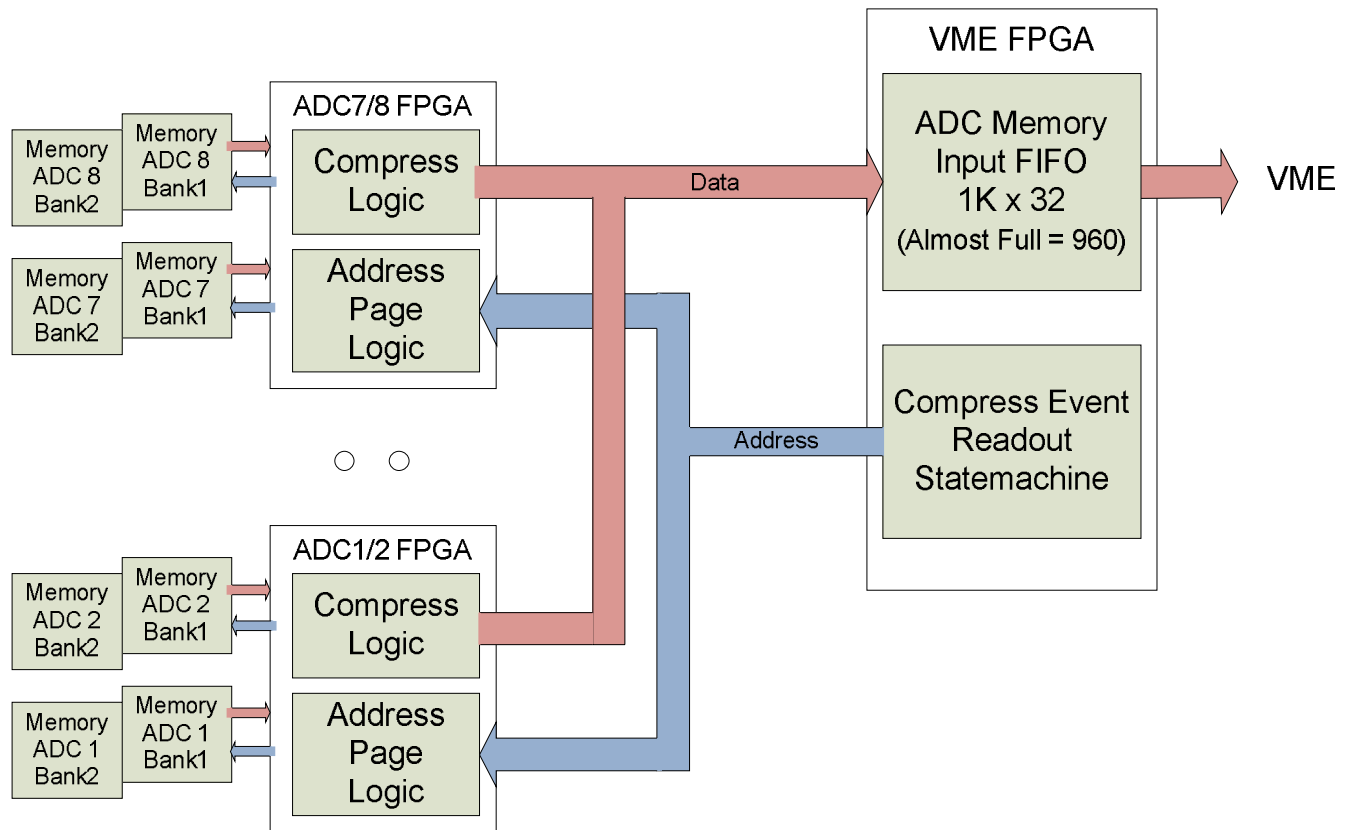
The following register and fifo addresses are implemented to control the logic and readout the data via VME:

- Start Compress Event Readout register (R/W).
- Abort/Stop Compress Event Readout register (W).
- Compress Event Readout Status register (R)
- Compress Event Readout Configuration register (R/W)
- ADC Memory Input Fifo (R)

```
                    ┌──────┐
                    │ idle │
                    └──────┘
                        │
                        │  Write to „Start Compress Event Readout""
                        ▼
        ┌───────────────────────────────┐
        │   Selected ADC FPGA writes     │
        │   compressed data to ADC       │
        │   Memory Input Fifo if the     │
        │   Input Fifo is NOT Almost     │
        │   Full                         │
        │                                │
        │        BUSY Flag = 1           │
        └───────────────────────────────┘
                        │
                        │   Requested number of data are written
                        │                  or
                        │   Write to „Abort Compress Event Readout""
                        ▼
                    ┌──────┐
                    │ idle │
                    └──────┘
```
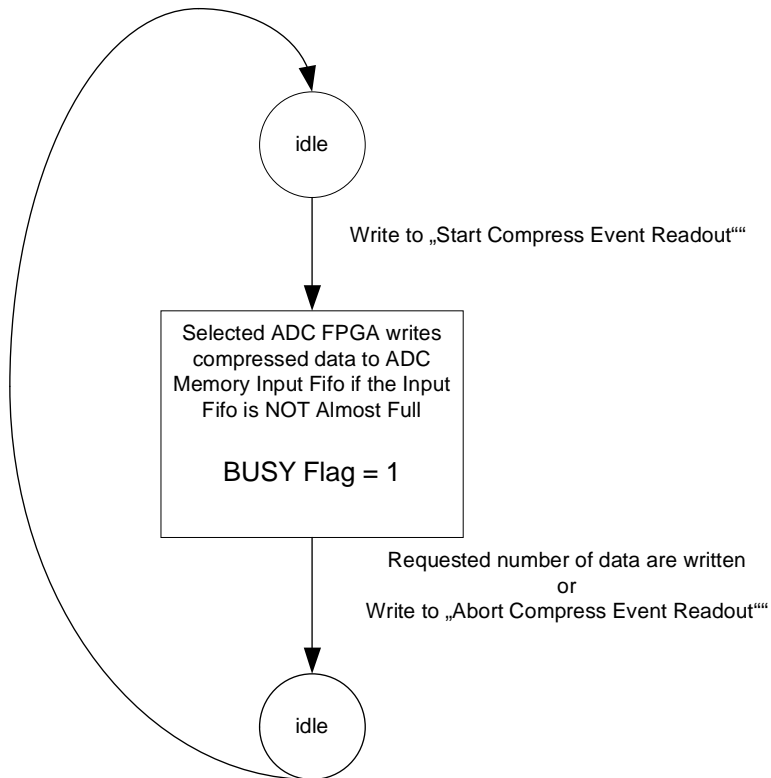
If the Compress Event Readout statemachine is busy then it is not possible/allowed to access (read or write) the ADC FPGAs !

## 6.1 Compress Event Readout register discription

### 6.1.1 Start Compress Event Readout register (0x50, read/write)

```
#define SIS3301_EVENT_READOUT_START_CMD      0x50   /* rd/wr; D32 */
```

A write to this register will start the "Compress Event Readout" statemachine. If bit 32 is set then the Input Fifo is cleared at the beginning.
The "Compress Event Readout" statemachine reads the ADC Memory from the written start address and pushes the requested number of data to the ADC Memory Input Fifo. The ADC Memory address will be increment inside the programmed wrap page. If the Input Fifo is almost full then logic waits until the fifo is read.

| Bit | |
|-----|---|
| 31 | "1" : Reset ADC Memory Input FIFO at the beginning |
| 30 | |
| ... | |
| ... | |
| 20 | Start Address: Bank Select |
| 19 | Start Address: ADC Select bit 2 |
| 18 | Start Address: ADC Select bit 1 |
| 17 | Start Address: ADC Select bit 0 |
| 16 | Start Address: ADC Memory address bit 16 |
| 15 | Start Address: ADC Memory address bit 15 |
| .. | |
| .. | |
| 0 | Start Address: ADC Memory address bit 0 |

The power up default value is 0

### 6.1.2 Stop/Abort Compress Event Readout register (0x54, write)

```
#define SIS3301_EVENT_READOUT_ABORT_CMD      0x54   /* write; D32 */
```

A write to this register stops/aborts the Compress Event Readout Statemachine.

### 6.1.3 Compress Event Readout Status register (0x54, read)

```
#define SIS3301_EVENT_READOUT_STATUS          0x54   /* read; D32 */
```

| Bit | |
|-----|---|
| 31 | Compress Event Readout Statemachine Busy Flag |
| 30 | 0 |
| ... | |
| 26 | 0 |
| 25 | Input fifo write pointer bit 9 |
| ... | |
| 16 | Input fifo write pointer bit 0 |
| 15 | 0 |
| .. | |
| 10 | 0 |
| 9 | Input fifo read pointer bit 9 |
| .. | |
| 0 | Input fifo read pointer bit 0 |

### 6.1.4  Compress Event Readout configuration register (0x100020, 0x200020, 0x280020, 0x300020, 0x380020)

```
#define SIS3301_EVENT_READOUT_CONFIG_ALL_ADC 0x100020  /* write only;D32 */


#define SIS3301_EVENT_READOUT_CONFIG_ADC12   0x200020  /* read/write;D32 */
#define SIS3301_EVENT_READOUT_CONFIG_ADC34   0x280020  /* read/write;D32 */
#define SIS3301_EVENT_READOUT_CONFIG_ADC56   0x300020  /* read/write;D32 */
#define SIS3301_EVENT_READOUT_CONFIG_ADC78   0x380020  /* read/write;D32 */
```

This register is implemented for each channel group.

| Bit | Function | Default |
|-----|----------|---------|
| 31 | Unused; read 0 | 0 |
| .. | .. | |
| 20 | Unused; read 0 | 0 |
| 19 | Reserved | |
| 18 | Event Readout compress factor bit 2 | |
| 17 | Event Readout compress factor bit 1 | |
| 16 | Event Readout compress factor bit 0 | 0 |
| 15 | Event Readout length bit 15 (MSB) | 0 |
| .. | .. | |
| 0 | Event Readout length bit 0 (LSB) | 0 |

The power up default value reads 0x 00000000

**Event Readout compress factor:**

| compress factor bit 2 | compress factor bit 1 | compress factor bit 0 | Sum over samples | Shift right factor |
|-----------------------|-----------------------|-----------------------|------------------|--------------------|
| 0 | 0 | 0 | 1 (no sum) | 0 (no shift) , 14 bit result |
| 0 | 0 | 1 | 2 | 0 (no shift), 15 bit result |
| 0 | 1 | 0 | 4 | 0 (no shift), 16 bit result |
| 0 | 1 | 1 | 8 | 1, 16 bit result |
| 1 | 0 | 0 | 16 | 2, 16 bit result |
| 1 | 0 | 1 | 32 | 3, 16 bit result |
| 1 | 1 | 0 | 64 | 4, 16 bit result |
| 1 | 1 | 1 | 64 | 4, 16 bit result |

Overflow/Underflow:
If one sample of the samples of the sum has an overflow or an underflow condition the sum will be set to 0xffff or 0x0.

**Event Readout length:**

| Event Readout Length | Number of 32-bit words | Number of compressed 16-bit words |
|----------------------|------------------------|-----------------------------------|
| 0 | 1 | 2 |
| 1 | 2 | 4 |
| 2 | 3 | 6 |
| . | . | |
| 65535 | 65536 | 2x65536 (128k samples) |

## 6.2   Compress Event Readout  Fifo  (0x180000 – 0x18fffc)

```
#define SIS3301_EVENT_READOUT_FIFO              0x180000
/* read D32, BLT32, MBL64, 2eVME; size: 0x10000 */
```

Data format:

| D31 :16 | D15:0 |
|---------|-------|
| second sum | first sum |

## 6.3   Example

```
// set compress factor and auto-readout length
     data = (i_compress_factor << 16) + readout_length_lwords - 1 ; //
     addr = base_addr + SIS3301_EVENT_READOUT_CONFIG_ALL_ADC ;
     vme_A32D32_write(&sis1100_device1, addr, data) ;



// Start FSM Readout
     data =     0x80000000           // reset input Fifo
            + (0x0 << 20)            // bank
            + (0x0 << 17)            // ADC select
            + (memory_start_index & 0x1ffff) ;         // memory address
     addr = base_addr + SIS3301_EVENT_READOUT_START_CMD ;
     vme_A32D32_write(sis1100_device, addr, data) ;



// special readout
     addr = base_addr + SIS3301_EVENT_READOUT_FIFO ;
     return_code =   vme_A32MBLT64_read(sis1100_device, addr, rblt_data,
                                   readout_length_lwords, &get_lwords) ;
```

**Data in ADC Memory with normal readout**

```
address         +0x0       +0x4       +0x8       +0xC
33400000     1000200    1010201    1020202    1030203
33400010     1040204    1050205    1060206    1070207
33400020     1080208    1090209    10a020a    10b020b
33400030     10c020c    10d020d    10e020e    10f020f
33400040     1100210    1110211    1120212    1130213
33400050     1140214    1150215    1160216    1170217
33400060     1180218    1190219    11a021a    11b021b
33400070     11c021c    11d021d    11e021e    11f021f
33400080     1200220    1210221    1220222    1230223
33400090     1240224    1250225    1260226    1270227
334000a0     1280228    1290229    12a022a    12b022b
334000b0     12c022c    12d022d    12e022e    12f022f
334000c0     1300230    1310231    1320232    1330233
334000d0     1340234    1350235    1360236    1370237
334000e0     1380238    1390239    13a023a    13b023b
334000f0     13c023c    13d023d    13e023e    13f023f
```

**Data with Compress Event readout**
Start Address = 0x0
Compress Factor = 0x0
Event Readout Length = 0xff

| address | +0x0 | +0x4 | +0x8 | +0xC |
|---|---|---|---|---|
| 33180000 | 1010100 | 1030102 | 1050104 | 1070106 |
| 33180010 | 1090108 | 10b010a | 10d010c | 10f010e |
| 33180020 | 1110110 | 1130112 | 1150114 | 1170116 |
| 33180030 | 1190118 | 11b011a | 11d011c | 11f011e |
| 33180040 | 1210120 | 1230122 | 1250124 | 1270126 |
| 33180050 | 1290128 | 12b012a | 12d012c | 12f012e |
| 33180060 | 1310130 | 1330132 | 1350134 | 1370136 |
| 33180070 | 1390138 | 13b013a | 13d013c | 13f013e |
| 33180080 | 1410140 | 1430142 | 1450144 | 1470146 |
| 33180090 | 1490148 | 14b014a | 14d014c | 14f014e |
| 331800a0 | 1510150 | 1530152 | 1550154 | 1570156 |
| 331800b0 | 1590158 | 15b015a | 15d015c | 15f015e |
| 331800c0 | 1610160 | 1630162 | 1650164 | 1670166 |
| 331800d0 | 1690168 | 16b016a | 16d016c | 16f016e |
| 331800e0 | 1710170 | 1730172 | 1750174 | 1770176 |
| 331800f0 | 1790178 | 17b017a | 17d017c | 17f017e |

**Data with Compress Event readout**
Start Address = 0x0
Compress Factor = 0x1
Event Readout Length = 0x0f

| address | +0x0 | +0x4 | +0x8 | +0xC |
|---|---|---|---|---|
| 33180000 | 2050201 | 20d0209 | 2150211 | 21d0219 |
| 33180010 | 2250221 | 22d0229 | 2350231 | 23d0239 |
| 33180020 | 2450241 | 24d0249 | 2550251 | 25d0259 |
| 33180030 | 2650261 | 26d0269 | 2750271 | 27d0279 |

**Data with Compress Event readout**
Start Address = 0x4
Compress Factor = 0x1
Event Readout Length = 0x0f

| address | +0x0 | +0x4 | +0x8 | +0xC |
|---|---|---|---|---|
| 33180000 | 20d0209 | 2150211 | 21d0219 | 2250221 |
| 33180010 | 22d0229 | 2350231 | 23d0239 | 2450241 |
| 33180020 | 24d0249 | 2550251 | 25d0259 | 2650261 |
| 33180030 | 26d0269 | 2750271 | 27d0279 | 2850281 |

# 7  Operation

## 7.1  Configuration:

- Issue key reset

- define in Interrupt configuration register
  - VME IRQ Level and Vector
  - type of IRQ requester

- define in Interrupt control register
  - enable IRQ source

- define in Acquistion register
  - Set Clock source
  - Set Start/Stop or Gate mode
  - Enable/Disable P2 External Start/Stop
  - Enable/Disable LEMO  External Start/Stop
  - Enable/Disable External Stop Delay
  - Enable/Disable External Start Delay
  - Set Single or Multi Event Mode
  - if Multi Event then enable/disable Autostart

- define in Event configuration register
  - Enable/Disable Autostop at end address of Page
  - Set Page size

## 7.2  Arm for sampling:

- define in Acquistion register
  - Enable Sample Clock for Memory Bank1 or Bank2

## 7.3  Start Sampling:

- in Single Event mode
  - Issue key Start or External Start

- in Multi Event mode with Autostart disabled
  - Issue key Start or External Start for **each** Event

- in Multi Event mode with Autostart enabled
  - Issue key Start or External Start for the **first** Event only

Note: activation of auto bank switch mode with multi event mode enabled will start sampling automatically

## 7.4   Stop Sampling (Event):

- in Single Event mode with Autostop enabled
  - sampling stops automatically at the end address of the page

- in Single Event mode with Autostop is disabled (Wrap around mode)
  - Issue key Stop or External Stop

- in Multi Event mode with Autostop is enabled
  - sampling stops automatically at the end address of each page

- in Multi Event mode with Autostop is disabled (Wrap around mode)
  - Issue key Stop or External Stop for each Event

## 7.5   End of Sampling (clear arm / disable Sample Clock):

- in single event mode
  the "Sample Clock Enable " bit of the sampling bank is cleared by the logic at the end of sampling (one event)

- in multi event mode
  the "Sample Clock Enable " bit of the sampling bank is cleared by the logic at the end of sampling (last event)

The user software can poll on the status of the sample clock enable bit in the acquisition control register or use the end of event or bank full interrupt conditions.

# 8 Board layout

A printout of the silk screen of the component side of the PCB is shown below.
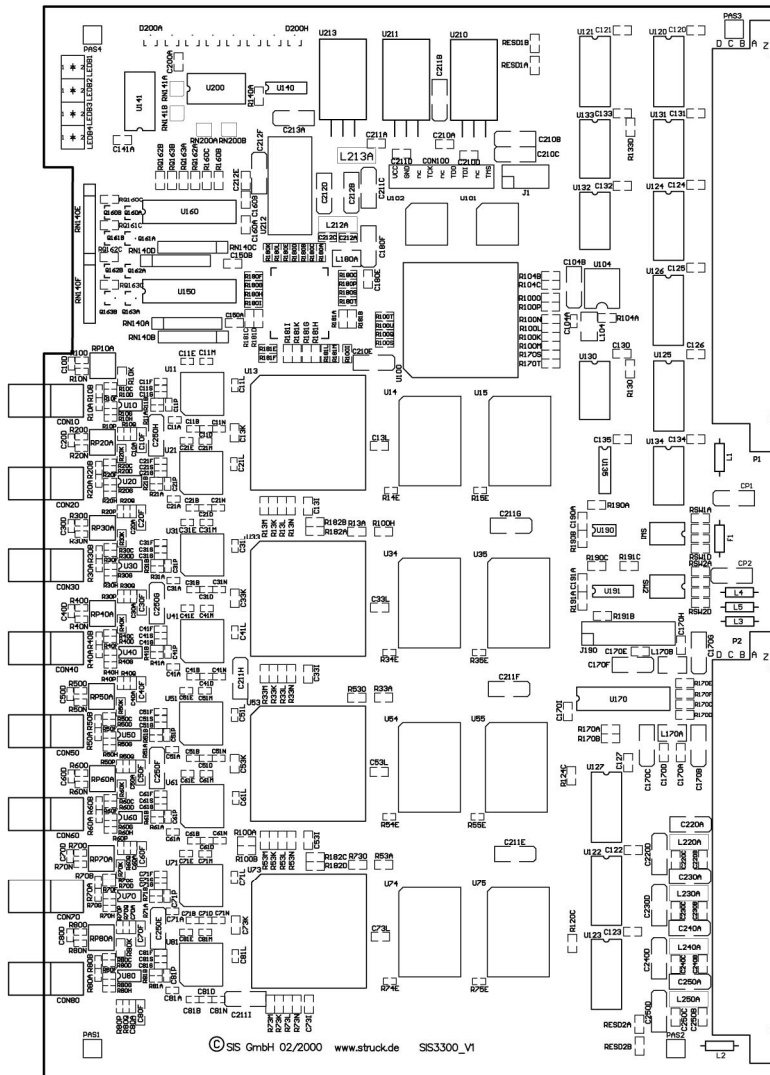
## 9   Front panel

The SIS3300 is a single width (4TE) 6U VME module. A sketch of the front panel (without handles) is show below.
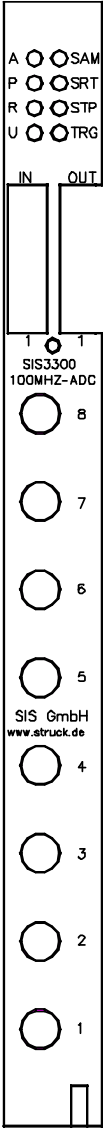
### 9.1   Control In/Outputs

The control I/O section features 8 LEMO00 connectors with NIM levels.

| Designation | Inputs | Outputs | Designation |
|---|---|---|---|
| 4 | Clock In | Clock Out | 4 |
| 3 | Start | Ready for Start/bank full output | 3 |
| 2 | Stop | Ready for Stop/bank full output | 2 |
| 1 | User in | User out/trigger/Multiplexer  Strobe/bank full output | 1 |

The ready for start and ready for stop outputs can be used to interfere with external deadtime logic. Ready for start will become active as soon as the sample clock for one of the banks is active. Ready for stop will go active as soon as the start signal was seen by the module.

The external clock must be a symmetric signal unless the module is operated in external random clock mode
The width of an external start/stop pulse must be greater or equal two sampling clock periods.

### 9.1.1   User input

User input functionality was implemented to allow for synchronous recording of one external status bit (like chopper on/off e.g.) with the ADC data stream. The user bin information is recorded with the ADC data (see section 4.33). The current status of the logic level is represented by Bit 16 of the status register.

### 9.1.2   Control input termination

The control inputs are configured for 50 Ω termination (i.e. with 47 Ω) by default.
Each input is terminated with a resistor network (5 pins, 4 resistors, common pin to socket pin 6) to ground, the names of the input sockets are listed in the table below.

| Designation | Inputs | Resistor Network |
|---|---|---|
| 4 | Clock In | RN140A |
| 3 | Start | RN140B |
| 2 | Stop | RN140C |
| 1 | User in | RN140D |

### 9.2   Analog inputs

### 9.2.1   Single ended LEMO version

The analog inputs of the single ended version are terminated with 50 Ω. The input range of the initial series is 5V, it is shifted with the offset adjustment potentiometer to match the required user input voltage range of 0 ... –5V or +2.5 V ... –2.5V.

### 9.2.2   Differential version

The differential input version will be based on another printed circuit design, input termination and availbale input ranges are yet to be defined.

## 9.3 LED's

The SIS3300 has 8 front panel LEDs to visualise part of the modules status. The user (and access) LED are a good way to check first time communication/addressing with the module.

| Color | Designator | Function |
|---|---|---|
| Red | A | Access to SIS3300 VME slave port |
| Yellow | P | Power |
| Green | R | Ready, on board logic configured |
| Green | U | User, to be set/cleared under program control |
| Red | SAM | Sampling, |
| Yellow | SRT | Start, lit with start input (or leading edge in gate mode) |
| Green | STP | Stop, lit with stop input (or trailing edge in gate mode) |
| Green | TRG | Trigger, lit if one or more channels are above threshold |

The on duration of the access, sampling, start, stop and trigger LEDs is stretched to guarantee visibility even under low rate conditions.

## 9.4 PCB LEDs

The 8 surface mounted red LEDs D200A to D200H on the top left corner of the component side of the SIS3300 are routed to the control FPGA, their use may depend on the firmware design.

# 10  Jumpers/Configuration

## 10.1  J1
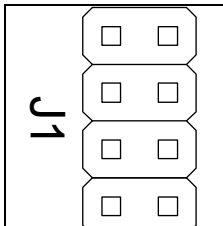
The function of J1 depends on the PCB (printed circuit board) revision level. The board revision level is printed in white on the lower edge of the card on the component side as a text of the form SIS3300_V1 e.g.

### 10.1.1 SIS3300_V1

Selection of bits 31-28 of the 32-bit A32 address (see. base address section)
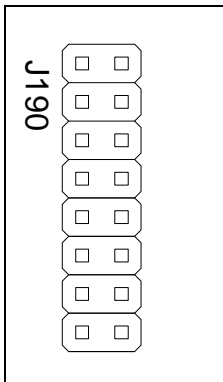
### 10.1.2 SIS3300_V2 (and higher)

The SIS3300 supports several addressing modes, the actual mode is selected by jumper array J1. The given mode is selected if its corresponding jumper is in place. The four jumper positions are described in the table below. The A32 jumper is closest to the modules front panel.

| Jumper | Function | Factory default |
|---|---|---|
| A32 | enable A32 addressing | closed |
| GEO | enable geographical addressing | open |
| VIPA | not implemented yet | open |
| reserved | reserved | open |

## 10.2  J190 Reset

Jumper 5 of jumper array J190 defines the reset behaviour of the SIS3300 upon VME Sysreset. If the jumper is closed the module will be reset with VME Sysreset. The other fields of the array are unused in the current firmware design.

| Jumper | Function | Factory default |
|---|---|---|
| 1 | unused | open |
| 2 | enable watchdog | closed |
| 3 | unused | open |
| 4 | unused | open |
| 5 | unused | open |
| 6 | Connect module reset to VME_Sysreset | closed |
| 7 | unused | open |
| 8 | unused | open |

The enable watchdog jumper has to be removed during the initial JTAG firmware load.

## 10.3 Offset adjustment

The pedestal or offset of the ADC channels can be adjusted with the potentiometers RP10A through RP80A (see table below). The sensitivity for the positive or negative offset can be reduced by two limit jumpers (2 mm), the full range is available with both jumpers open. Do not install both jumpers for a channel in parallel.

| channel | limit pos. offset | limit neg. offset | Offset-Potentiometer |
|---------|-------------------|-------------------|----------------------|
| 1 | JP78 | JP79 | RP80A |
| 2 | JP76 | JP77 | RP70A |
| 3 | JP58 | JP59 | RP60A |
| 4 | JP56 | JP57 | RP50A |
| 5 | JP38 | JP39 | RP40A |
| 6 | JP36 | JP37 | RP30A |
| 7 | JP18 | JP19 | RP20A |
| 8 | JP16 | JP17 | RP10A |

The position of the two jumpers JP78 and JP79 close to potentiometer RP80A for ADC channel 1 is illustrated in the portion of the board shown below. The displayed area is the vicinity of the channel 1 LEMO input connector (CON80).
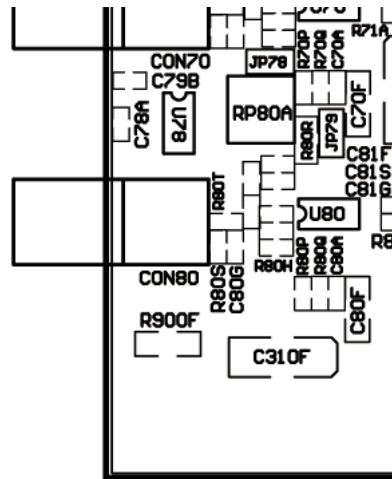
## 10.4 JTAG

The SIS3300 on board logic can load its firmware either from two serial PROMs or via the JTAG port on connector CON100. A list of firmware designs can be found under http://www.struck.de/sis3300firm.htm.

Hardware like the XILINX HW-JTAG-PC in connection with the appropriate software will be required for in field JTAG firmware upgrades.

The JTAG connector is a 9 pin single row 1/10 inch header, the pin assignment on the connector can be found in the table below.

| Pin | Short hand | Description |
| --- | --- | --- |
| 1 | VCC | Supply voltage |
| 2 | GND | Ground |
| 3 | nc | not connected, cut to avoid polarity mismatch |
| 4 | TCK | test clock |
| 5 | nc | not connected |
| 6 | TDO | test data out |
| 7 | TDI | test data in |
| 8 | nc | not connected |
| 9 | TMS | test modus |

# 11  Appendix

## 11.1  Data acquisition modes

### 11.1.1 Random external clock mode

Random external clock mode is activated by writing 0x800 to the acquisition control register .

### 11.1.2 Auto bank switch mode

Auto bank switch mode was introduced for efficient use of the two memory banks on acquisition . The mode is activated by issuing a KEY_START_AUTO_BANK_SWITCH after the feature was activated by setting bit 2 in the acquisition control register. The bank full flags (B1_FULL and B2_FULL)  are cleared with the KEY, at the same time a first start is generated if AUTOSTART is enabled also. Data will be acquired into memory bank 1 until the bank is full. At this point the flag B1_FULL will be set and acquisition changes over to bank 2 (if the flag B2_FULL is not set). The user can read out data from bank 1 in parallel to ongoing acquisition into bank 2 and clear the B1_FULL flag after the readout was completed. As soon as memory bank 2 is filled acquisition will be handed over to bank 1 again if B1_FULL has been cleared already.
The active memory bank will acquire data until the bank is filled if a KEY-STOP_AUTO_BANK_SWITCH is issued.

### 11.2 consumption

The SIS3300/1 is a single supply design to facilitate operation in any VME environment, i.e. the module does not require special backplanes or non standard VME voltages.
The power consumption of a two memory bank module digitizing at 100 MHz was measured to be:

| Voltage | Current |
|---------|-----------|
| + 5V | < 6A |
| +12 V | < 40 mA |
| - 12 V | < 60 mA |
| P < 32 W | |

### 11.3 Operating conditions

#### 11.3.1 Cooling

Although the SIS3300/1 is mainly a 2.5 and 3.3 V low power design, substantial power is consumed by the Analog to Digital converter chips and linear regulators. Hence forced air flow is required for the operation of the board. The board may be operated in a non condensing environment at an ambient temperature between 10° and 40° Celsius. A power up warm up time of some 10 minutes is recommended to ensure equilibrium on board temperature conditions.

#### 11.3.2 Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default. The SIS3300 is configured for hot swap in conjunction with a VME64x backplane. In non VME64x backplane environments the crate has to be powered down for module insertion and removal.

## 11.4 Connector types

The VME connectors and the two different types of front panel connectors used on the SIS3300 are:

| Connector | Purpose | Part Number |
|---|---|---|
| 160 pin zabcd | VME P1/P2 | Harting 02 01 160 2101 |
| LEMO PCB | Coax. control connector | LEMO EPB.00.250.NTN |
| 90$^o$ PCB LEMO | Analog input connector | LEMO EPL.00.250.NTN |
| 90$^o$ PCB LEMO | Analog input connector (3301 differential input version) | LEMO EPG.00.302.NLN |

## 11.5 P2 row A/C pin assignments

The P2 connector of the SIS3300 has several connections on rows A and C for the F1002 compatible use at the DESY H1 FNC subdetector. This implies, that the module can not be operated in a VME slot with a special A/C backplane, like VSB e.g.. The pin assignments of P2 rows A/C of the SIS3300 is shown below:

| P2A | Function | P2C | Function |
|---|---|---|---|
| 1 | -5.2 V | 1 | -5.2 V |
| 2 | -5.2 V | 2 | -5.2 V |
| 3 | -5.2 V | 3 | -5.2 V |
| 4 | not connected | 4 | not connected |
| 5 | not connected | 5 | not connected |
| 6 | DGND | 6 | DGND |
| 7 | P2_CLOCK_H | 7 | P2_CLOCK_L |
| 8 | DGND | 8 | DGND |
| 9 | P2_START_H | 9 | P2_START_L |
| 10 | P2_STOP_H | 10 | P2_STOP_L |
| 11 | P2_TEST_H | 11 | P2_TEST_L |
| 12 | DGND | 12 | DGND |
| 13 | DGND | 13 | DGND |
| 14 | DGND | 14 | DGND |
| 15 | DGND | 15 | DGND |
| 16 | not connected | 16 | not connected |
| ... | ... | 17 | ... |
| 31 | not connected | 18 | not connected |

## 11.6 Row d and z Pin Assignments

The SIS3300 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing (PCB revisions V2 and higher) and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

| Position | P1/J1 | | P2/J2 | |
|---|---|---|---|---|
| | Row z | Row d | Row z | Row d |
| 1 | | VPC (1) | | |
| 2 | GND | GND (1) | GND | |
| 3 | | | | |
| 4 | GND | | GND | |
| 5 | | | | |
| 6 | GND | | GND | |
| 7 | | | | |
| 8 | GND | | GND | |
| 9 | | GAP* | | |
| 10 | GND | GA0* | GND | |
| 11 | RESP* | GA1* | | |
| 12 | GND | | GND | |
| 13 | | GA2* | | |
| 14 | GND | | GND | |
| 15 | | GA3* | | |
| 16 | GND | | GND | |
| 17 | | GA4* | | |
| 18 | GND | | GND | |
| 19 | | | | |
| 20 | GND | | GND | |
| 21 | | | | |
| 22 | GND | | GND | |
| 23 | | | | |
| 24 | GND | | GND | |
| 25 | | | | |
| 26 | GND | | GND | |
| 27 | | | | |
| 28 | GND | | GND | |
| 29 | | | | |
| 30 | GND | | GND | |
| 31 | | GND (1) | | GND (1) |
| 32 | GND | VPC (1) | GND | VPC (1) |

**Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.**

# 12 Index