A Cherenkov Camera with Integrated Electronics based on the "Smart Pixel" Concept

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Abstract.
An option for the cameras of the HESS telescopes, the concept of a modular camera based on "Smart Pixels" was developed. A Smart Pixel contains the photomultiplier, the high voltage supply for the photomultiplier, a dual-gain sample-and-hold circuit with a 14 bit dynamic range, a time-to-voltage converter, a trigger discriminator, trigger logic to detect a coincidence of X=1...7 neighboring pixels, and an analog ratemeter. The Smart Pixels plug into a common backplane which provides power, communicates trigger signals between neighboring pixels, and holds a digital control bus as well as an analog bus for multiplexed readout of pixel signals. The performance of the Smart Pixels has been studied using a 19-pixel test camera.

INTRODUCTION

HESS is a next-generation array of imaging atmospheric Cherenkov telescopes (IACTs) to be built in the Southern Hemisphere in the Khomas Highland of Namibia. Details of the HESS project are given elsewhere in these proceedings (see Hofmann et al.). In its final stage, the HESS experiment should consist of 16 telescopes each with a $\sim$100 m^2 reflector and a high-resolution camera in the focal plane. The camera initially contains $\sim$700 photomultiplier pixels each viewing 0.16° of the sky (4.3° field-of-view), with a subsequent expansion to $\sim$850 photomultiplier pixels (5° field-of-view). The schedule foresees to start with scientific operation of the first 4-telescope subsystem in 2002 (Phase 1). The energy threshold of about 40 GeV, the angular resolution of less than a few arc minutes and the flux sensitivity of the full system above 100 GeV of a few 10^{-12} ph cm^{-2} s^{-1} should allow the observation of a significant number of objects and new source populations at GeV-TeV energies.

THE SMART PIXEL DESIGN

The Smart Pixel design was driven by the desire to

- Achieve a low energy threshold and good spectroscopic measurements by providing the shortest possible path for fast signals in order to allow short gate times, thereby minimizing night sky background noise and uncertainties due to timing jitter along the signal path.
- Use a highly modular design with multiple slow control and monitoring information, which allows the simple test and exchange of modules as well as a fast identification of faulty modules.
- Avoid a large number of long cables routing fast signals from the camera to an electronics unit at the base of the telescope.

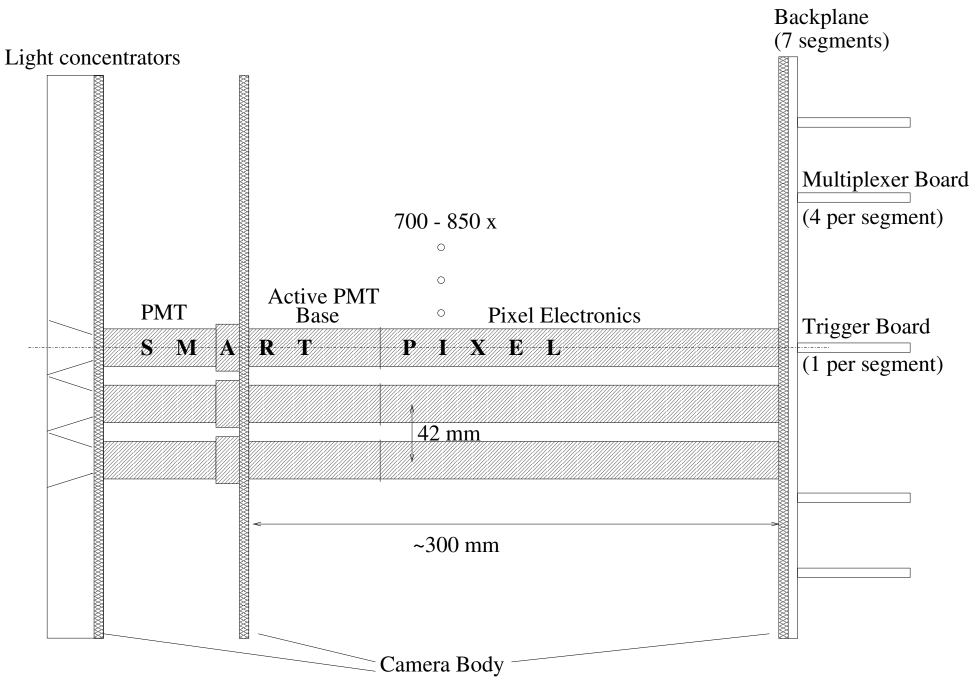

FIGURE 1. The layout of the Smart Pixel camera.

The Smart Pixel design incorporates analog signal processing electronics, the trigger, and slow control electronics in the camera (see Figure 1). A Smart Pixel contains the photomultiplier (PMT), the high voltage supply for the PMT, a dual-gain sample-and-hold circuit, a trigger discriminator, trigger logic to detect a coincidence of X=1…7 neighboring pixels, a time-to-voltage converter for trigger timing, an I/V-converter for the PMT current, and an analog ratemeter. The Smart Pixels plug into a common backplane which provides power, communicates trigger signals between neighboring pixels, and holds a digital control bus as well as an analog bus for the multiplexed readout of the pixel signals. Multiplexer boards (1 per 32 pixels) for the multiplexing of the analog signals and trigger boards (1 per 127 pixels) for the dispatching of the trigger signal plug into the backside of the backplane.

The analog multiplexed outputs of each pixel include the PMT high- and low-gain outputs of the sample-and-hold, the PMT DC current, the mean trigger rate, two temperatures, supply and reference voltages, and the HV voltage and current signals. With the digital bus, it is possible in each pixel to set the multiplexer, the width and delay of the dual-gain sample-and-hold gate, the pedestal offsets, the X of the X/7 trigger, the range of the analog ratemeter, and the HV. Further functions include the enabling / disabling of the trigger and the HV as well as a global reset.

The camera is triggered if a X/7 $> q_0$ photoelectrons condition is met (X=1...7). The discriminator output of each pixel is fed into the microcontrollers of the pixel itself and the six neighboring pixels. The X/7 trigger fires if the discriminator output of the pixel itself and (X-1) of the six neighbor signals overlap. The entire camera is divided into seven segments with 100 to 127 pixels each, and for each segment the X/7 output signals of the pixels are ORed on a trigger board, dispatched to the trigger boards of the other segments, and then fanned out to all pixels. The time for the camera trigger formation is $\sim$55 ns. The analog signal is delayed for this time with a thin coaxial cable bundled into each pixel, and then stored in the sample-and-hold. The trigger signal is also sent to the central station to form the global, multi-telescope coincidence trigger. If a camera trigger is not followed by a global trigger, the camera is reset after 2 μs, i.e., the sample-and-hold is cleared and the discriminator output is enabled.

Only about 50 cables are needed between the camera and a local electronics station. These include $\sim$30 multiplexed analog outputs, one per group of 32 pixels, the digital bus lines, the camera trigger output, the global trigger input, an analog reset for the case that a camera trigger is not followed by a global trigger, a test input and a digital reset.

The camera readout is as follows: the pixel multiplexer of all pixels is set to the first value (the high-gain PMT signal). All multiplexers on the multiplexer boards (1 per 32 pixels) are then successively set to pixels 1,2,...,32. The pixel multiplexers of all pixels are then set to the second value, etc. With a readout frequency of 5 MHz, it takes 6.4 μs to read out a single analog value for all pixels. Typically, for each event one would read out the low- and high-gain PMT signal and the time-to-amplitude converter (TAC) giving the trigger timing. Thus, the readout time is $\sim$20 μs. Assuming one ADC per 32 pixels, after readout the data are arranged in the ADC memory with words 0 to 31 as the high gain of 32 pixels, words 32 to 63 as the low gain of 32 pixels, words 64 to 95 as the TAC values of 32 pixels, and optional monitoring information following, if requested. Besides the event readout, the slow control and monitoring signals would be read out periodically.

The HV supply and PMT base are on a separate board behind each PMT built by industry according to our specifications. The board contains a DC-DC converter, allowing a DAC-controlled HV to be set for each individual pixel, and has voltage and current monitoring. The last three dynodes of the voltage divider network are actively stabilized, allowing a reduction in power consumption compared to conventional resistive dividers.

The total power consumption for a 850-pixel camera is 3.5 kW. The power consumption is 0.2 W/unit for the HV supply and 3.6 W/unit for the pixel electronics. Tests with a full-size model of a quadrant of the camera show that air cooling is sufficient to remove the heat and keep the pixels at constant temperature independant of ambient temperature. The Smart Pixels are inserted into tubes through which air is funneled via small holes in the backplane.

To test the performance of the Smart Pixels, a 19-pixel prototype camera was built up. A photo of the camera can be seen in Hofmann et al. in these proceedings. A custom-built VME-based sender module sends commands via the digital bus to the pixels. The readout frequency for the prototype is 2 MHz. A Hytec VTR2535T 12-bit 10 MHz transient recorder, synchronized with the sender clock, is used to digitize the signals. A pulse generator and a programmable 127 dB attenuator are used to simulate PMT pulses. The performance of the sample-and-hold (pulse response, linearity, noise, dynamic range, out-of-gate signal suppression, droop, fast clear), of the trigger electronics, (minimal discriminator threshold, X/7 trigger efficiency vs. overlap time, trigger timing), and of the slow control electronics (stability of the HV output, DC current linearity, trigger control, temperature readout) were investigated.

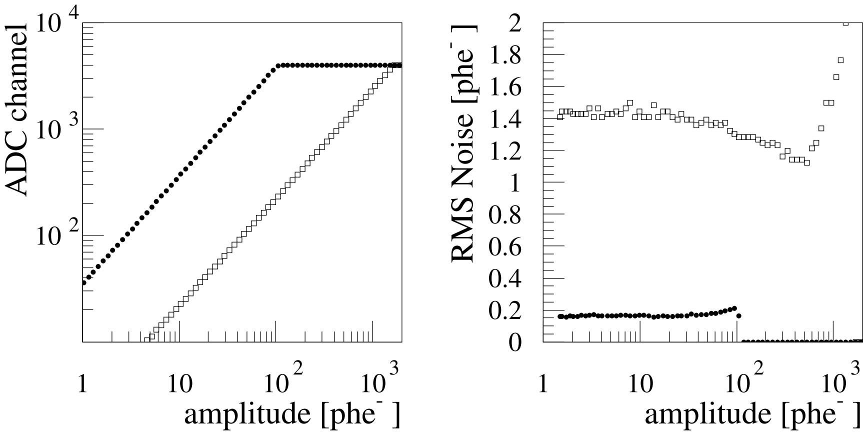

FIGURE 2. The left-hand plot shows the ADC channel as a function of the signal amplitude in photoelectrons (phe$^-$) for the high gain (filled circles) and the low gain (open squares) branch. The right-hand plot shows the rms noise as a function of signal amplitude.

A typical linearity curve is shown in Figure 2. The gate width of the sample-and-hold is 12 ns, the input pulse has a 4.5 ns width (FWHM). Typical pixel output signals for the high-gain branch are a gain of 19 mV/phe$^-$ and a range of 0 - 105 phe$^-$, and a gain of 1.2 mV/phe$^-$ and a range of 0 - 1700 phe$^-$ for the low-gain branch. The useful range is 0 - 2 V. As one can see from Figure 2, the electronics

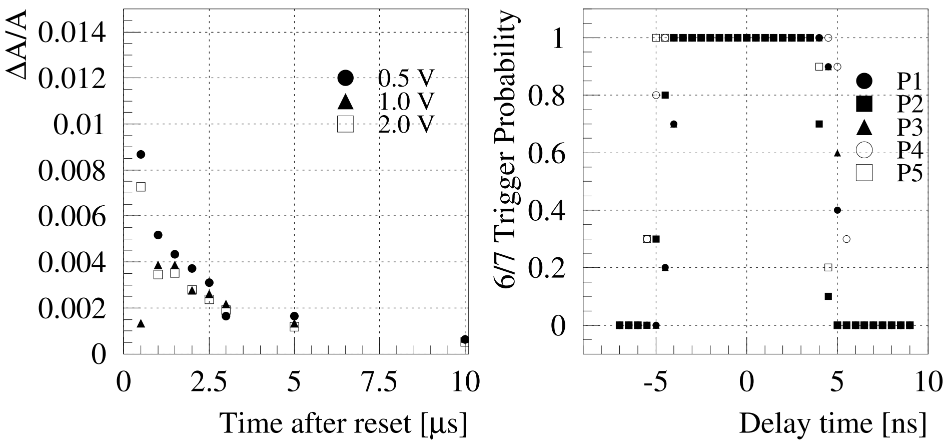

FIGURE 3. The left-hand plot shows the relative increase in amplitude as a function of the time between the reset and the next signal pulse for three output amplitudes. The right-hand plot shows the 6/7 trigger probability as a function of the relative delay time between signals for five neighbor pixels.

have single photoelectron resolution capability. The gate width of the sample-and-hold is adjustable from 6 - 18 ns in 3 ns steps. The time-to-amplitude converter measures the time between the discriminator firing and the camera trigger signal with a resolution of 25 mV/ns, and is used to verify that the gate is centered on the pulse.

The left-hand plot of Figure 3 shows the performance of the fast clear. Waiting an additional 0.5 μs after the reset before enabling the trigger for the next event implies a maximal amplitude increase due to the former signal of 1%. This implies an acceptable deadtime of 2.5 μs for local trigger events not followed by a global trigger. The right-hand plot of Figure 3 shows the performance of the X/7 trigger. The 6/7 trigger probability is measured while changing the relative timing of the input signals. The discriminator output is 8 ns long. There are slight $\leq$1 ns timing differences between the pixels. A 2.5 ns minimal overlap is necessary for the X/7 trigger to fire.

CONCLUSIONS

The performance of the prototype camera has shown the feasibility of the Smart Pixel design for the HESS project. Tests of the prototype camera with PMTs will be performed. The total cost of the camera electronics is estimated to DM 440,- per pixel, including the cost of components, PCB, and mounting of components, for the HV supply, the pixel electronics, the backplane, multiplexer and trigger boards. For a $\sim$850 pixel camera, the total cost is 370 kDM, not including the photomultipliers, the camera mechanics, the power supplies, and the data acquisition electronics.