SAM (Swift Analogue Memory) : a new GHz sampling ASIC for the HESS-II FEE

Philippe Goret, Eric Delagnes
CEA/DSM/DAPNIA, CE-Saclay, F-91191 Gif-sur-Yvette Cedex, France

Patrick Nayman, François Toussenel, Pascal Vincent
LPNHE, IN2P3/CNRS Universités Paris VI & VII, Paris, France

The HESS-II project consists of building a 600m^2 high energy gamma-ray Cherenkov telescope at the center of the existing HESS-I array of four 107m^2 telescopes. The new telescope will work either in coincidence with the array above $\sim$50 GeV or in a standalone mode in the 10-50 GeV range. In the latter mode, the telescope trigger rate is expected to be of the order of a few KHz. This constraint and the requirement of an extended dynamic range both call for a new design of the front end electronics. The Swift Analogue Memory (SAM), a Gsample/s chip developed for the readout of the $\sim$2000 PMTs HESS-II camera, is described in the present paper.

1 Introduction

The HESS (High Energy Stereoscopic System) high energy gamma-ray observatory is a multi-telescope atmospheric Cherenkov array located at 1800m a.s.l. in Namibia (23°16'S, 16°30.0'E). The first phase of the experiment, hereafter called HESS-I, consists of four 107m^2 mirror telescopes, each equipped with a 960 photomultipliers tubes (PMT) camera at the focal plane (see [1] for details). The HESS-I array has been fully operating since the end of 2003 with unprecedented performances: i) an energy threshold of $\sim$100 GeV at zenith, ii) a sensitivity of a few percent of the Crab flux and iii) an angular resolution of a few arcmins. In its first 18 months of operation, the experiment has already yielded a number of outstanding observations above 100 GeV. ¿From detailed mapping of extended SNRs to faint distant AGNs to a systematic scan of the galactic plane, a wealth of new, and quite often unexpected, astrophysical results has been published. However, except for the pioneering observations by the CELESTE and STACEE non-imaging atmospheric Cherenkov experiments, the high energy gamma-ray band 10-100 GeV is largely unexplored so far. Observations of sources with energy cut-offs below 100 GeV, such as pulsars and very distant AGNs,

and/or with very soft energy spectra, call for new instruments with high sensitivity below 100 GeV. This energy range will soon be investigated by the forthcoming space gamma-ray experiment GLAST to be launched in 2007. Still, low energy gamma-ray observations using appropriate imaging atmospheric Cherenkov telescopes (IACT) are needed. The effective gamma-ray detection area for IACTs is of the order of 10^8cm^2 compared to $\sim 10^4$cm^2 for GLAST. Accordingly, the detection sensitivity for (moderately extended) gamma-ray sources is about 2 orders of magnitude larger for IACTS than it is for GLAST. Therefore, despite their inherent narrow field of view of a few degs, IACTs will be able to monitor specific variable faint sources, such as flaring AGNs and GRBs, on a much shorter time scale than GLAST can do. Accurate observations of the energy cut-off region for some pulsars could also be done with high statistical accuracy. ¿From the above considerations, it is clear that a new type of very large IACT sensitive to gamma-rays below 100 GeV is required. Unlike operating a single giant telescope like MAGIC [2], we consider that the new IACT should be integrated to the existing HESS-I array, so that it can also participate to stereo observations.

Taking into account the above considerations, the second phase of the HESS experiment, hereafter called HESS-II, is currently under development. An additional very large telescope, with a mirror collecting area of $\sim$600m^2 and a $\sim$2000 PMTs camera, will be erected at the center of the HESS-I array (i.e. HESS-II = HESS-I + 1). Using the 5-telescopes array, the capabilities of HESS for gamma-ray observations will extend down to $\sim$ 10GeV at zenith.

In the energy range 10-50 GeV, the telescope will operate in the standalone mode since these low relatively energy events will not trigger any of the smaller telescope. In this mode, the averaged telescope trigger rate is expected to be of a few KHz, i.e. one order of magnitude larger than for the HESS-I telescopes. In order to reduce the latter rate still further, a level 2 trigger, based on real time imaging rejection, is considered. For energies ranging from $\sim$50 GeV up to $\sim$100 GeV, it is likely that at least one small telescope will trigger in coincidence with the big one. The trigger rate for these stereo events is estimated to $\sim$1KHz. Above 100 GeV, the trigger rate will be of the order of the present HESS-I stereo trigger rate of $\sim$400Hz at zenith (for the coincidence of $\geq$2 tels out of 4).

Clearly, the HESS-II electronics will have to cope with increased trigger rates together with a dynamic range extended by one decade in energy.

In order to meet these new, more severe, requirements imposed by the lower energy threshold, a new ASIC for the HESS-II Front End Electronics (FEE) has been developed and tested.

2 Fast Analogue Sampling of PMT signals: from HESS-I to HESS-II

The HESS-I FEE design was based on the ARS0 (Analogue Ring Sampling V.0) [3], developed initially for the ANTARES experiment. The PMT output signals are split two ways to a low and high gain channels with a gain ratio of 12.5. Each signal channel is fed into one of the 5 inputs of an ARS0 chip to be sampled at a frequency F_S adjustable from 0.3 up to 1 GHz. The samples are stored in successive capacitors arranged in a 128-cells ring configuration such that each cell is overwritten every 128 cycle by new data. The sampling frequency for HESS-I being set to 1 GHz, the corresponding memory depth for each channel is 128 ns. Upon detection of a local Cherenkov event in a given telescope camera, a trigger signal is sent both to the ARS0 to stop the sampling process and to the central trigger generator to check for simultaneous triggers from other telescopes [4]. The analogue samples are then readout within an appropriate time window with a location in memory corresponding to the event arrival time and a width fitted to the Cherenkov pulse. For HESS-I, the window width is set to 16 ns to accomodate a possible timing jitter and the pulse stretching due to the limited 80 MHz analog input bandwidth of the ARS0. After completion of the 16 cells readout, which takes $\sim$60 μs, the analogue data of one channel are multiplexed towards the ADC . The 16 digital samples are then summed and sent to an FPGA buffer for further processing. The overall readout time per event is $\sim$275 μs which limits the acquisition bandwidth to $\sim$4 Kevents/s. With the HESS-I trigger rate of a few hundreds Hz the deadtime amounts to 10-15%. It is clear that with a projected HESS-II trigger rate of a few KHz, the readout time of the present FEE would lead to unacceptably large values for the deadtime. Therefore, the FEE architecture had to be redesigned to achieve event readout times in the μs range. In particular, it implies that a new analog sampling ASIC be conceived with readout time in the range of a few μs. It turned out that the ring architecture *à la* ARS0 was no more adapted to this new constraint, leading to a matrix design instead. Another advantage resulting readily from the matrix structure is that the readout noise is greatly reduced compared to the linear case. In turn, it leads to a significant increase in the dynamic range as is required for the HESS-II FEE. Finally, the 0.8μm technology used for the ARS0 is outdated so that the design had to be optimized for the new 0.35μm technology. For all these reasons, (and some more), a new ASIC for the analog sampling of the HESS-II PMT signals has been designed and tested. In the next section, the new chip is described and tests results are presented.

3 SAM: a new Swift Analogue Sampling ASIC for HESS-II

Taking into account the constraints elaborated in the preceding chapter, the new analogue sampling ASIC for HESS-II should now meet the following requirements:

- a fast readout time of analog data from memory of a few μs
- a dynamic range of 11-12 bits per channel
- an increased input bandwidth of $\sim$300 MHz
- a cross-talk reduced to a few per mil
- a linearity better than 2 % over the full dynamic range
- an adjustable sampling frequency of up to 2 GS/s
- a memory depth increased up to 256 cells (128 ns at 2 GS/s)
- a low power consumption in the range of $\sim$300mW/chip

The SAM block diagram is shown in fig. 1.

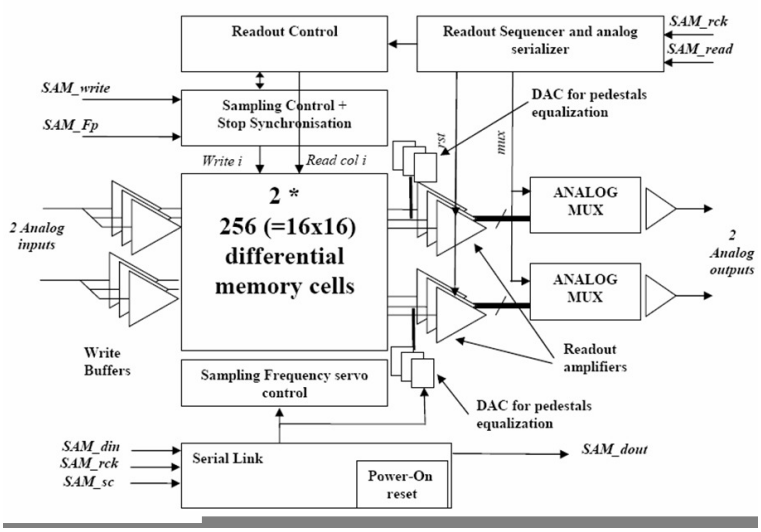

Figure 1: the SAM block diagram

With an area of 10 mm^2, the ASIC is designed using the 3.3V CMOS AMS 0.35μm technology. As done in the ARS0, the sampling frequency F_S of the SAM is obtained by virtual multiplication of the lower frequency clock F_P using internally

servo-controlled Delay Line Loops (DLL). The design was made so that DLL unlock during readout is avoided, which otherwise would add extra deadtime between events.

An analogue memory channel is configured as a matrix of 16×16 capacitors, as shown in fig.2. Such a configuration enables a larger bandwidth/power consumption ratio and a better immunity to switching noise to be obtained than is possible with the linear structure of the ARS0. The analogue input signal is sampled at a rate F_S and written to successive capacitors *in the same column* until the column is filled up. Then the following data are written to the next column. Consequently, the successive capacitors *in a given line* contain samples separated in time by $1/F_P=16/F_S$ (i.e. 16ns at F_S=1 GS/s).

This structure, which enables a fast parallel readout of groups of up to 16 consecutive samples, is perfectly suited to handle fast Cherenkov signals with duration of several ns. The data are further multiplexed and digitized by an external ADC (one per channel) at a rate of 11 MHz.

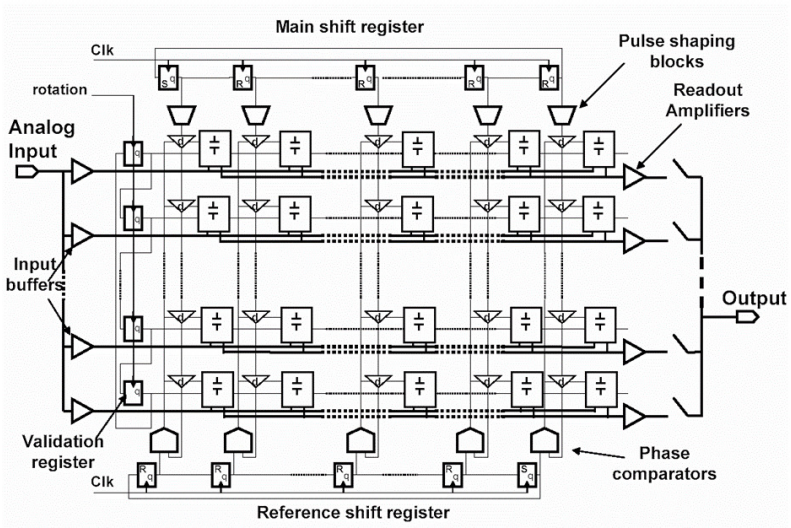

Figure 2: The 16×16 capacitors matrix configuration of the SAM. The data are written in successive cells one column after another

A peculiarity of the matrix structure is that each line has its own offset (or pedestal) which leads to a cell to cell dispersion of the readout values. Two 7-bits programmable DACs per row are provided in order to compensate for the readout baseline. The DACs should be set prior to starting the acquisition. Both the DACs and the number of consecutive cells to be read per event, N_F, are programmable through

a serial link. The latter can also be used to configure the chip in various operating or testing modes. Both analogue channels in the SAM are fully differential, which greatly reduce the digital cross-talk. All inputs and outputs use LVDS standards.

The main tests results on the first SAM prototype are given in the next section.

4 Test results and performances from the first SAM prototype

The first SAM prototypes were received in April 2005 and thoroughly tested. The SAM test board itself was designed as a prototype of the HESS-II front-end electronics. It includes 2 dual-gain ($\times 1$ and $\times 25$) channels, each fitted with a fast discriminator to allow auto-triggering. The SAM characteristics, as measured on this test bench, are summarized in Table 1.

The SAM prototype has been characterized using the nominal sampling rate of 1 GS/s, but the chip can operate up to $\sim$2.5 GS/s. A most important result is that the measured readout time for a typical 16 cells event is $\sim$1.6 μs, which fully meets the requirement. The dynamic range of $\sim$11.3 bits has been checked to be within specifications . The linearity has also been evaluated using PM-like pulses from a generator over the full HESS-II dynamic range. As shown on fig. 3, the integral non-linearity over the range 1-5000 photoelectrons is found to be less than 2%, as required for unbiased HESS-II spectral measurements.

Finally, the amplitude spectrum of single photoelectrons generated from a PMT is shown in fig. 4. A standard deviation/mean ratio of $\sim$0.5 and a peak/valley ratio of $\sim$1.5 for the single photoelectron peak is observed. These results confirms the suitability of the SAM for calibration of the HESS-II camera using single photoelectrons (as is currently done in HESS-I).

A more detailed evaluation of the SAM chip will be found in a forthcoming paper [5].

5 Conclusion

The HESS-II project of a very large atmospheric Cherenkov telescope to detect high energy gamma-rays down to 10-20 GeV requires a novel design of the FEE electronics to cope with the associated increased trigger rates and larger dynamic range. The SAM, a dual-channels ASIC for fast analogue sampling of PMT signals, has been specifically developed for the HESS-II project. Its matrix architecture brings significant improvements compared to the older ARS0 linear design, as is currently used in HESS-I. A prototype of the SAM has been successfully produced and tested. With a

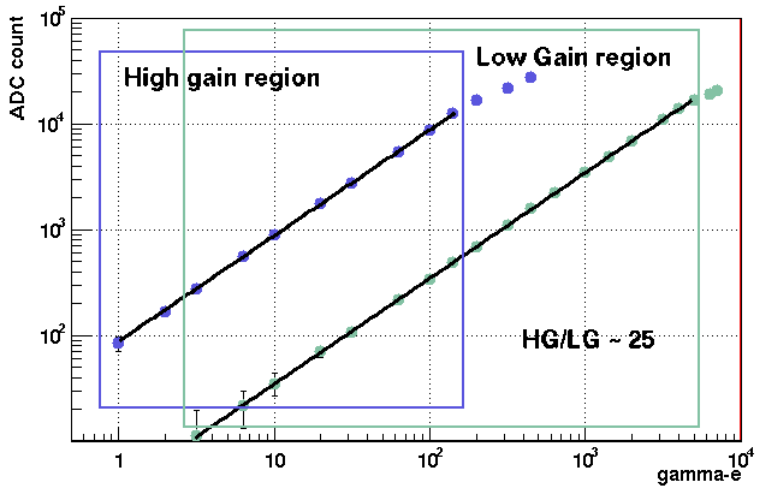

Figure 3: The measured linearity on the prototype SAM low and high channels

dynamic range of ∼11.3 bits, an analog input bandwidth of ∼250 MHz and an event readout time of less than 2μs, the SAM performances meet the HESS-II stringent requirements. The final chip will be manufactured by mid-2006. After testing, it will be implemented in the FEE of the HESS-II camera for commissioning in early 2008. A upgraded version of the SAM, with an on-chip ADC, is also under development.

References

[1] Hinton, J. A. 2004, New Astron. Rev., 48, 331

[2] Mariotti, M. 2005, these proceedings pp. 29-41

[3] Lachartre, D., Feinstein F. 2000, Nucl. Instr. Methods **A**, 442, 99

[4] Funk, S., et al. 2004, Astropart. Phys., 22 285

[5] Delagnes, E., et al. 2005, to appear in Proceedings of the IVth Beaune Conference on Photodetecteurs, Beaune, June 19-24 2005

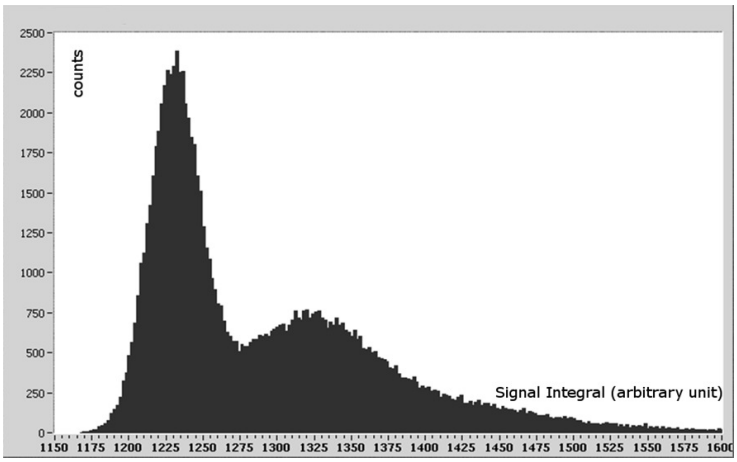

Figure 4: The amplitude distribution of single photoelectrons as recorded by the prototype HESS-II FEE chain, including the SAM

Parameter	Value	Unit
Power cons.	300	mW
Sampling Freq.	$<$1 up to 2.5	GS/s
Analog Bandwidth	$\sim$250	MHz
Max event readout freq.	$>$400	kHz
Readout time N cells	90+90$\times$N	ns
Noise/channel	0.8	mV rms
Maximum signal	2	V
Dynamic range	11.3	bits
Crosstalk	$<$3	per mil
Integral non-linearity	$<$2	%

Table 1: Measured main performances of the SAM first prototype