A Multi-channel Digital Acquisition System for Nuclear Spectroscopy Experiments

S. Riboldi [1,2], F. Zocca [1,2], F. Camera [1,2], A. Pullia [1,2], C. Ur [3], R. Isocrate [3], D. Bazzacco [3]

[1] Universita' degli Studi di Milano - Italy; [2] I.N.F.N. Milano - Italy; [3] I.N.F.N. Padova / L.N.L.- Italy

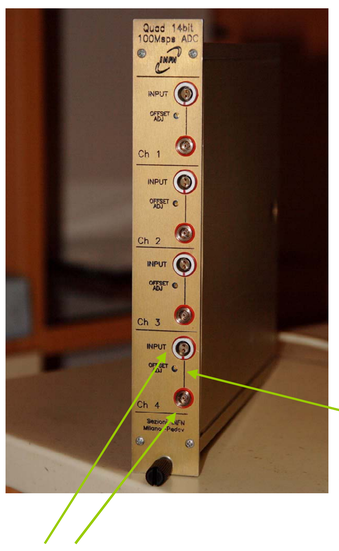
Main Characteristics of DAQ System are:

- 4 Channels per NIM Module
- 14 bit, 100 MSamples/s Free Running ADC per Channel
- Low Noise Front-End Electronics with Adjustable Gain
- Fully Differential Design for Improved Noise Immunity
- Fast transmission link to PCI boards into user PC

In 2005 we developed a 4-channels DAQ system, in mechanical NIM standard, that achieves good performances in terms of noise, bandwidth and linearity.

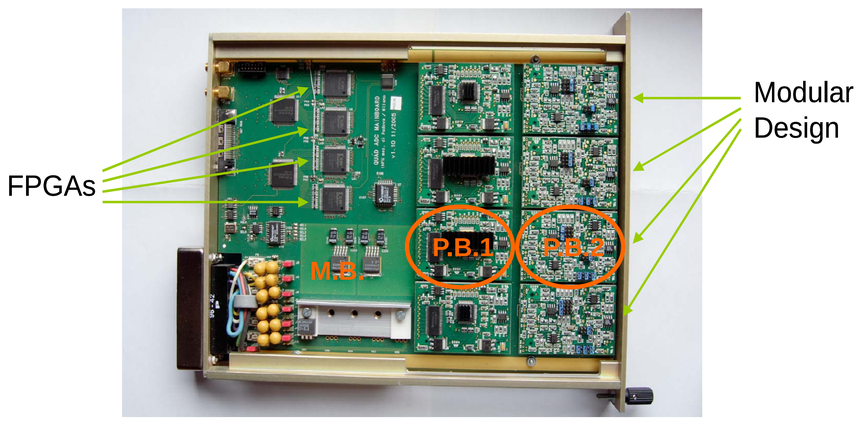
Among its main characteristics are: choice of single ended or differential input standard; selectable inversion of polarity and selectable attenuation (0dB / 12 dB); signal conditioning providing selectable gain (0dB / 6dB / 12dB / 18 dB) and offset correction; anti-aliasing filtering with 30 MHz bandwidth; fully differential architecture in order to minimize the effect of common-mode disturbances.

Analog to digital conversion is based on the Analog Devices AD6645 A/D converter (14 bits, 100 Msamples/s,1.75W power consumption, single ended digital signal output), i.e. one of the most suitable devices at the time of choice.



This entire system is based on a modular design, i.e. each one of 4 DAQ channels is composed of a mother-board and two small piggy-back boards, one for analog signal conditioning and the second one to implement analog to digital signal conversion and single ended to differential conversion for the ADCs digital output signals.

The mother-board, apart from mechanical support, provides ADC signal collection and back-conversion into single ended electrical standard and their serialization for high-rate transmission into commercially available twisted copper cables.



In order to provide the required task of ADC signal collection and conversion, but also to allow for additional flexibility and future needs, we choose to use 4 field programmable gate array (FPGA) devices by Xilinx (XC3S50-4VQ100C), very small in terms of logic equivalent number of gates.

The overall DAQ system is composed also by a far-end custom-made PCI receiver board, connected to a personal computer running the Linux operating system. The whole system has been tested and shows good performances, in agreement with the needs of nuclear spectroscopy experiments.

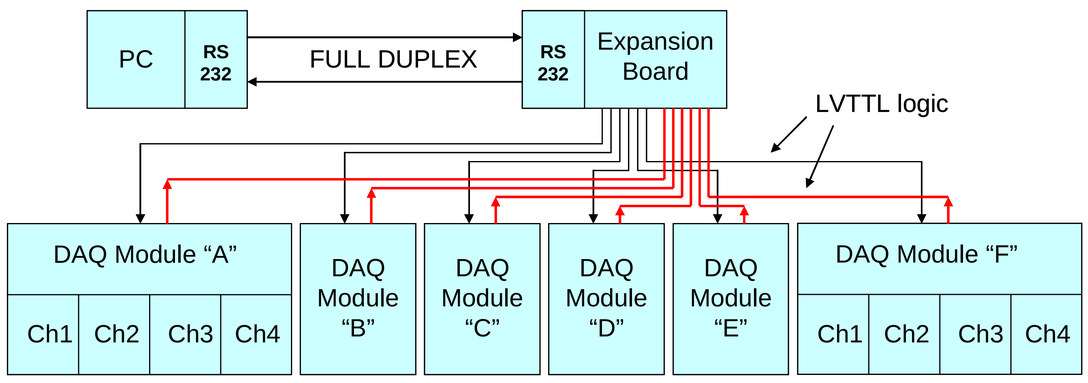
New Features for the DAQ System of the Gerda Phase I Experiment

- Real Time Digital Trigger (with good noise rejection)
- Slow Control (asynchronous serial link to user PC)
- Rate-Meter of Events
- Digital Estimator of Signal Baseline Level
- Self-adaptive Synchronization of ADC Readout Clock

In order to better fulfill the requirements of actual multi-channel nuclear spectroscopy experiments and thanks to the availability of digital logic resources in the FPGA devices, we've recently worked to add more functionalities into the DAQ system.

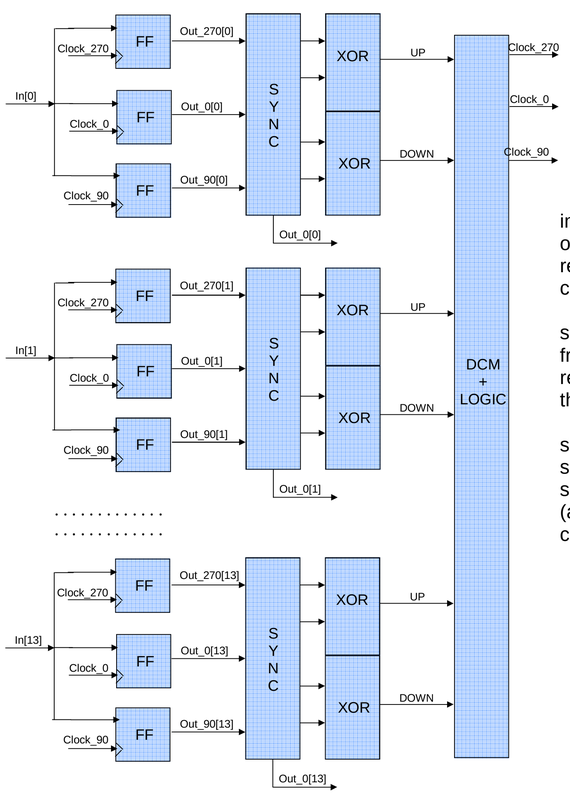
We implemented: i) a bi-directional asynchronous serial (UART) link between the user PC and the DAQ system as a whole, e.g. consisting of up to 64 channels in 16 NIM modules; ii) a digital trigger with user definable thresholds for every channel, able to detect even very low level pulses with small amplitude-to-time skew; iii) a digital counter of triggered events for each channel; iv) a digital estimator of baseline level for each channel, working even in presence of low-to-medium rate (100/200 cps) of incoming events and v) adaptive phase-delaying of the ADCs digital output signals and their alignment to a single global clock.

Slow control of multiple DAQ modules through a single PC user interface



- RS232 interface implemented in Xilinx Spartan3 FPGA with dedicated VHDL code (38400 bit/s custom and efficient protocol with CRC implementation)
- 16 byte-long user register available for each DAQ channel
- Each one of the DAQ channels is specifically addressable through the expansion board
- Diagnostic of defective channels implemented at expansion board level

Self-adaptive Synchronization of ADC Readout Clock

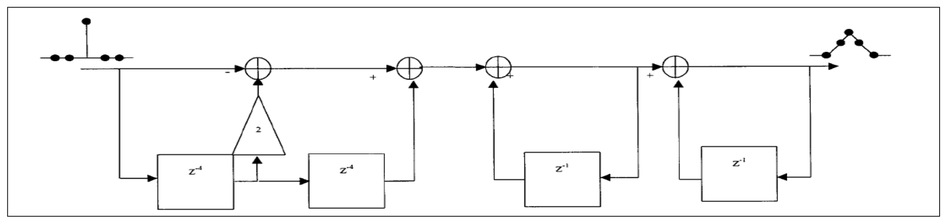


In order to reliably operate ADC signals readout we implemented a real-time self adjusting method to optimally adjust the phase relationship of the ADC readout clock signal with respect to the main system clock (100 MHz).

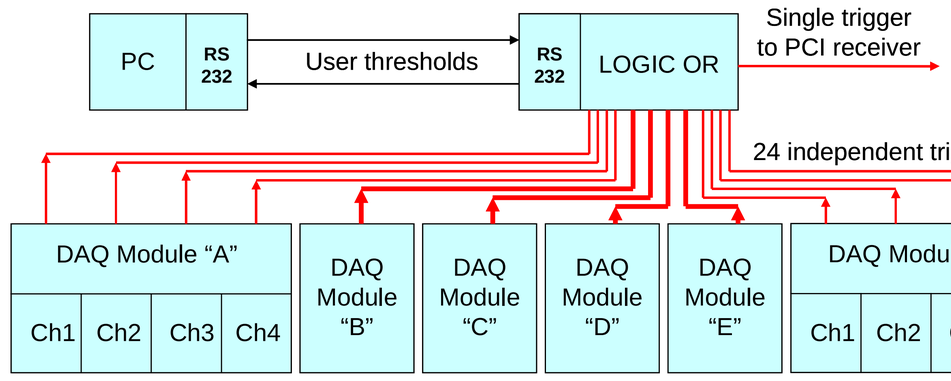
Three registered signals for each ADC output signal (14 bits) are compared. They are obtained from three different clock signals, with fixed phase relationship of –90, 0, +90 degrees with respect to the actual ADC readout clock signal.

If all of them are equal, the ADC readout clock signal is optimally set; if that is not the case and some discrepancies are present, all three clock signals are shifted by a very small amount of time (about 15 ps) on the right side, until the optimal condition is met again.

Real Time Digital Trigger



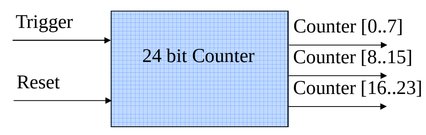
Resource saving implementation in a very tiny Field Programmable Gate Array (FPGA) device (Xilinx Spartan3 50), using Dual Port Block-RAMs and accumulators. The peaking time of the trigger filter is set to 1 us, as a good compromise between signal sensitivity/noise rejection and the ability to detect consecutive events close in time, but could be extended up to about 10 us. (See A. Geraci et al.: "Digital spectroscopy in programmable logic", TNS, IEEE)



- Digital trigger has high sensitivity and low time-to-amplitude walk
- Trigger is implemented with resource-saving techniques in FPGA
- Each DAQ channel can have independent trigger thresholds
- The expansion board provides logic OR-ing of all triggers from the DAQ channels

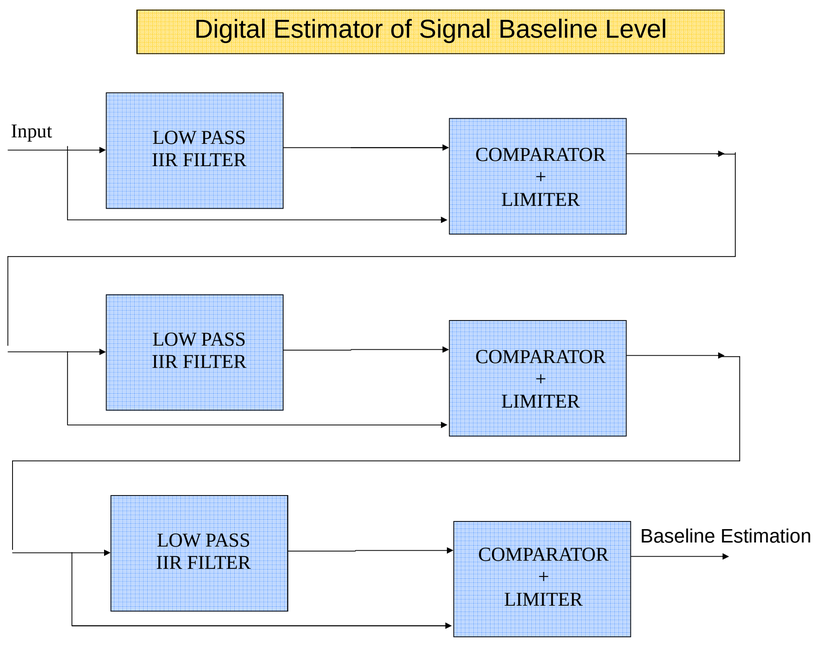
Up to 24 DAQ channels will be connected to a single PC, each one with specific user defined trigger threshold and trigger enable parameters.

Rate-Meter of Events



Counter reset and counter enable are accomplished by setting the proper bit level in the Counter User Register through the UART slow control; counter value is read as 3 separate bytes, after disabling the counter to avoid inconsistency.

Digital Estimator of Signal Baseline Level



Baseline estimation is based on a recursive procedure, that is implemented by means of resource sharing techniques in FPGA (e.g. a unique high speed block is multiplexed to many low frequency signals).