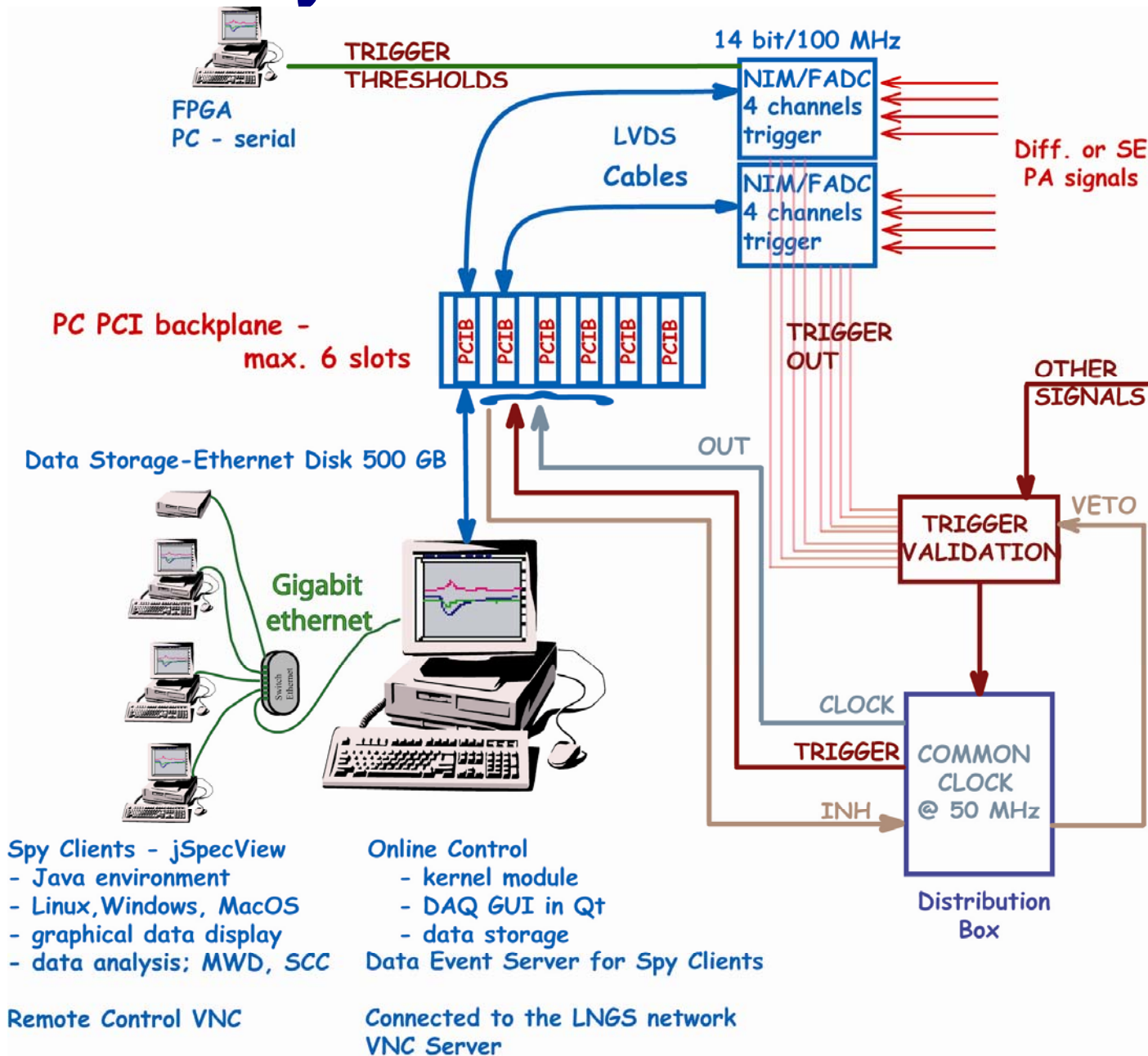# GeDDAQ and Online Control

Status Report

INFN Padova

INFN & University Milano

Calin A. Ur

General Layout

New Features

- DMA readout from PCI

- updated core PCI → PCI transfer at 32bit/66MHz

  → max.output rate > 60 MB/s (calibrations) – limited by the HD write speed

- counters: 64 bit clock   counter @ 100 MHz / NIM module
  32 bit trigger counter
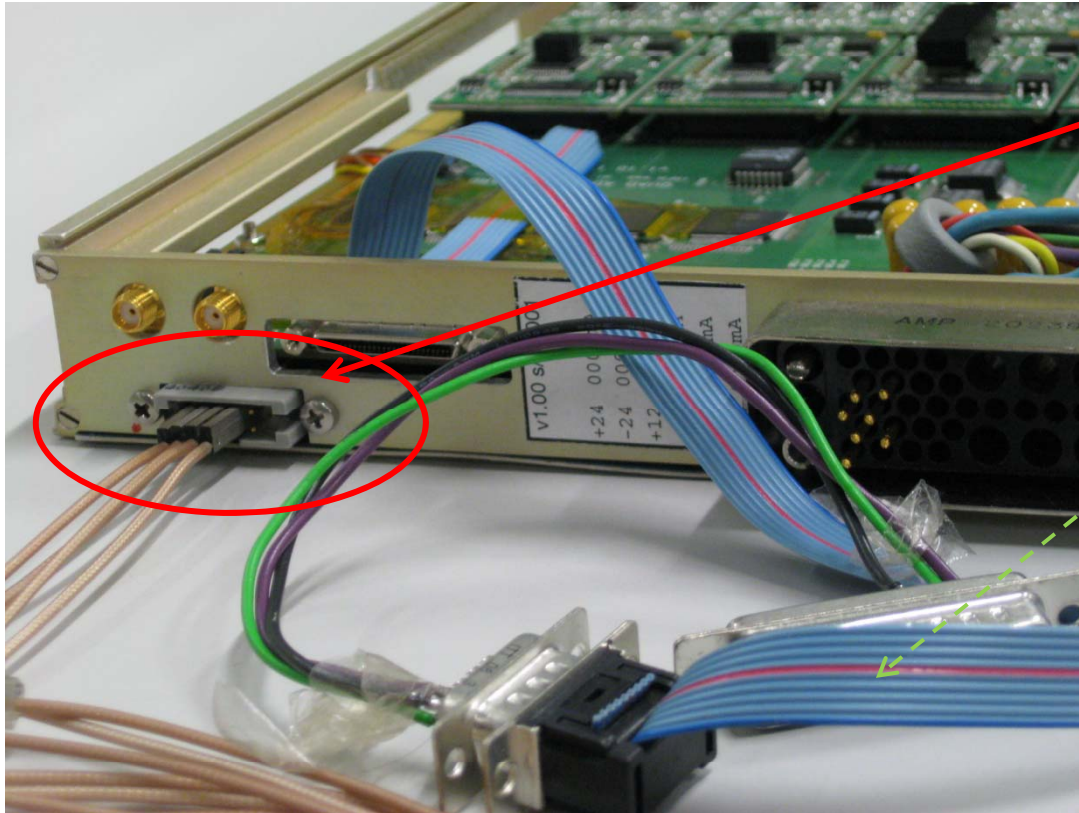
  system running test measurements

- synchronization of data transfer when several boards work together (FPGA)

  → 1 master PCI board – produces the irq request

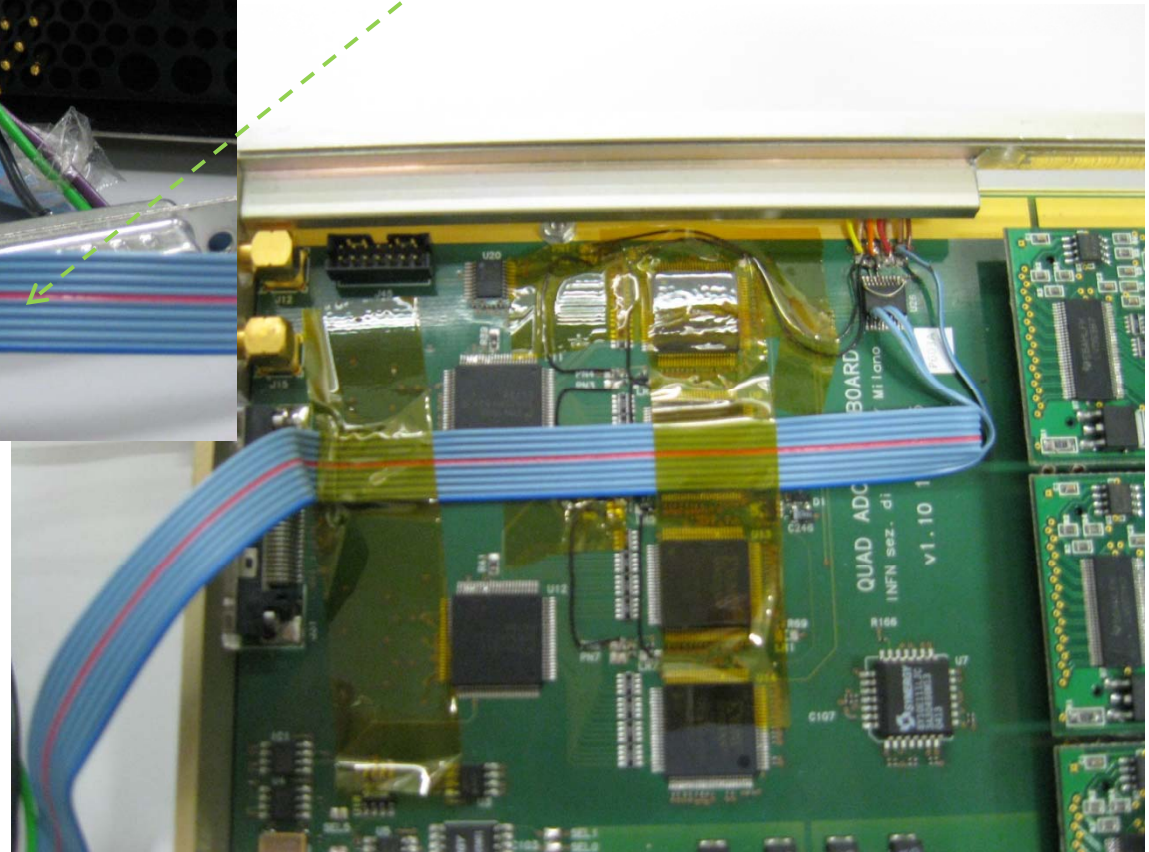 → slave PCI boards – notify the master board when transfer is finished

Internal Trigger

- implemented in the Xilinx FPGA's on the NIM boards

Prototype board
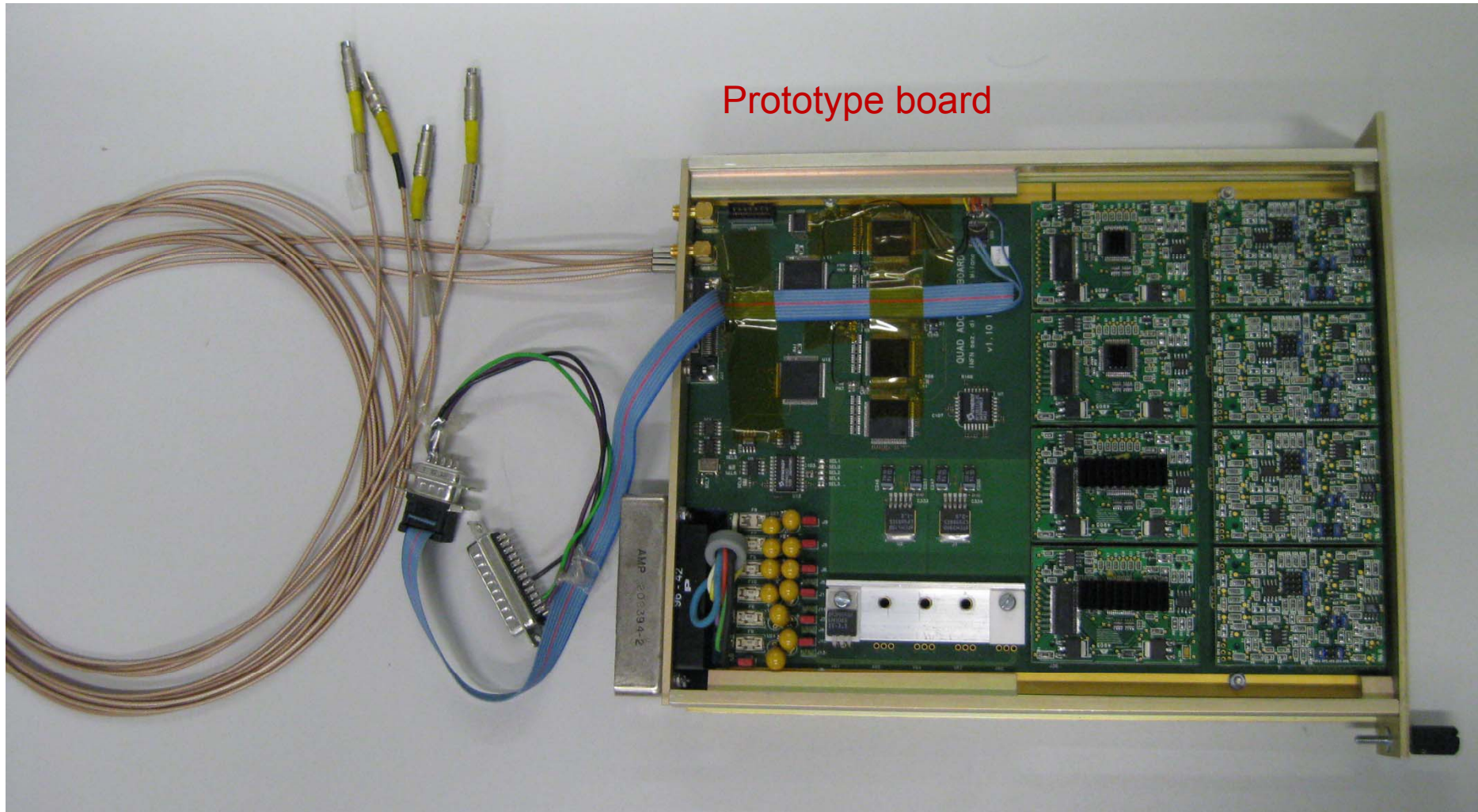
Internal Trigger

- 10 pin multiple connector
  - 4 x 2 TTL out signals
  - 2 x serial prog. thresholds

Internal Trigger

- simple algorithm – dual delay line

  – triangular filter

  – signal offset removal

  – independent of the signal height

  – low energy threshold

- threshold programmed from PC or specialized FPGA via serial line

- individual output trigger signals TTL

Advantages

- eliminates the need of splitting the signals from the Ge detectors

- simplifies the trigger electronics needed for starting the DAQ

Online Control

DAQ Control – running on Linux OS

- setup the DAQ configuration

- manage the communication between PC and PCI cards

    (load/unload kernel module)

- save data on disk

- monitor the acquisition rates and acquisition time

Graphical viewer and analysis program - jSpecView

- platform independent (Java) – online/offline

- manipulation of digital waves – digital filters

- building and saving of histograms

- setting gates and building histograms with conditions

- standard spectra operations (calibration, fit, integral, …)

- oscilloscope function

- generating and viewing of 2-D matrices

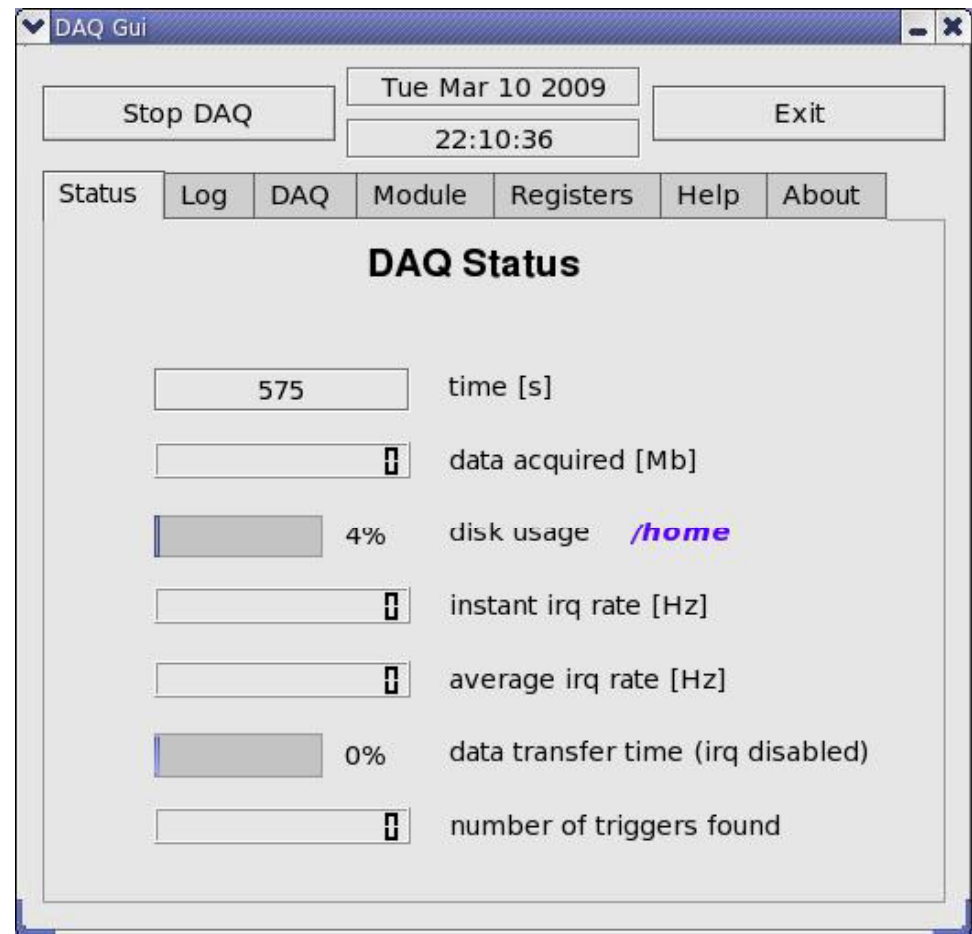# DAQ Control

- **kernel module linux 2.4**

  - handles the interrupts from PCI cards

  - transfers the data from PCI cards

  - minimal data manipulation

  - pipes the data into a character device

- **user program**

  - takes the data from the character device

  - saves only the channels selected by the user

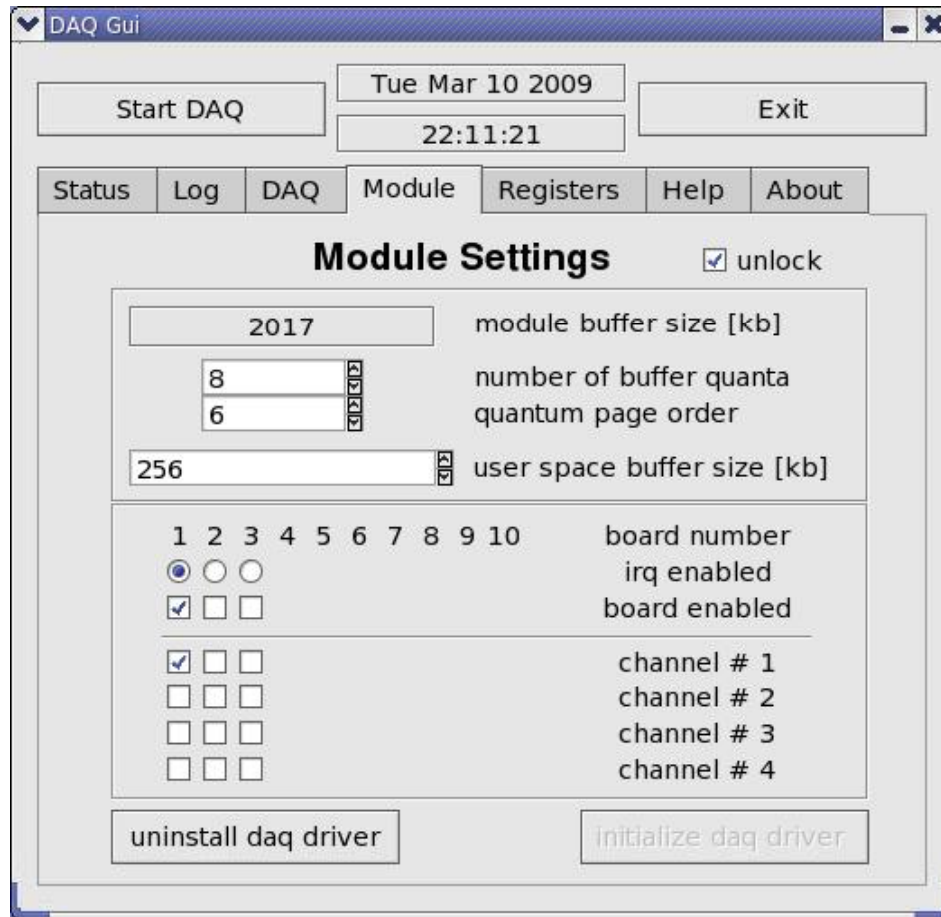 - writes the data on HD

- **graphical user interface**

  - developed in Qt 3

  - controls module loading and data manipulation

  - start/stop of the acquisition

DAQ Control

- load/unload the kernel module
- select the channels to be acquired
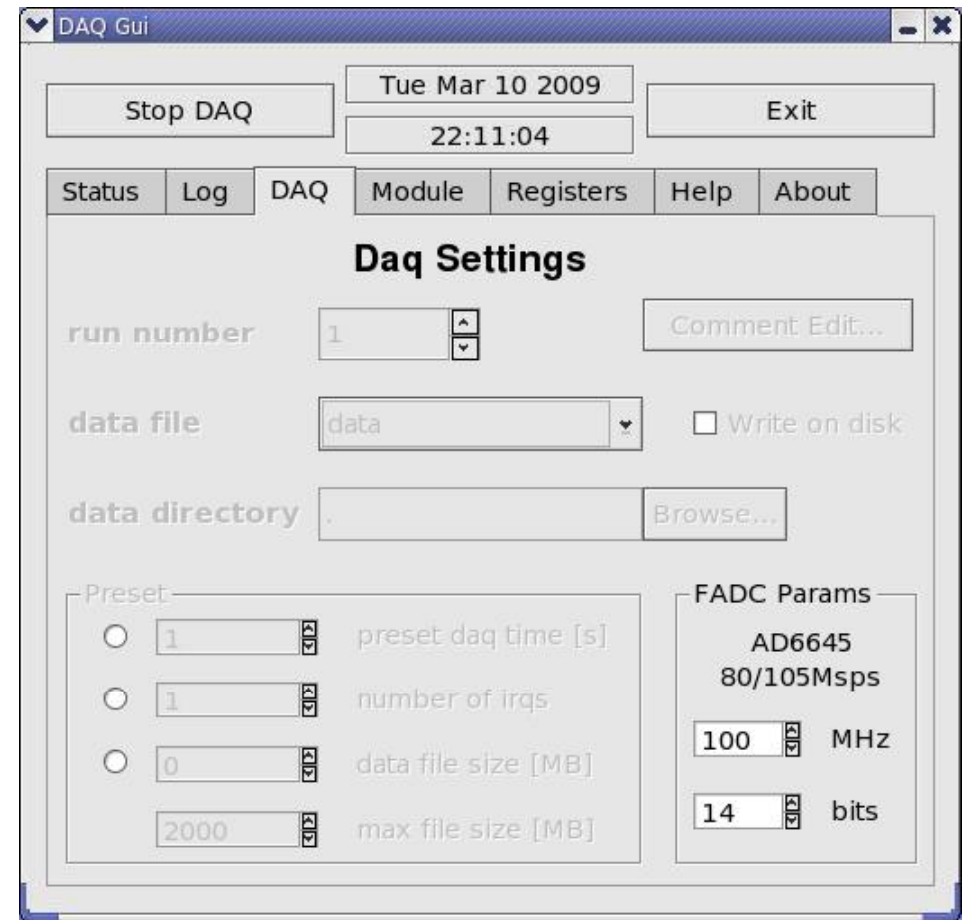- buffer size – when data are written on disk

- define the position of the leading edge
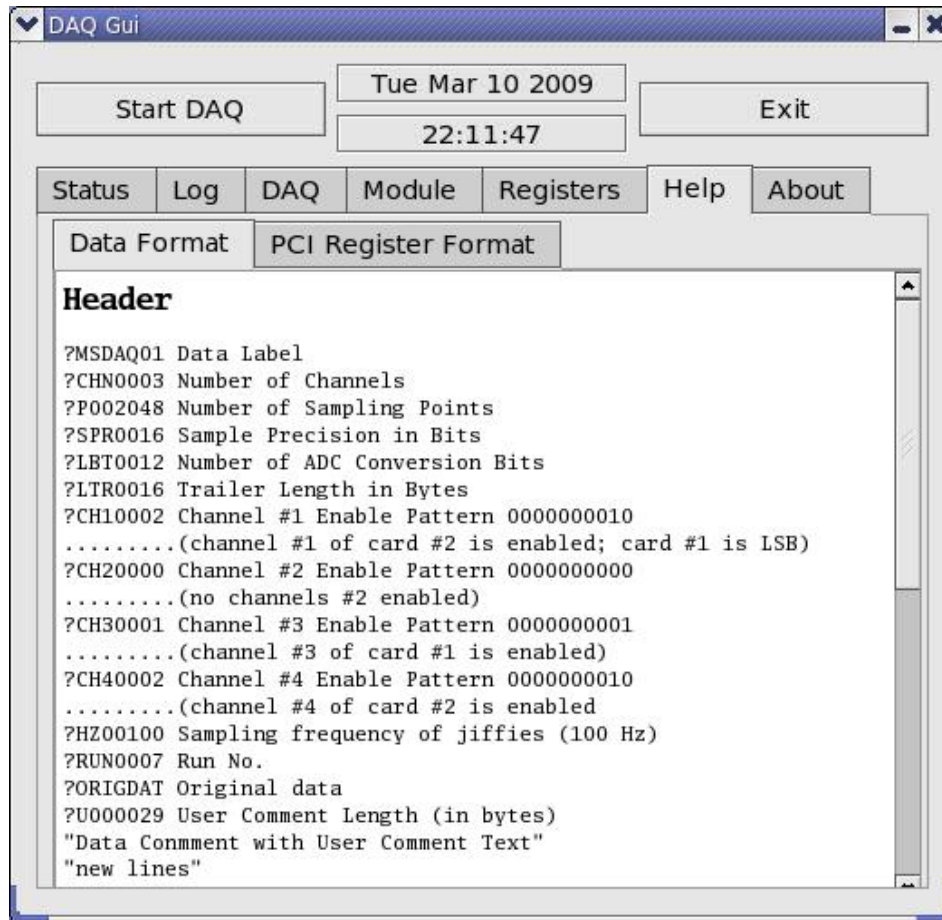- enable/desable debug ramp

DAQ Control
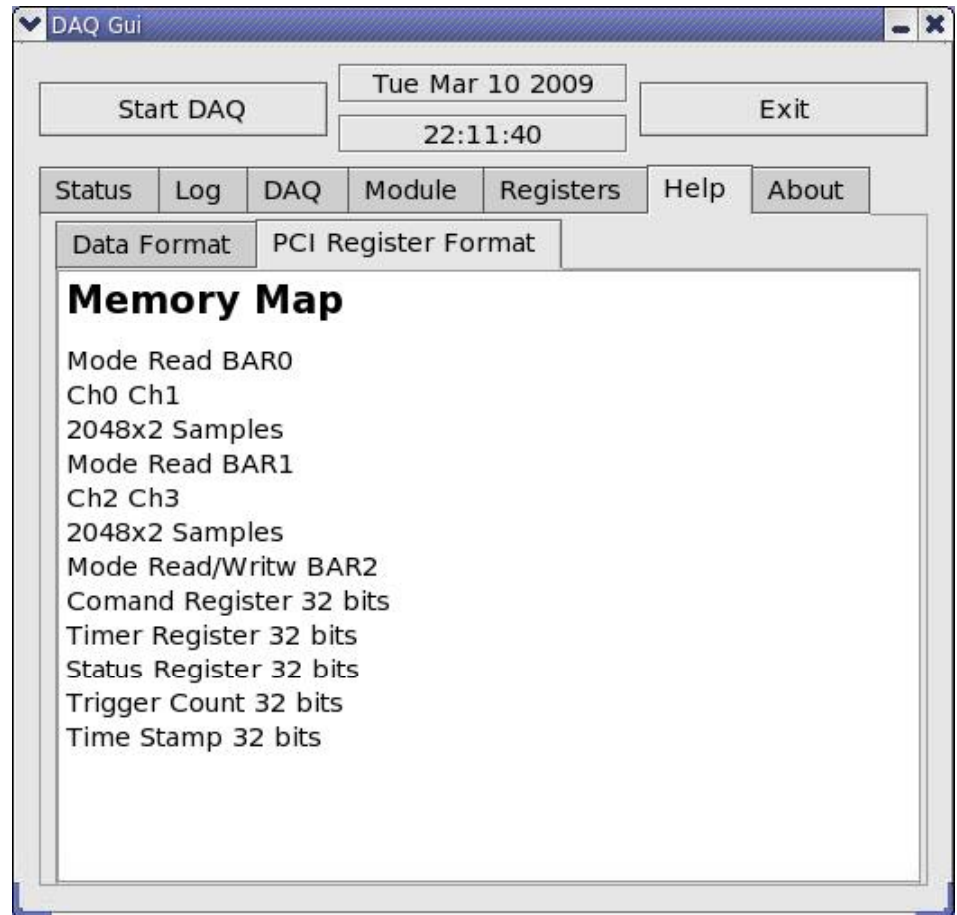

- logging the performed operations

- enable/disable write on disk
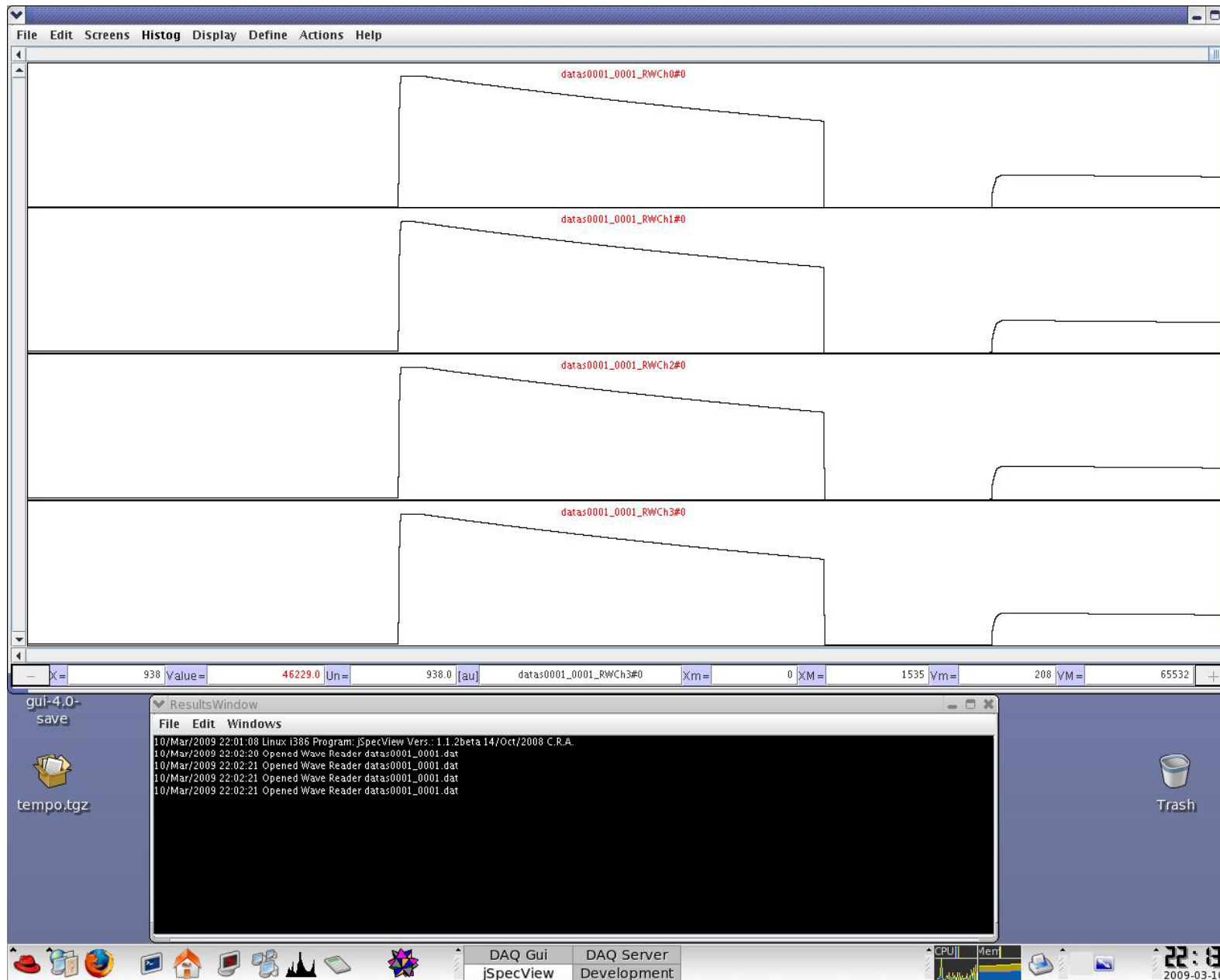- run comments
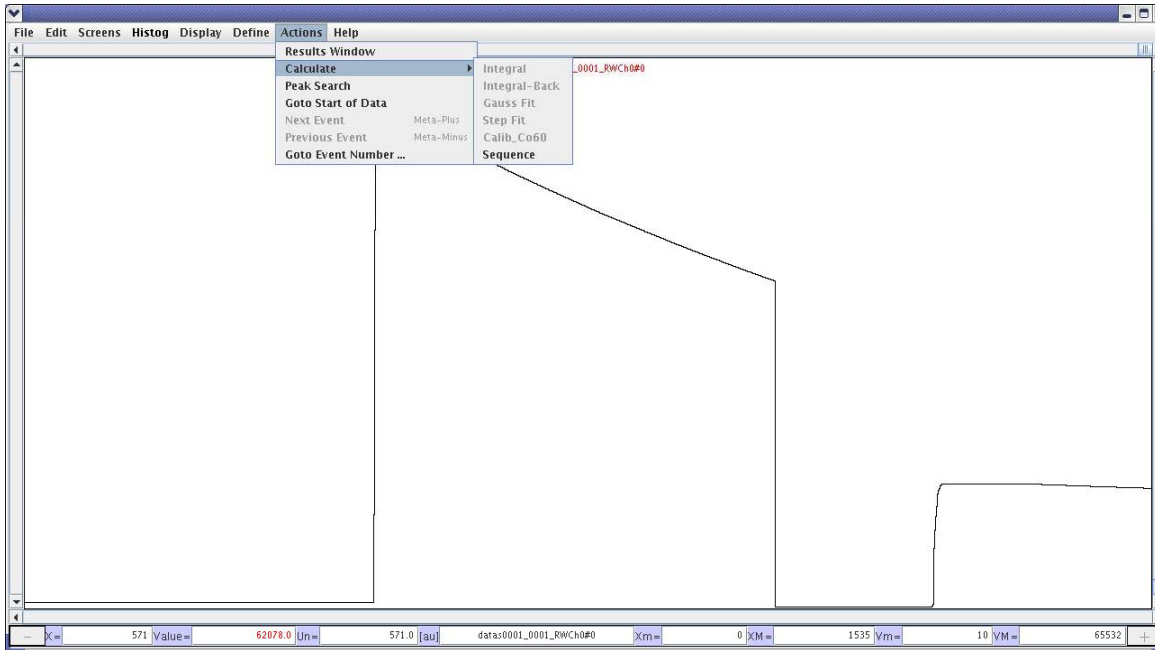- presets

DAQ Control

- data format

- configuration of the PCI memory bars

Graphical Analysis - jSpecView
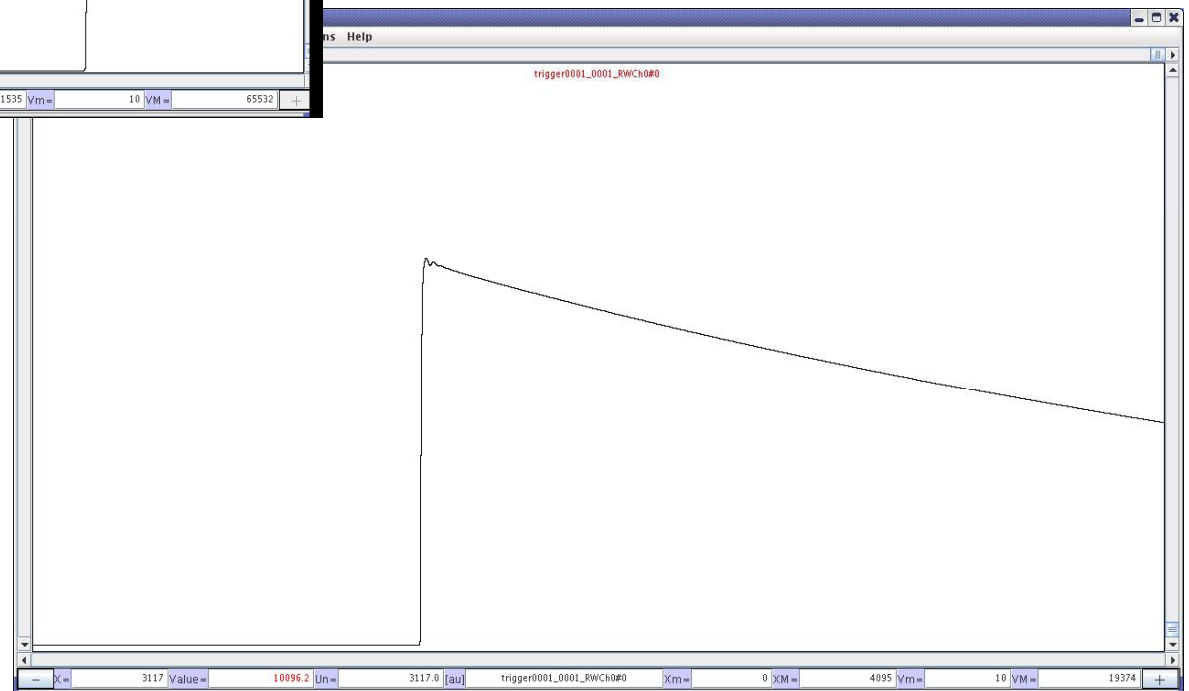
Graphical Analysis - jSpecView

- structure of the original data stored
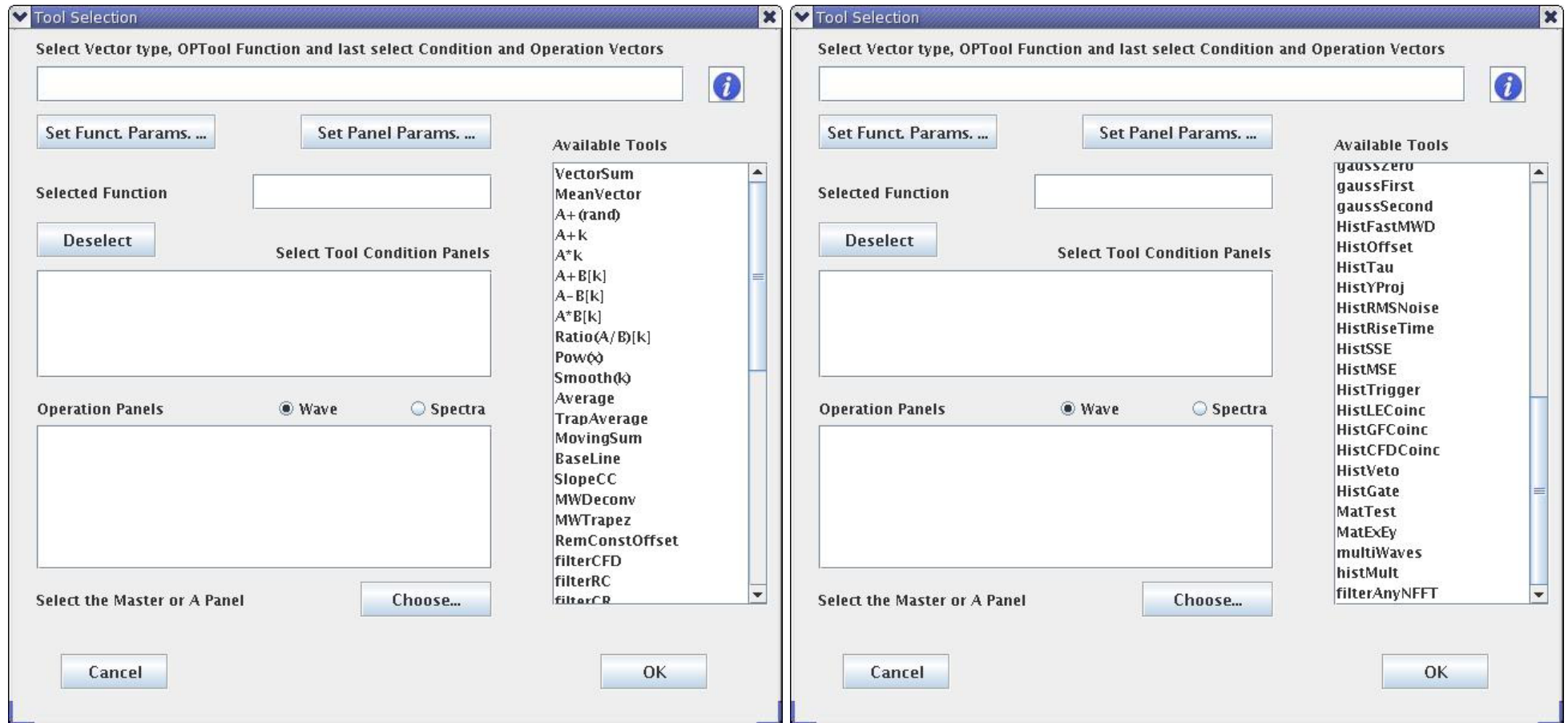
on disc:

- 1024 channels @ 40 ns/chan

- max 512 channels @ 10 ns/chan

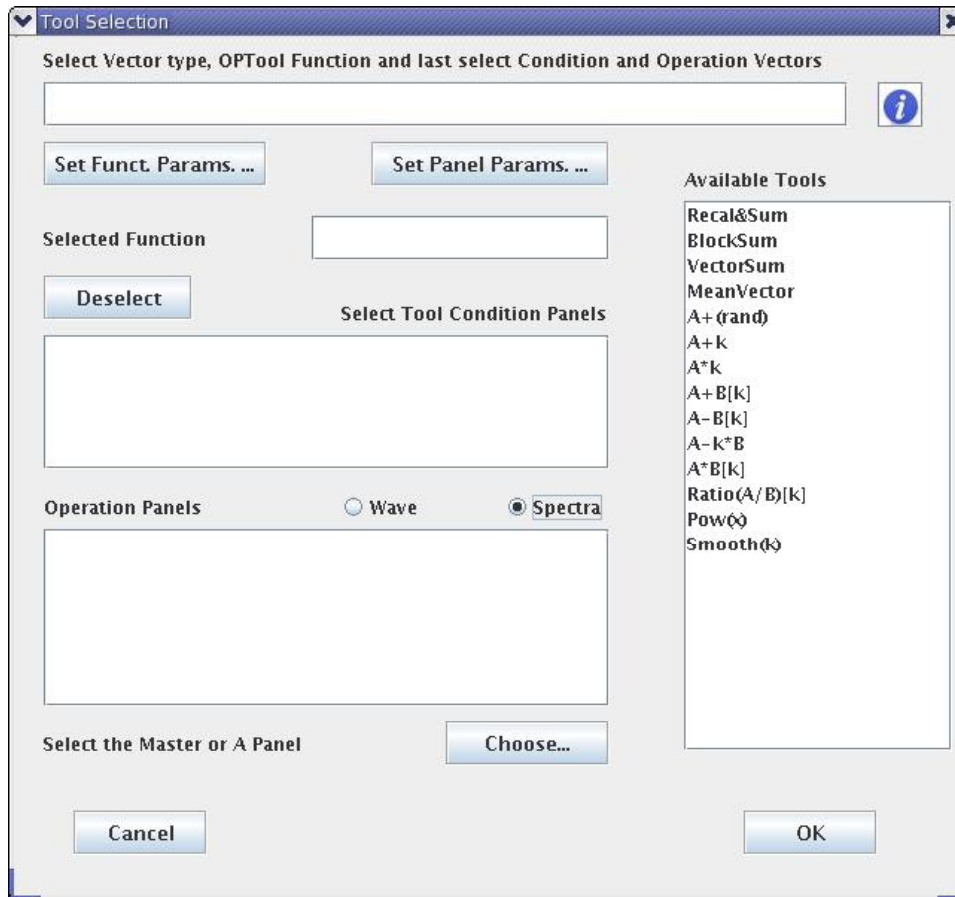- reconstructed wave for analysis

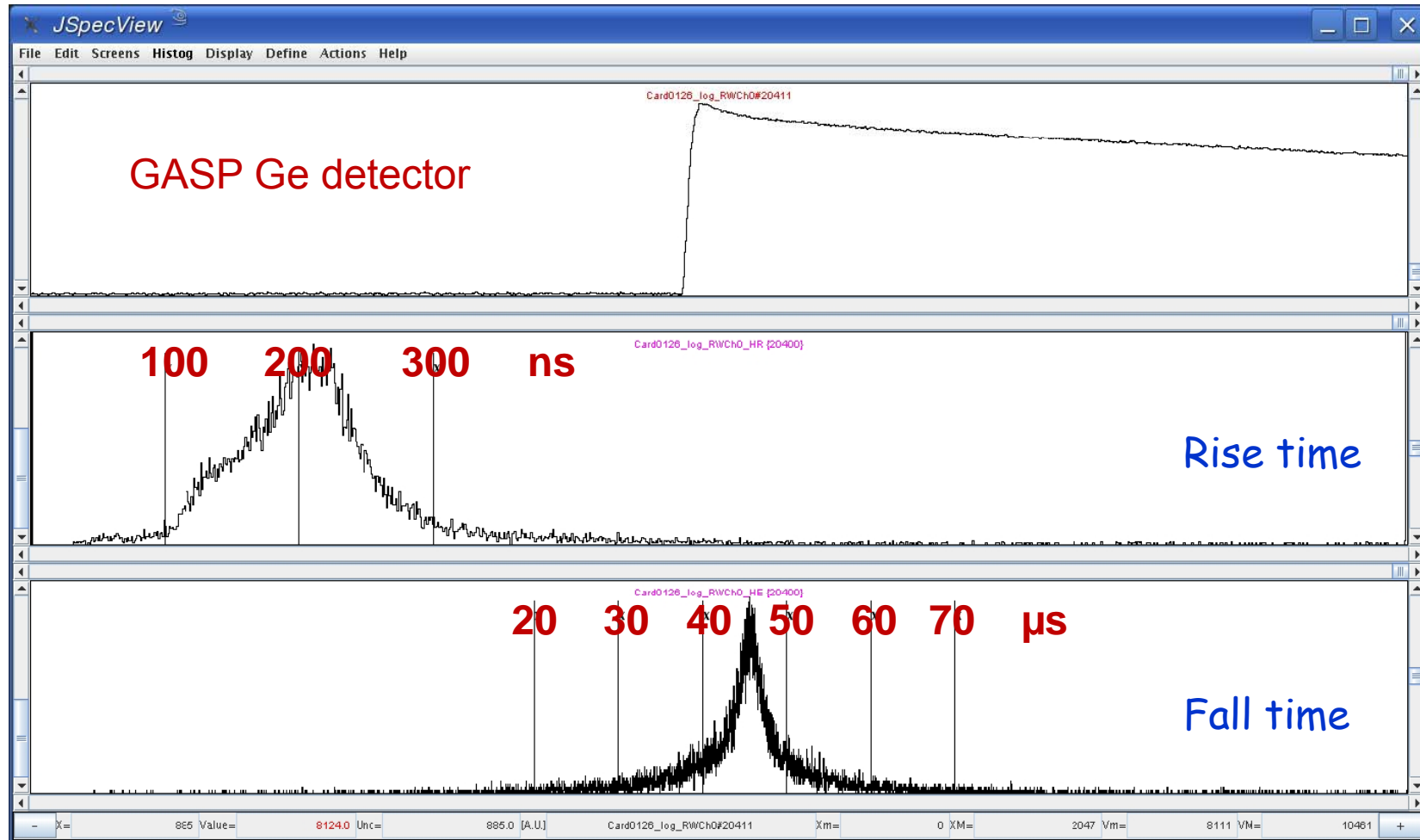# Graphical Analysis - jSpecView

- operations with waves

Graphical Analysis - jSpecView

- operations with spectra

Graphical Analysis - jSpecView

- rise time and fall time determination

Graphical Analysis - jSpecView
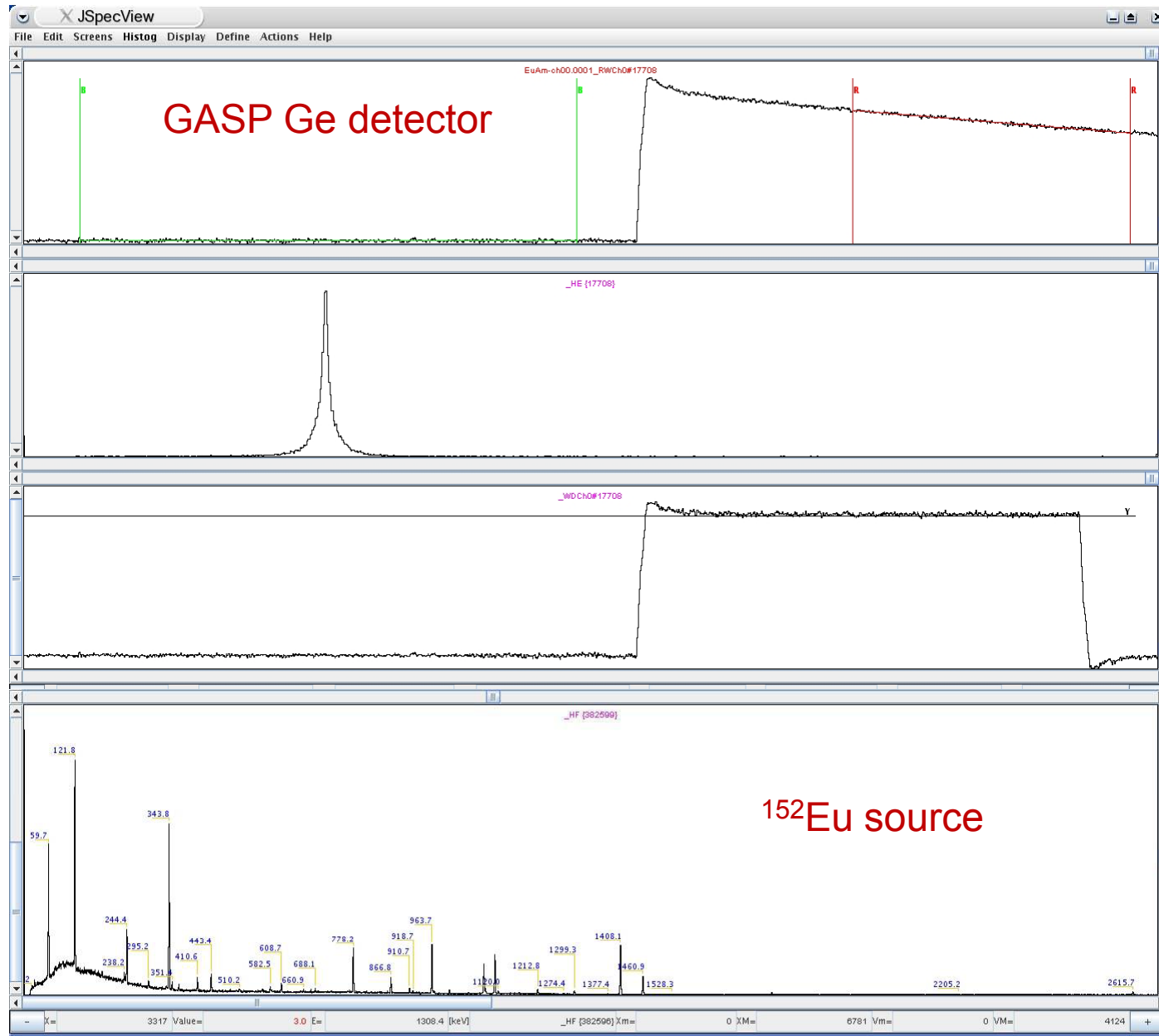
- example of MWD to produce an energy spectrum

Leakage Current Monitor

- continuously monitor the position of the baseline for all detectors

- quantify the baseline shift in pA

        -trigger needed to record data

           - produce periodically a train of TTL signals to be used as

              trigger

           - identify these events by registering a signal on a supplementary

              acquisition channel

           - data analyzed by a specialized program and the values passed

              to Slow Control (graphic, alarm)

     $\rightarrow$ CRON process (PC)

Remote Control

Visible to the LNGS network

Outside world tunnel via a local PC
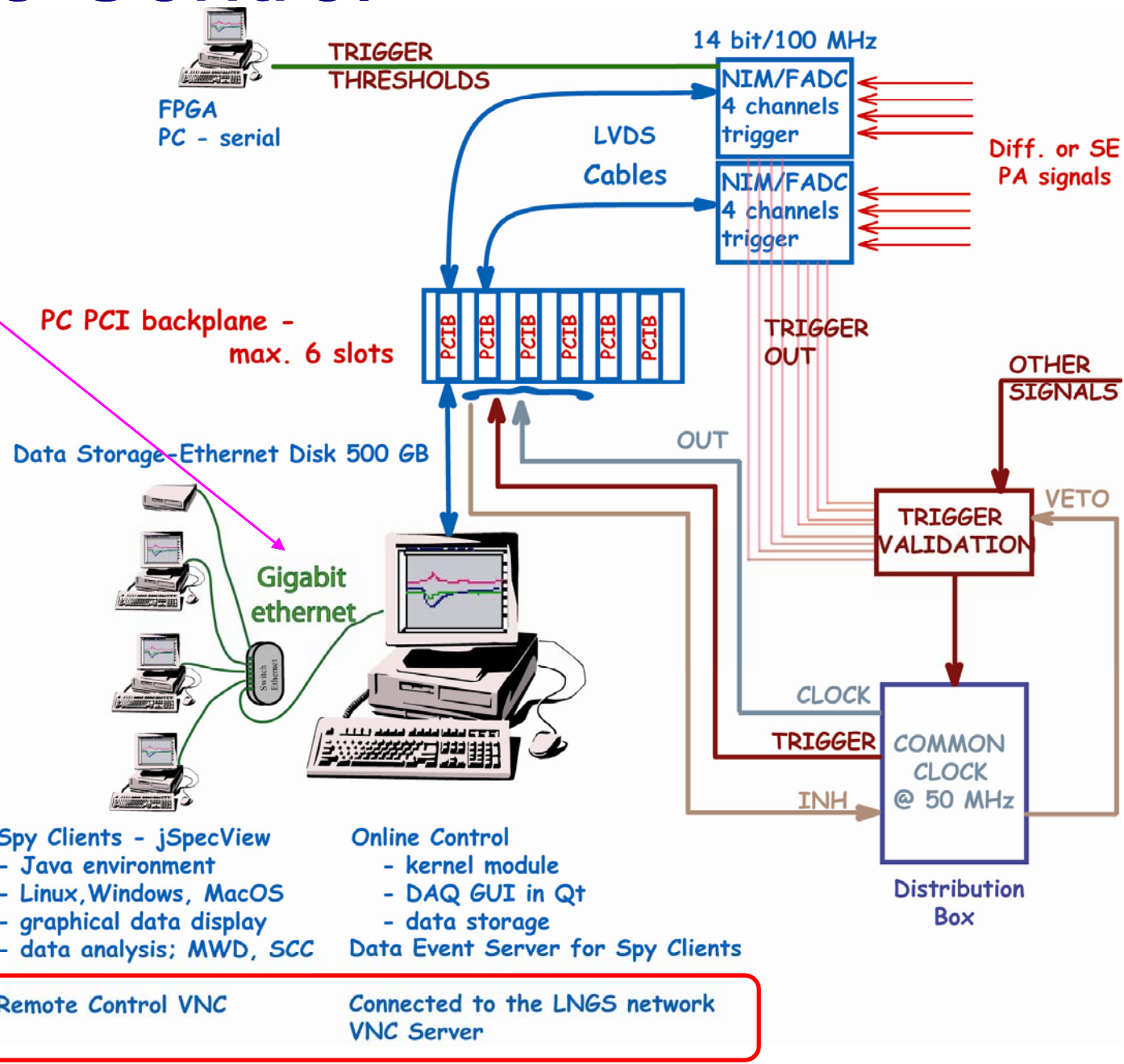
TRIGGER THRESHOLDS

FPGA PC - serial

14 bit/100 MHz

NIM/FADC 4 channels trigger

LVDS Cables

NIM/FADC 4 channels trigger

Diff. or SE PA signals

PC PCI backplane - max. 6 slots

PCIB PCIB PCIB PCIB PCIB PCIB

TRIGGER OUT

OTHER SIGNALS

Data Storage-Ethernet Disk 500 GB

OUT

TRIGGER VALIDATION

VETO

Gigabit ethernet

CLOCK

TRIGGER

COMMON CLOCK @ 50 MHz

INH

Distribution Box

Spy Clients - jSpecView
- Java environment
- Linux, Windows, MacOS
- graphical data display
- data analysis; MWD, SCC

Online Control
- kernel module
- DAQ GUI in Qt
- data storage
Data Event Server for Spy Clients

Remote Control VNC   Connected to the LNGS network
                          VNC Server

Work in Progress

- implement the hardware modification for the trigger

- thorough tests of the newly implemented features

- adjust the analog conditioning for the FE electronics
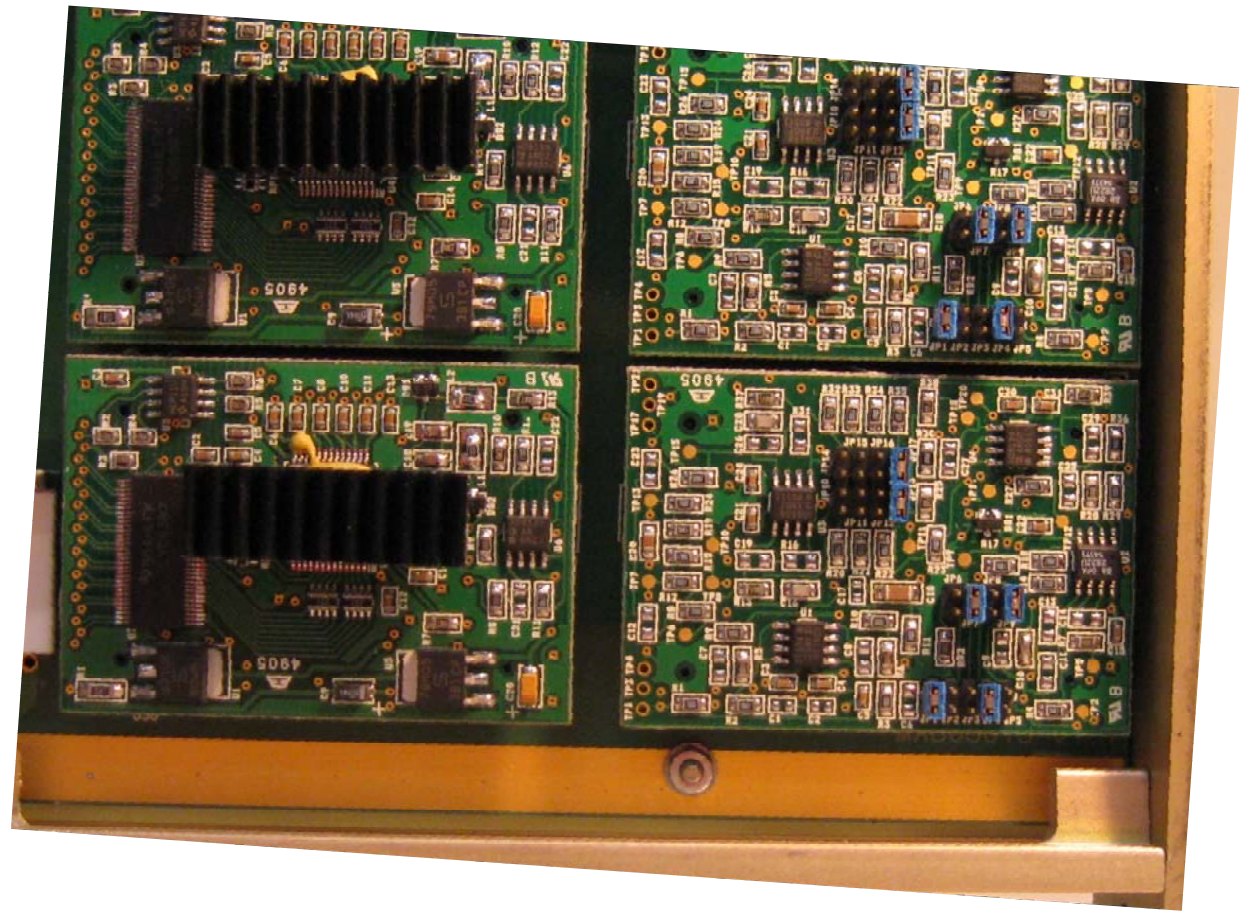
Collaborators

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