First Results from F-CSA104 »Gullinbursti«

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fbe ASIC Design and Consulting

Outline

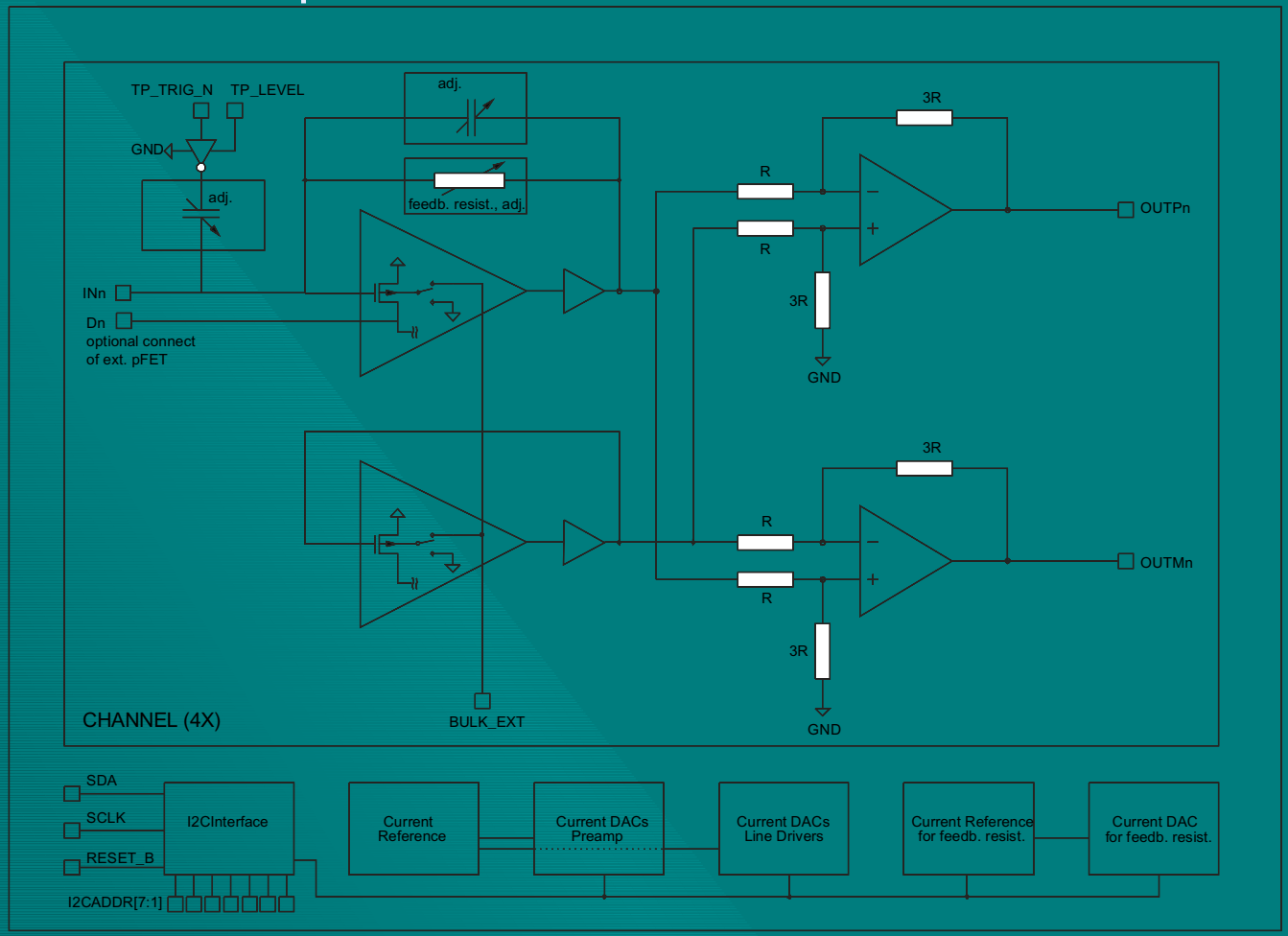
- Overview
  - Requirements
  - Schematics
  - Layout
- Tests and Results
  - Setup and Infrastructure
  - I^2C
  - Power Consumption and Ref. CS
  - Pulse Shape
  - Linearity
  - Noise
  - Long Cables
- Summary & Conclusions

Requirements

- Very low Noise (*ENC*=220e$^-$ @ C_{det}= 30pF, T=27°C, t_{peak}=20µs)
- Temperature Range -200°C...+50°C
- Fast differential Outputs (t_{rise}<30ns)
- Gain 5.84mV/fC, 316mV/MeV (Ge), 258mV/MeV (Si)
- Input Signal Range ±600fC, ±11MeV(Ge), ±13MeV(Si)
- 14bit Linearity for Spectroscopy Applications
- Adjustable Preamplifier Time Constant 1µs...1.5ms
- Optional Connection of external p-Channel FET
- Optimised for Detectors of 30pF (0...100pF)
- All Stages DC coupled, Offset Suppression
- I^2C-Interface for Parameter Adjustment

Schematics

- F-CSA104 Top-Level Schematic

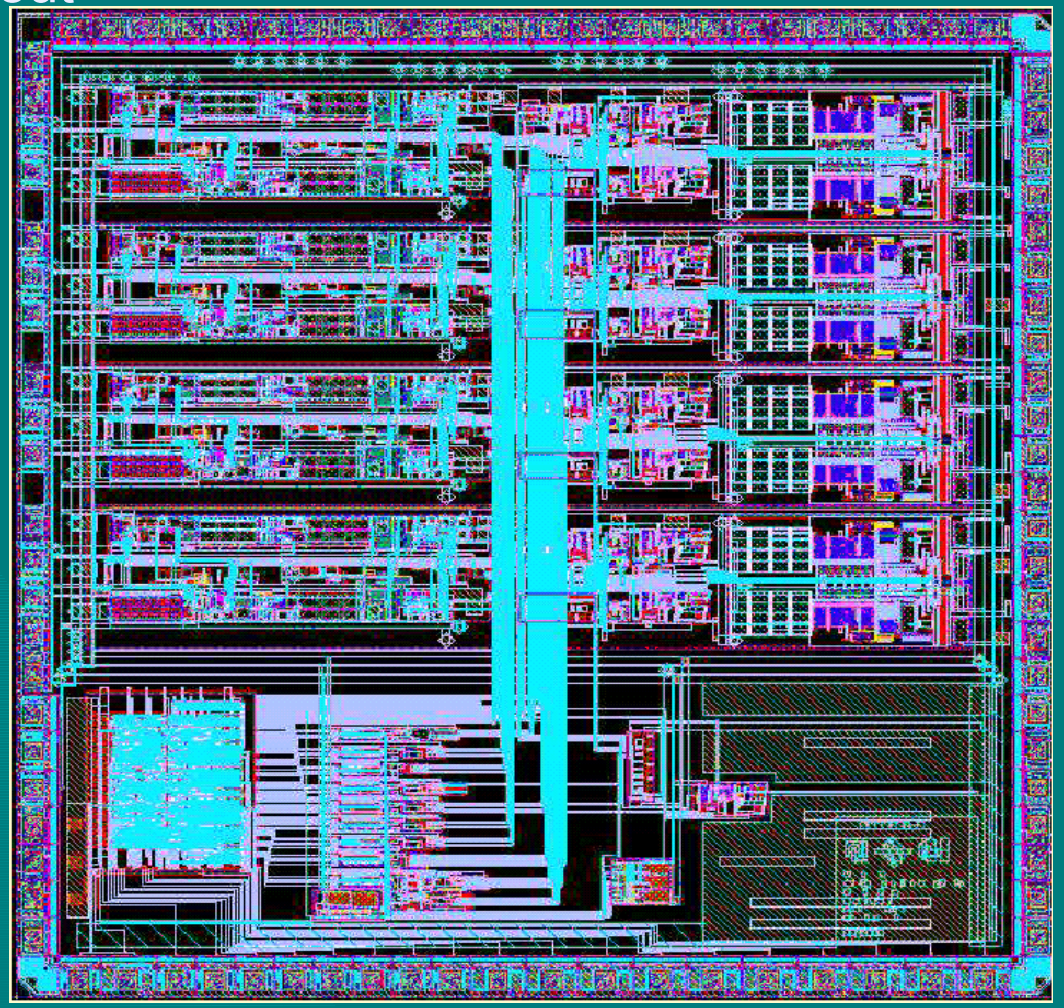


Layout

- F-CSA104 Chip Layout

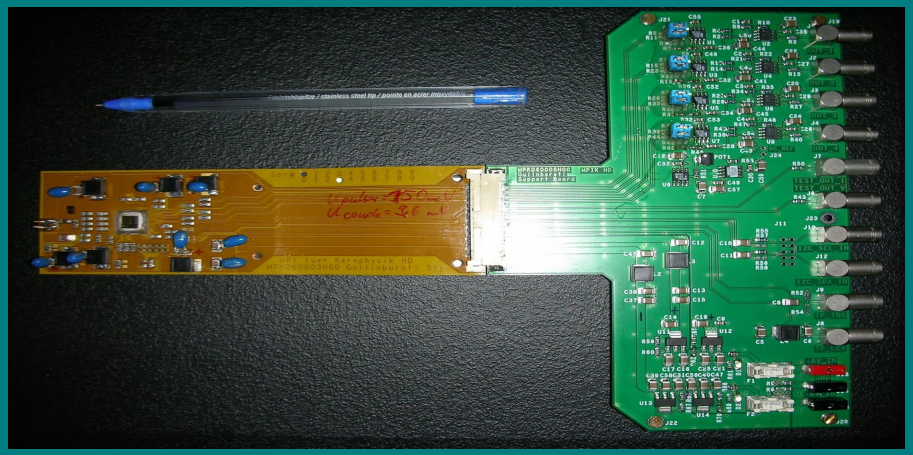
Reference Channel 1	Diff. Output Driver
Channel 1	
Reference Channel 2	Diff. Output Driver
Channel 2	
Reference Channel 3	Diff. Output Driver
Channel 3	
Reference Channel 4	Diff. Output Driver
Channel 4	

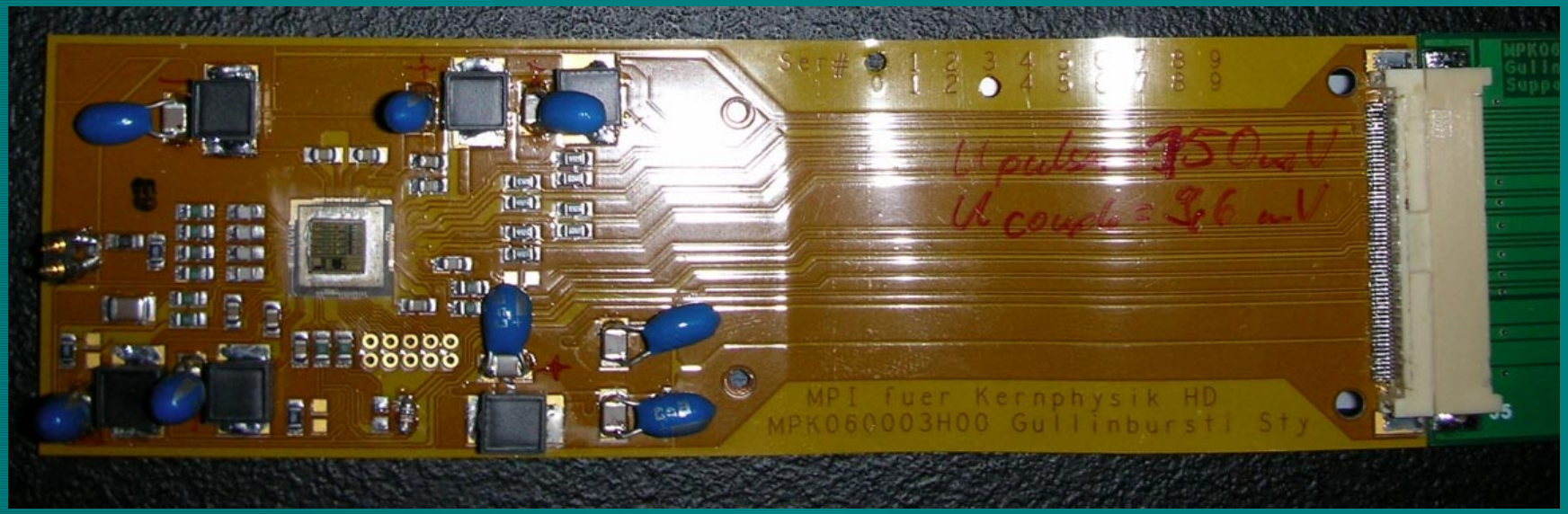
I^2C-Inter-face	Bias-Gen.	Test-Mux



Test Setup

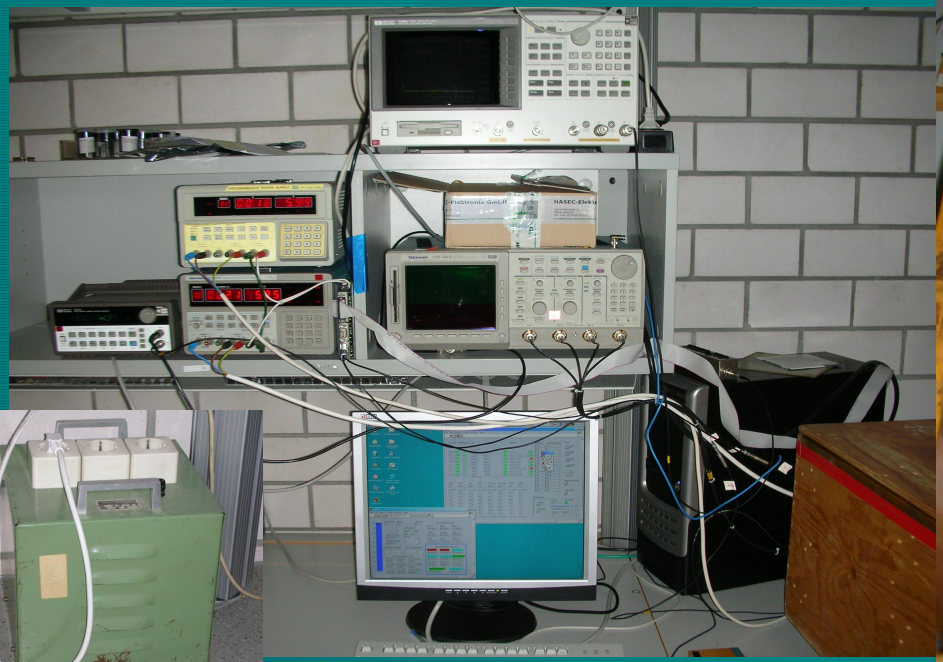
- F-CSA104 Board
- Differential Receiver
- CR-$(RC)^4$-Shaper





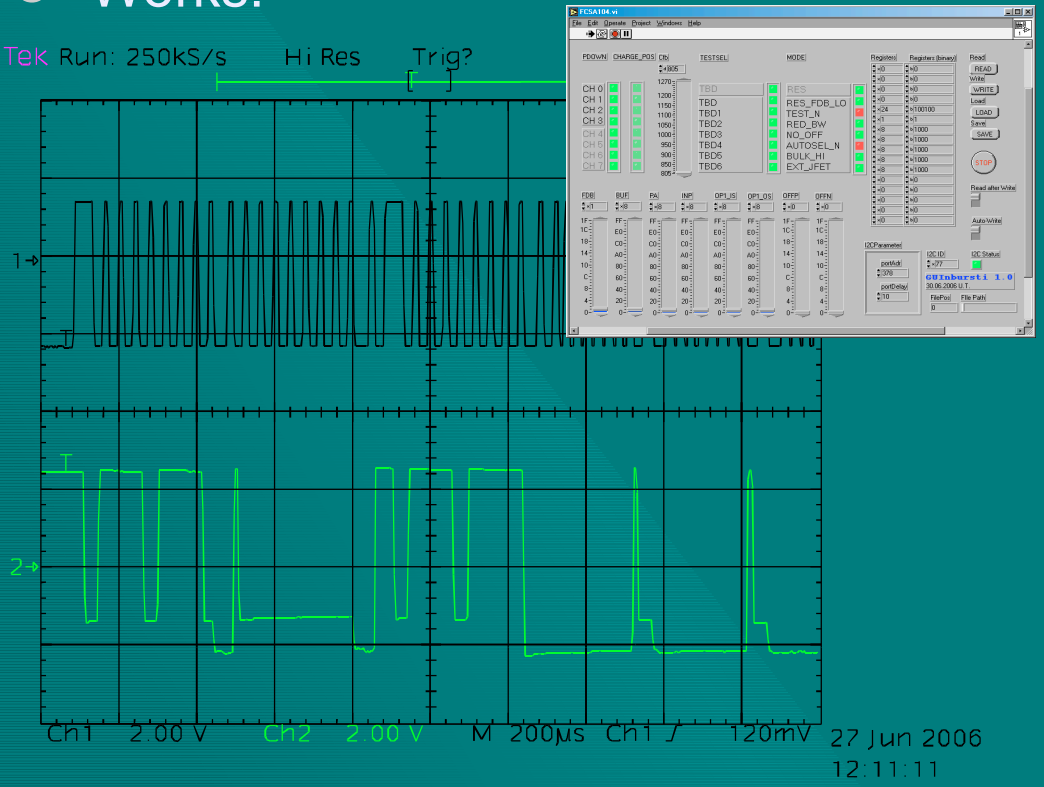
Test Setup

- Isolation Transformer
- Shielding Box
- Spectrum Analyser
- TDS784D Scope
- PC



I²C-Interface

- Requires Levelshifter (0-5V -> ±2.5V)
- Register Map »off-by-one«
- Works!



Register Name	Register Address		Default Value
	Sim.	Exp.	
		0x00	0x00
PDOWN	0x00	0x01	0x00
CFB	0x01	0x02	0x0D
TESTSEL	0x02	0x03	0x06
MODE	0x03	0x04	0x05
FDB	0x04	0x05	0x08
BUF	0x05	0x06	0x08
PA	0x06	0x07	0x08
INP	0x07	0x08	0x08
OP1_IS	0x08	0x09	0x08
OP1_OS	0x09	0x0A	0x08
RESERVED	0x0A	0x0B	0x00
RESERVED	0x0B	0x0C	0x00
OFFP	0x0C	0x0D	0x00
OFFN	0x0D	0x0E	0x00
CHARGE PO	0x0E	0x1F	0x00
	0x1F	0x10	0x10
	0x10	0x11	0x11
	...	...	...
	0xFE	0xFF	0xFF
	0xFF		

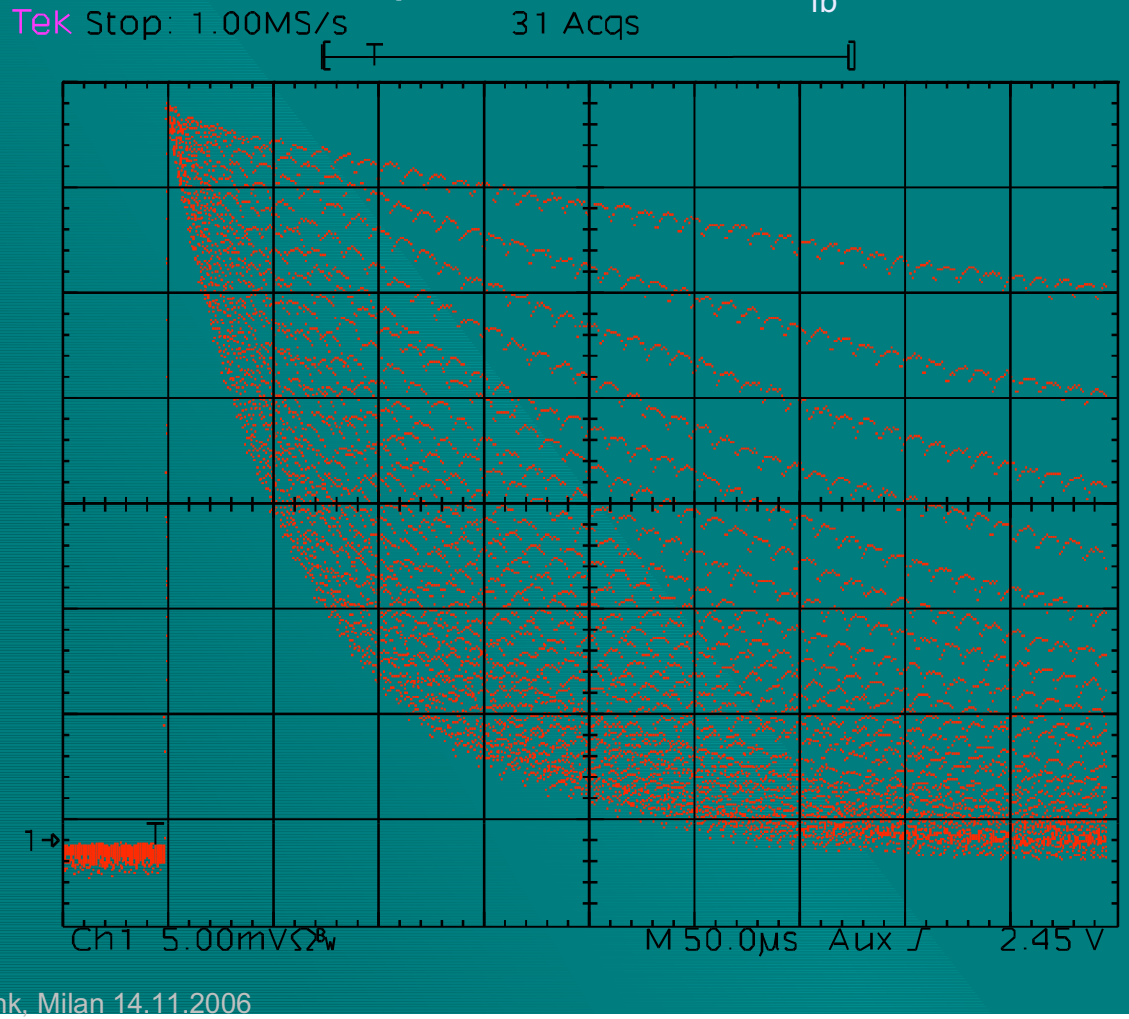
Power Consumption

- Higher than Simulation (w/o Pads and I^2C)
- Channel Power very uniform
  - Almost no Difference between 300K and 77K
  - Due to Ref. Current Source (Sim: 28ppm/°C)

	Measured				sim.
	77K		300K		
	Vdd	Vss	Vdd	Vss	Vdd
4 channels	65mA	75mA	73mA	79mA	60.0mA
3 channels	55mA	64mA	62mA	67mA	50.5mA
2 channels	45mA	53mA	51mA	55mA	41.0mA
1 channel	35mA	42mA	43mA	45mA	31.5mA
0 channels	25mA	30mA	33mA	35mA	22.0mA

Pulse Shape

- Pulse Shape for different R_{fb} Values

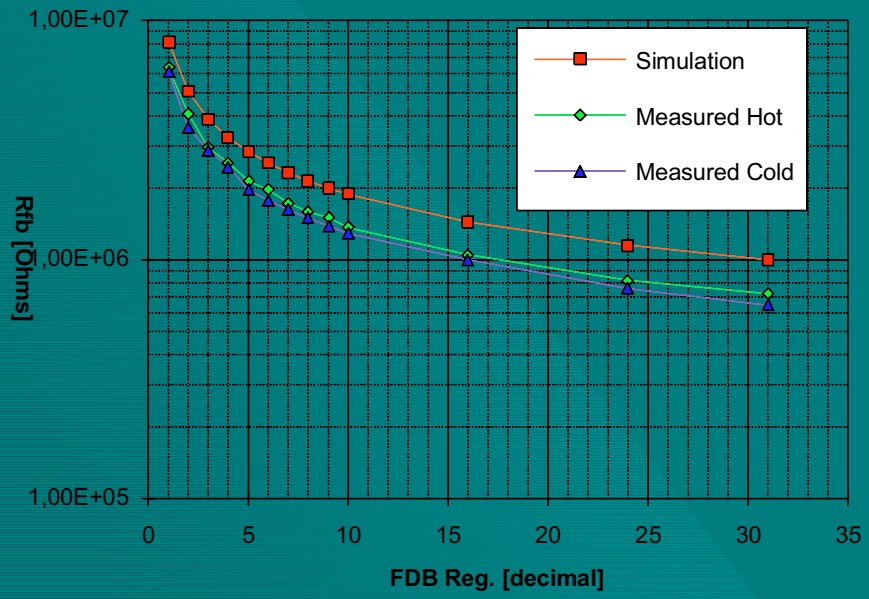


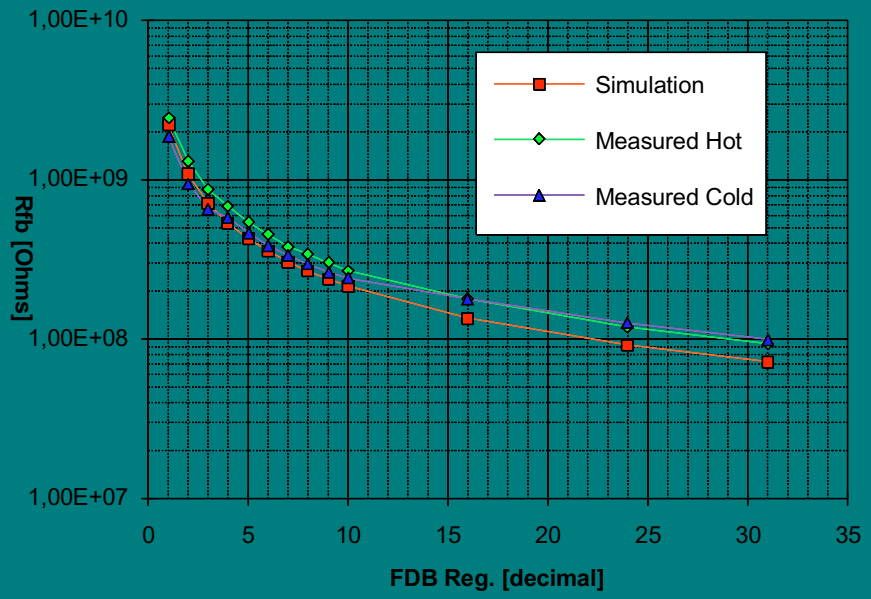
Cp	33 pF	100pF
trise (77 K)	10 ns	12 ns
trise (300K)	18 ns	24 ns
trise (sim., 300K)a	22 ns(b)	28 ns(c)

(a) with Cp = 0
(b) Qin = 40fC
(c) Q = 541 fC (1MeV (Ge))

Pulse Shape

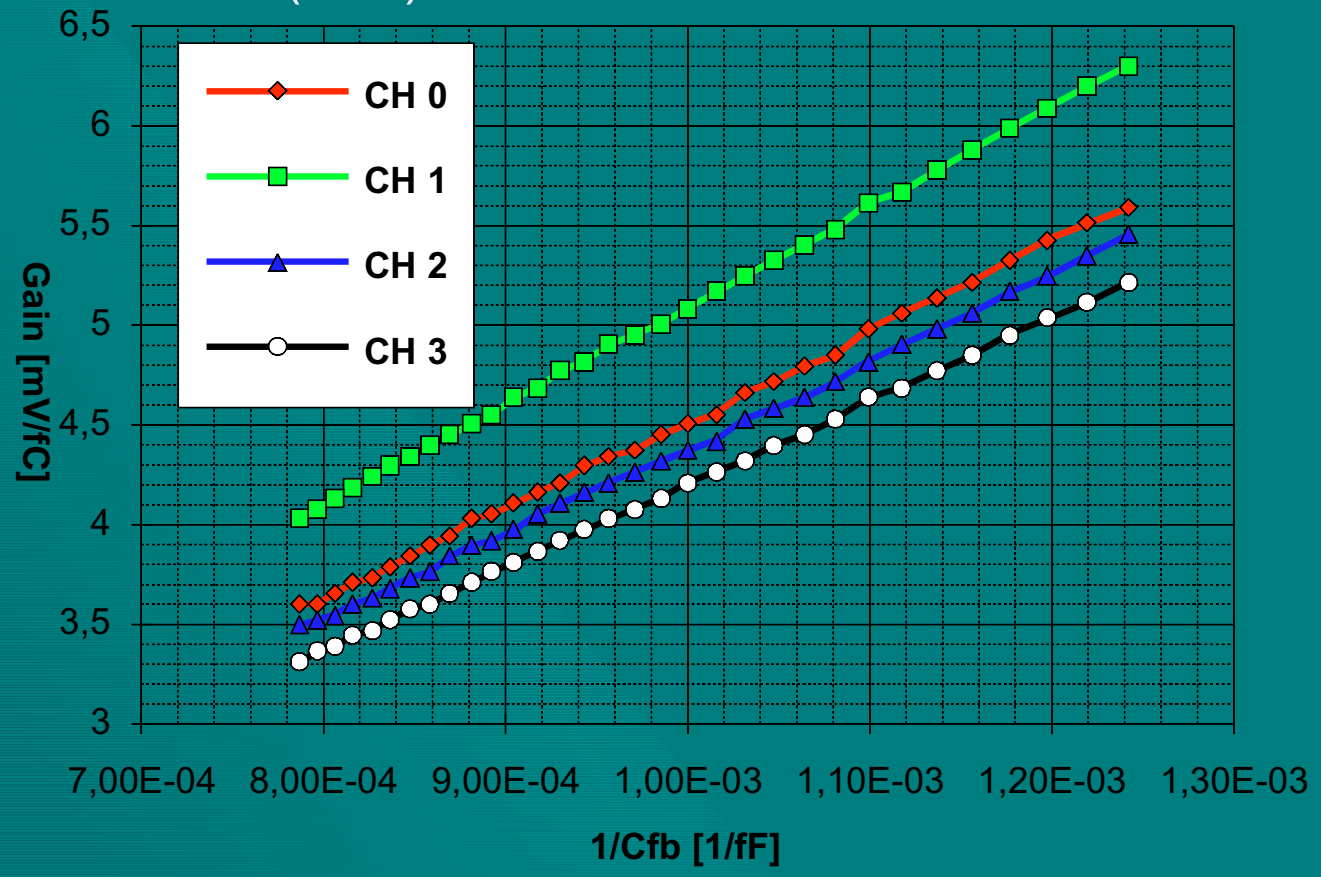
- R_{fb} Values from measured Decay Times





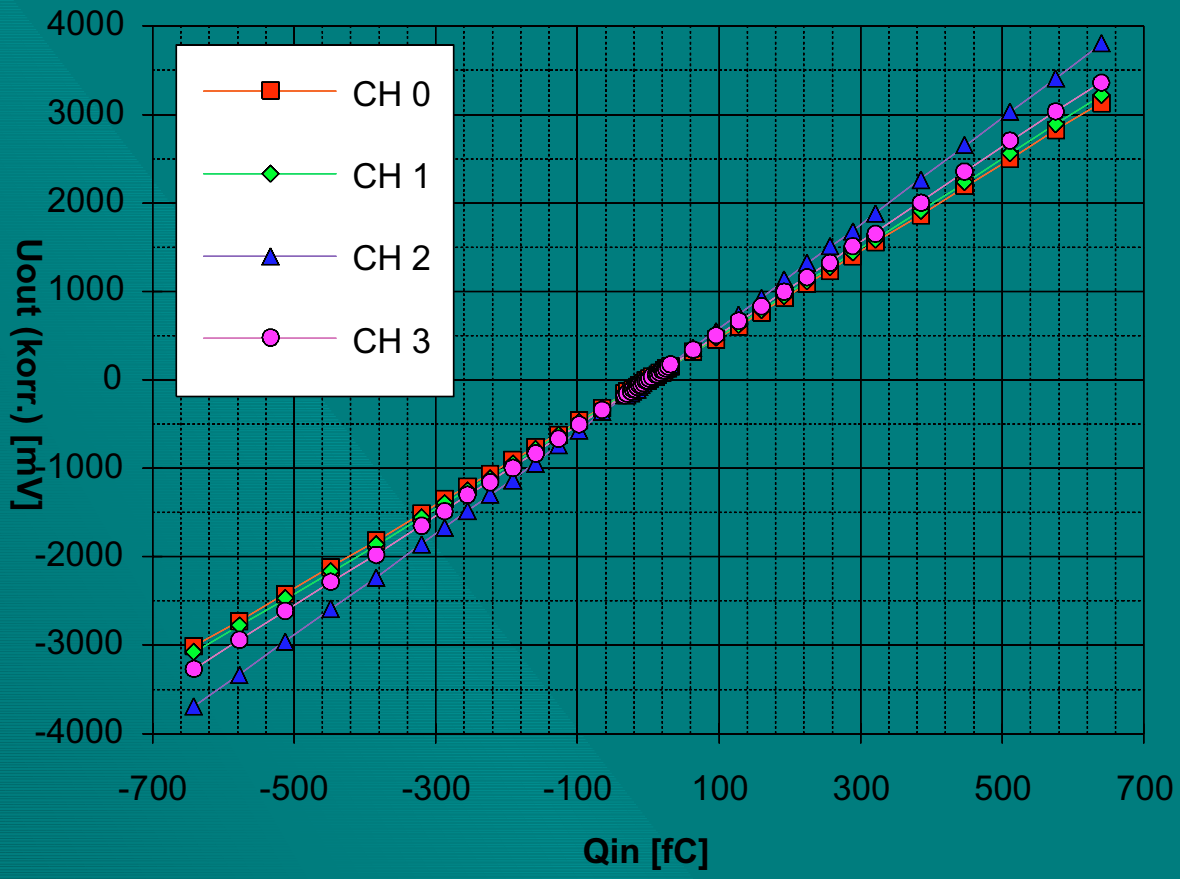
Gain

- Less than expected:
  - 4.7 mV/fC (meas.)
  - 5.84mV/fC (sim.)



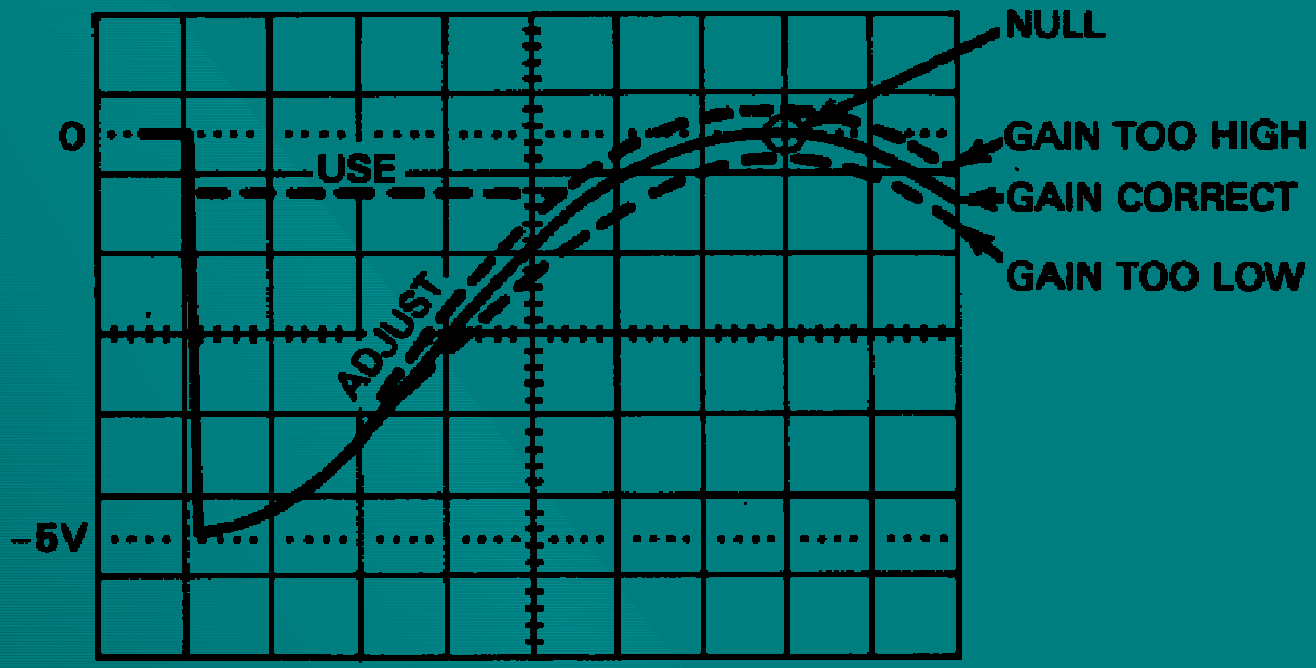
Linearity

- 14bit Equivalent



Linearity

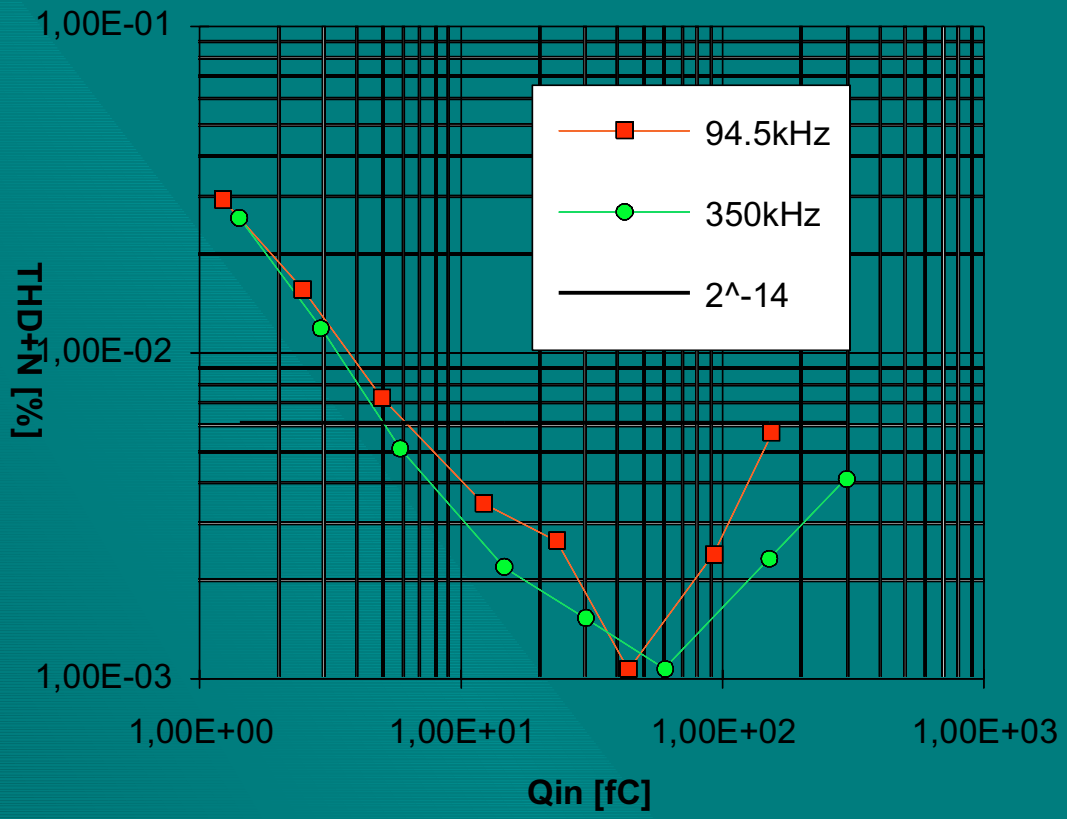
- IEEE Std. 301-1988
  - $\Delta U \approx 150 \mu V$
  - Requirements for Error Amp (G=100 @ BW>10MHz)



Linearity

- THD+N Method
  - Only upper Limit
  - Shift in Operating Point
  - Frequency dependent

$$NL \leq THD + N = \sum_{i=2}^{\infty} \frac{k_i}{k_1}$$



Noise

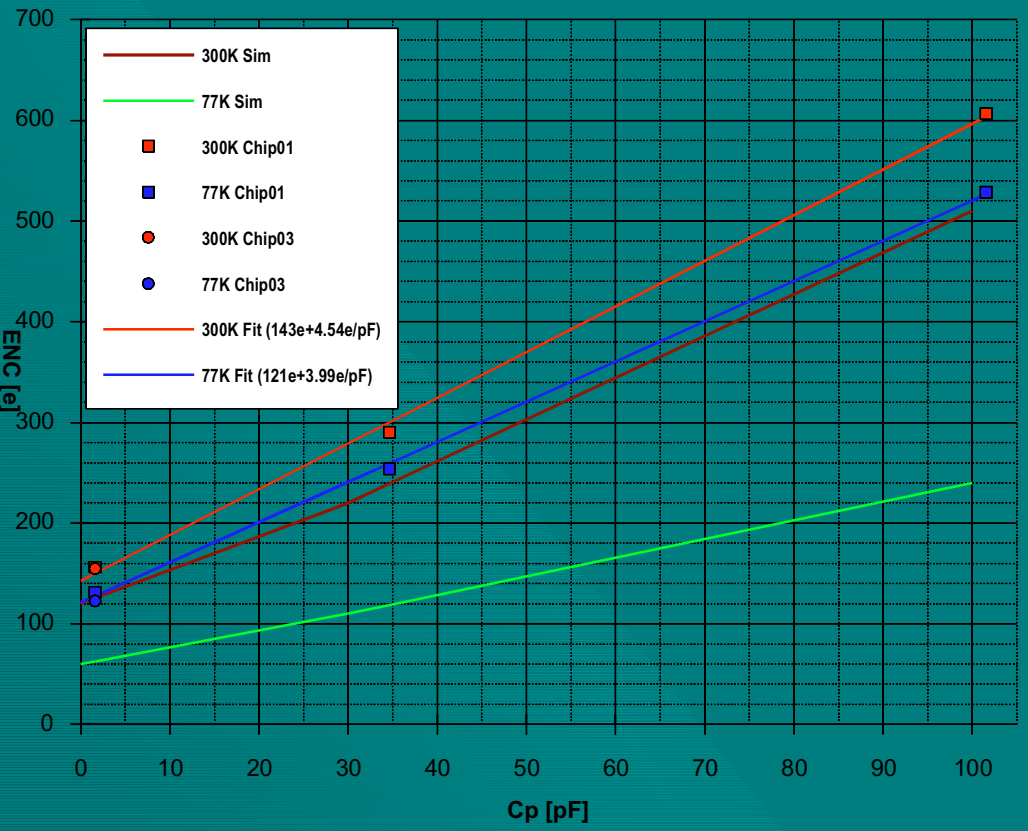
- Measurement Setup:
- CR-(RC)^4-Shaper t_{peak}=20µs, TDS784D Scope & LabVIEW
- 100Acq × 5k Samples @ 2.5Ms/s = 250Hz...1.25MHz
- TDS built-in RMS and MEAN Functions
- Struck 100MHz/14bit VME FADC
- Software for Shaping and Analysis
- Comparable Results
- Huge Common Mode

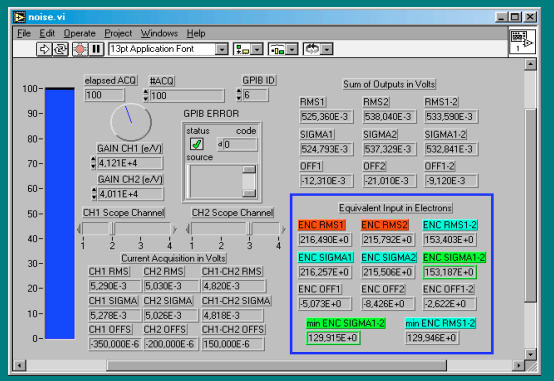
	300K	77K
1.5pF	218e	193e
34.5pF	741e	521e
101.5pF	1900e	1212e

ENC=194e^-+ 16.33e^-/pF @ 300K
ENC=177e^- + 10.52e^-/pF @ 77K

Noise

- ENC=ENC(ChA-CHB)/√2

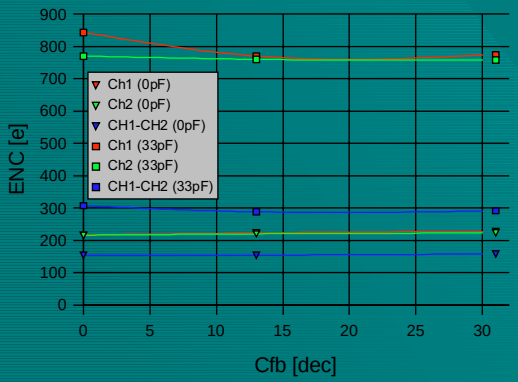


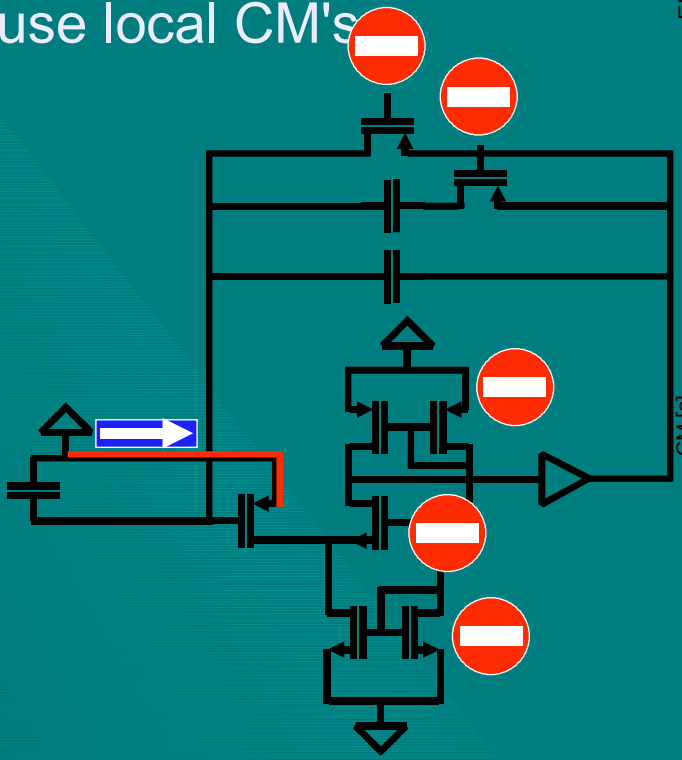


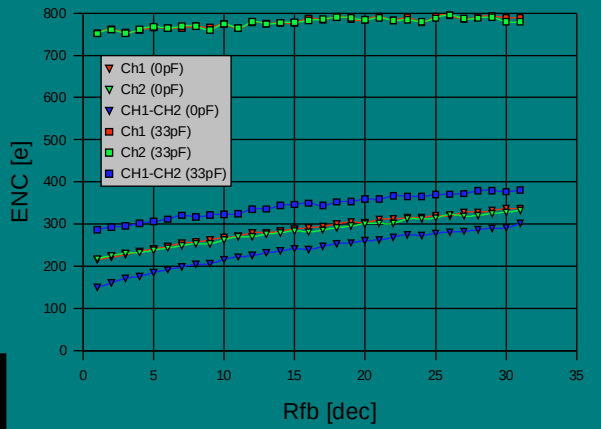
		Offset	Slope
300K	sim.	120e	3.62e/pF
	meas.	143e	4.54e/pF
77K	sim.	60e	1.73e/pF
	meas.	121e	3.99e/pF

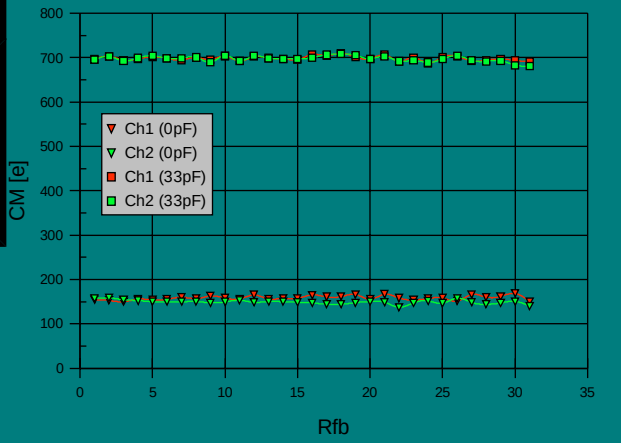
Search for a Correlated Noise Source

- 3 Sensitive Nodes
  - R_{fb}-Gate Voltage
  - C_{fb}-Switches
  - Input FET Source Node
- 2 other Nodes use local CM's



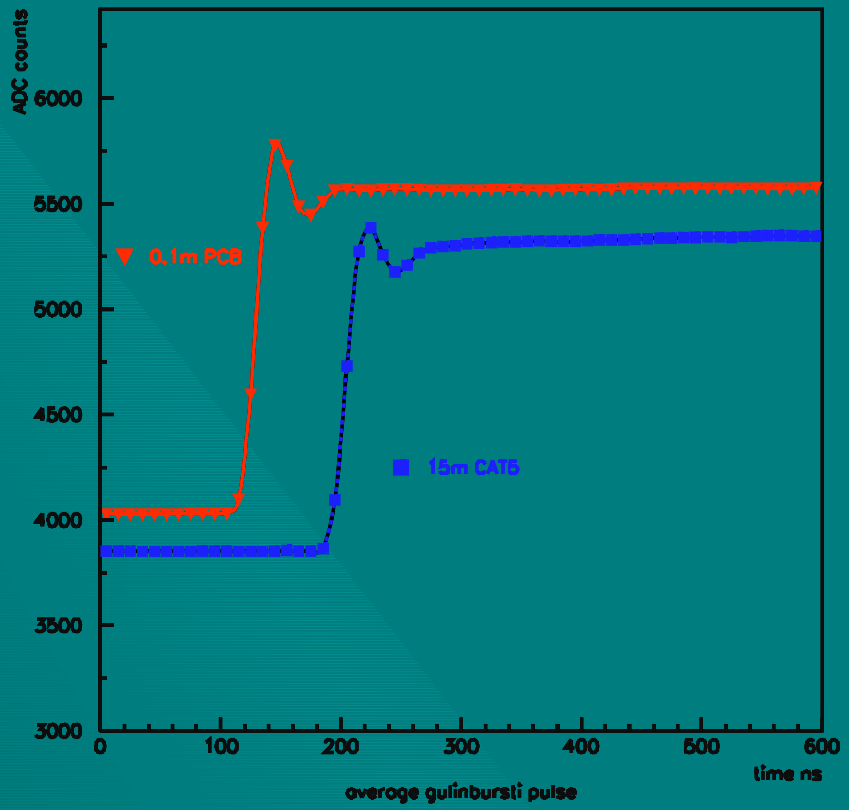






Long Cables

- 15m CAT5 Cable
- 50Ω series Termination, 100Ω parallel Termination
- 1.2% Attenuation
- No Change in Rise-Time or Noise



Summary & Conclusions

- ✔ F-CSA104 works!
- ✔ Can drive 15m TP Cable
- ✔ works at 77K
- ✔ stable Adjustment of R_{fb} and Bias (at 300K and 77K)
- ✔ Linearity better than 14bit Equivalent
- ● Excess Noise at Room Temperature: 18% (30%)
- ✗ Noise improves by 18% (11%) instead of 50% at 77K
- ✗ huge Common Mode

Next Steps depend on.....

- Simulation Results at MPI
- Noise of Setup with new PCB
- Clues on the Correlated Noise Source