# Cold FE for prototype crystal operation at LARGE

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• The FE preamplifier based on monolithic JFET IPA4 chip

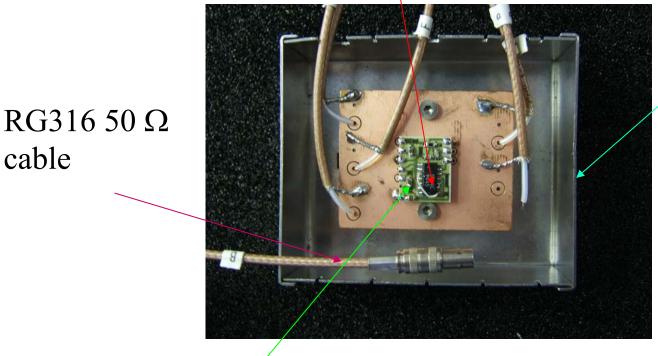
- The new PCB for crystal operation

- Status of tests at LARGE site
- INFO on
  - HV flanges
  - HV cables
  - Signal cables
- Construction of a new dewar + insertion lock system for electronic tests at LNGS

~ 2 V/pC with C <sub>f</sub> = 0.5 pF $\rightarrow$ 108 mV/1 MeV in Ge
75 dB $-$ 60 dB (depending on the adopted configuration)
9.7 mA/V
1820 μm, 15 μm
$1.52 \text{ nV/Hz}^{1/2}$
9 pF
400 ns with $C_f = 0.5 \text{ pF}$
Single ended. Do not drive 50 $\Omega$ load.
ion $\sim 100 \text{ mW}$
positive and Negative
+12 V, -6 V

### The monolithic N-JFET preamplifier

Developed in the '90s in a joint reasearch project between BNL, Italian MURST and INFN, for LAr, LKr calorimetry.



Shielding box

The IPA4 polarization circuit.

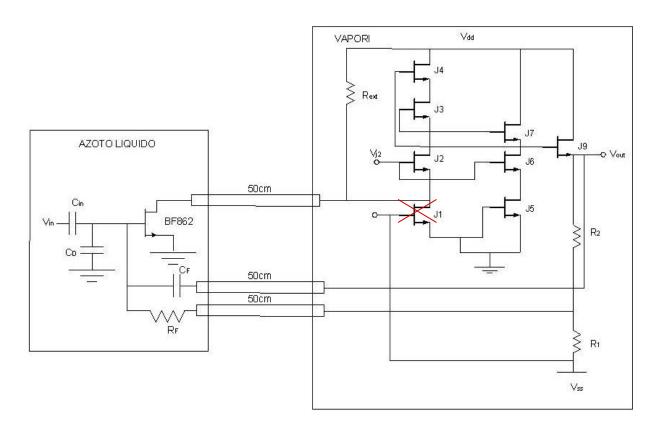
V. Re, co-author of the IPA4 circuit, provided us several

IPA4 chip in SOIC plastic case + 1 polarization board, and several useful discussions.

cable

IPA4+external FET BF862: J1 ( $g_m = 9.7 \text{ mA/V}$ ) is blocked and substituted by external BF862 ( $g_m = 30 \text{ mA/V}$  which can

be kept at 0- 60 cm from the CSA amplifying circuit



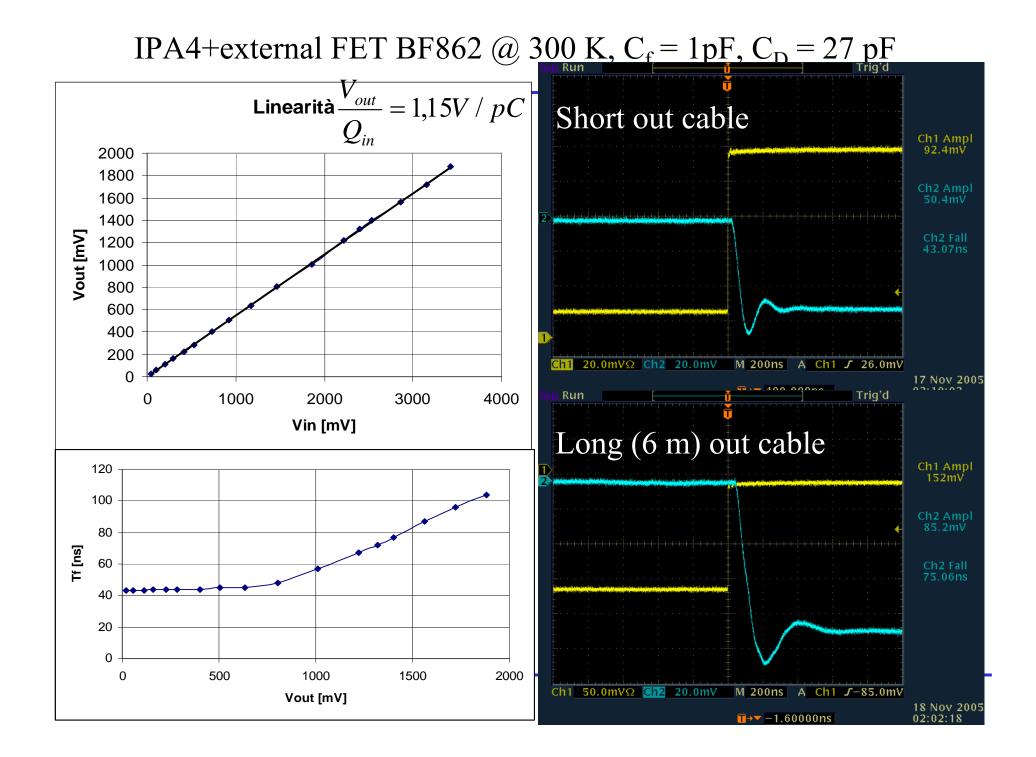
## Comparison of pulse fall time for IPA4 with internal and external FET.

CD [pF]	τf [ns] (BF862)	τf [ns] (J1)
0	27	110
15	36	140
27	44	155

$$\tau_f = C_T \, \frac{C}{C_F \times g_m}$$

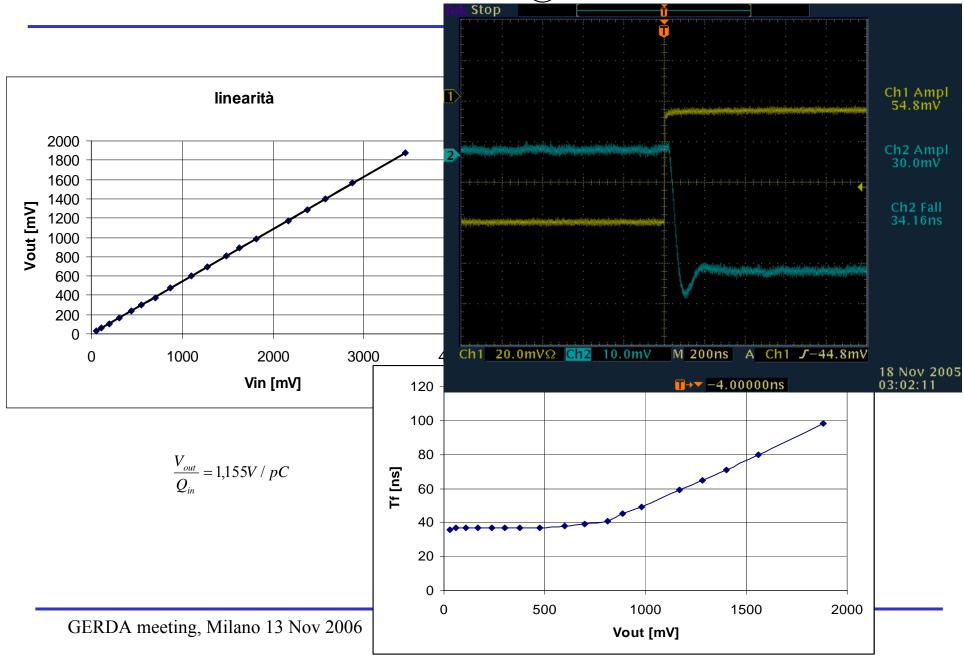
 $g_{\rm m} J1 (I_{\rm ds} \sim 2.6 \text{ mA}) = 9.7 \text{ mS}$ 

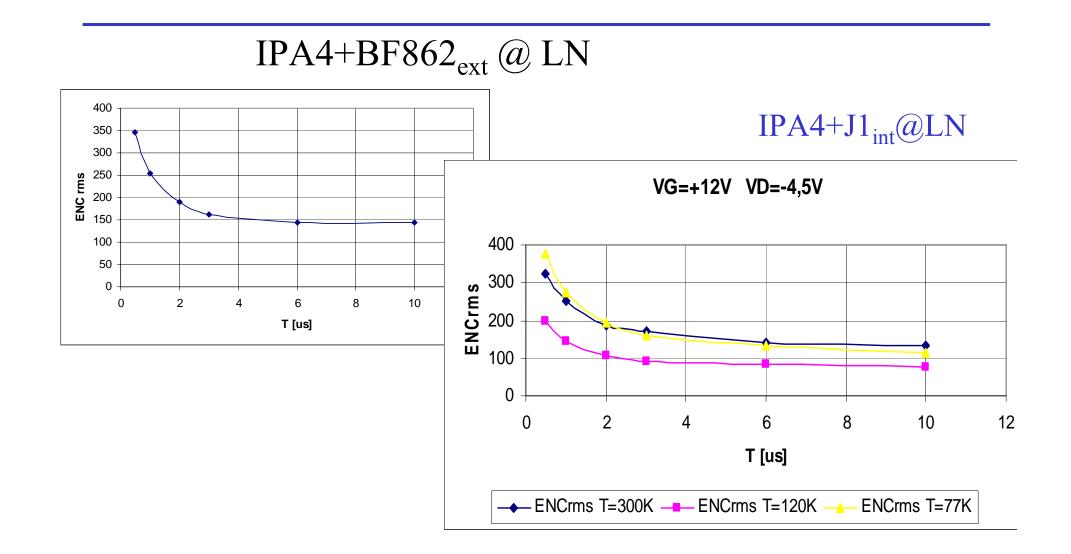
 $g_{\rm m} BF862 (I_{\rm ds} \sim 3 \text{ mA}) = 30 \text{ mS}$ 



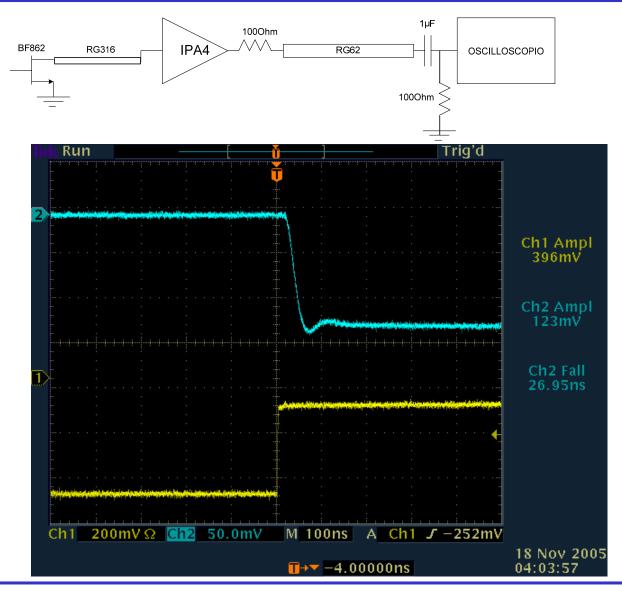
 $\frac{V_{out}}{Q_{in}} = 1,155V / pC$ 

IPA4+BF862 @ LN





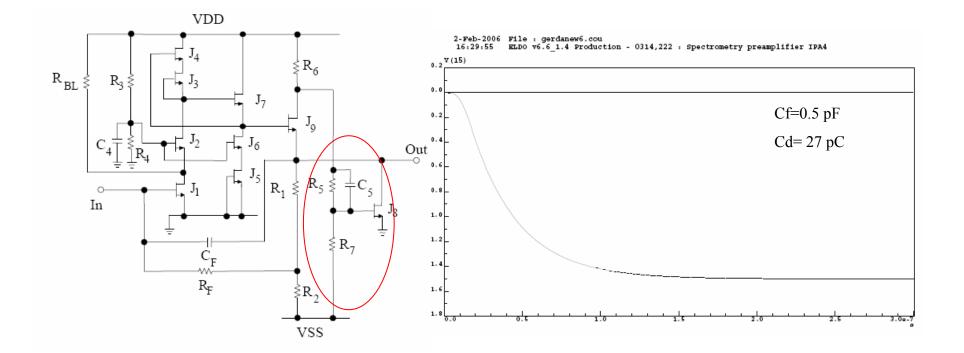
#### IPA4+external FET BF862 @ 300 K: adapted to 100 Ohm



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#### IPA4 + $J1_{ext}$ + 100 Out stage: simulated pulse 50 ns fall time (@ 300 K).



Swing to -1.5 V

IPA4 +  $J1_{ext}$  + 100  $\Omega$  Out stage: the new test board.

Results: Obtained pulse shape not as expected, 2 slopes

New setup for LN measurements

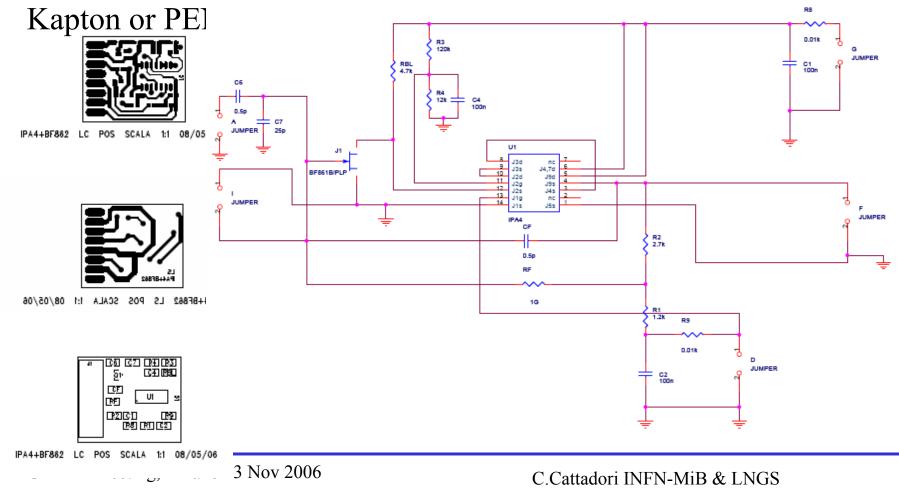


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Production of 25 FE cryogenics circuits (based on IPA4 JFET monolithic circuit) for LNGS Phase I detector tests and MU

18 fold segmented prototype

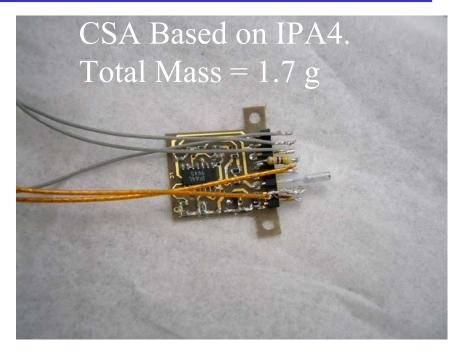
Production of PCB: 23 june at AREL, without 100  $\Omega$  output stage. PCB in DICLAD 880, 0.25 mm thick. Can be done in



#### The tested CSA

- PCB: DICLAD 880 0.25mm thick (MPCB= 0.57 g)
- IPA4 Chip in plastic SOIC14 case (MIPA4= 0.13 g)
- 9 HF pins for HF connection (Mpins = 0.45 g)

No 50Ω cold driving stage.
On top of flange warm second
stage based on LM6624 or
LM7171 (to match with FADC input impedence) , or directly to
spectroscopy amplifier



Result: CSA not connected to crystal, connected to flange through cables (70 cm long), + PSA.

### Results of measurements of CSA based on IPA4 mounted on copper cross suspension

- Measuring conditions as with crystal connected
  - HV off
  - Crystal disconnected
  - CSA connected to flange through cables (70 cm long)
  - PSA (semi-Gaussion ORTEG mod. 572) + ADC + MCA

	Shaping time [µs]	FWHM		E
		[keV]	Rel [%]	
	0.5	1.51	0.121	1244.85
	1.0	1.07	0.08	1337.6
)	2	0.98	0.07	1392.85
Ċ	3	1	0.071	1404.72
<	6	1.07	0.076	1411.17
	10	1.2	0.089	1439.03

Conclusion: Minimun of ENC found at 3 ms for CD = 0 pF, FWHM = 1 keV @ 1.404 MeV  $\rightarrow$  agreement with previous measurements

#### The tested setup (August 2006)

Discharge problems on
filter (warm) due to construction
technology → solved
HV connector in Ar gas due to

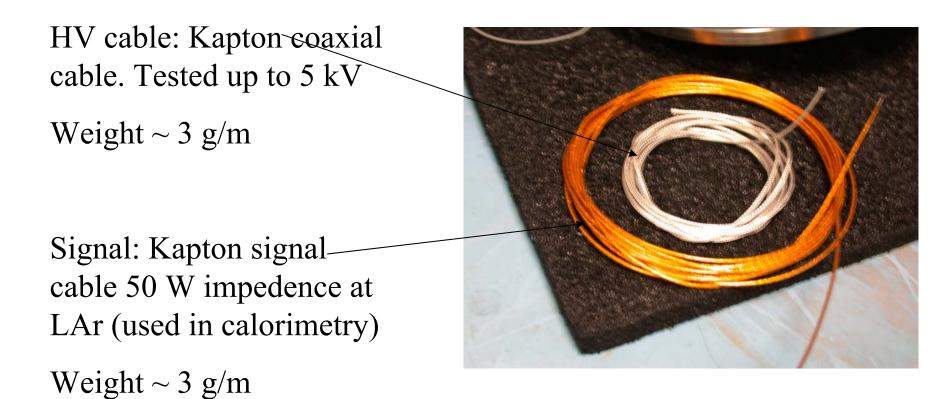
proximity of HV to ground and low break-down of gas Ar  $\rightarrow$  solved by means of Stycast glue poored in the



Teflon insulator subsequently applied The flange for cold CSA

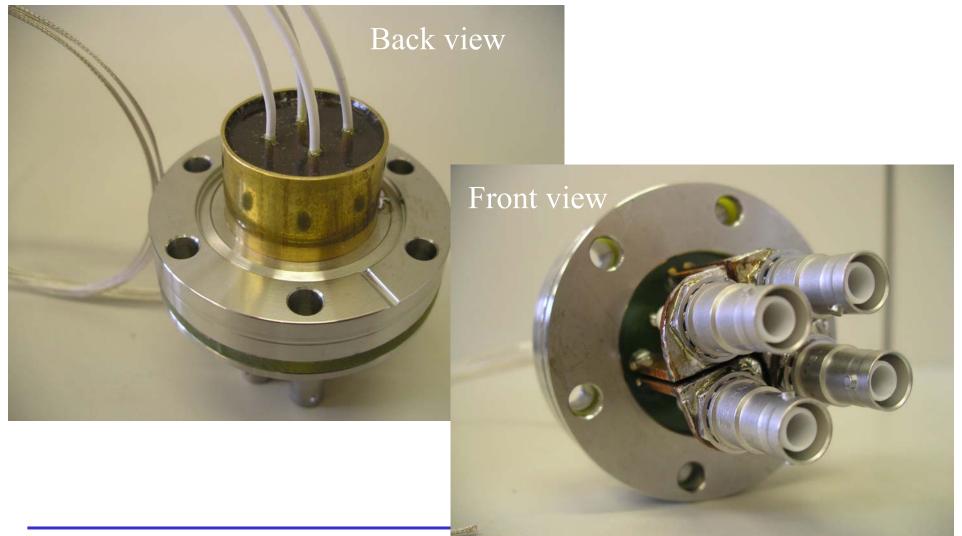


#### Adopted Cables for LARGE tests



Assuming 10 mBq/kg (actual upper limit on  $\gamma$ - meas of Th and U on HV cable)  $\rightarrow$  600  $\mu$ Bq from last meter of cable (nearest to electronic)

# HV flanges against discharges: Developped and patented by INFN PD



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#### Conclusions on IPA4 based CSA and next steps

- CSA based on IPA4 is ready for testing with prototype non enriched crystal at LARGE.
- Performances of sensitivity and bandwidth adequates.
- For PA mounted with crystal mounting
  - ENC rms (@  $C_D=0$ ,  $\tau = 3 \mu s$ ) = 110 e<sup>-</sup> = 0.7 keV FWHM
  - ENC rms (@  $C_D = 33$ ,  $\tau = 3 \mu s$ ) = 170 e<sup>-</sup> = 1.1 keV FWHM
- Flanges and other parts necessary to operate cold FE
  - Flange 1 available 1 new in preparation at LNGS workshop with SHV connectors insulated by teflon + Stycast
  - HV Filter available  $\rightarrow$  OK tested
  - Low noise PS for cold FE  $\rightarrow$  available
- 1 new crystal insertion system + lock in preparation at LNGS to dedicate one test line (1 non-enriched crystal) to test cold FE (ASIC, semi-integrated) in same conditions with crystal connection.

Other possible not ASIC solutions for LARGE Tests (nonenrCrystals) and experimental program with enr Crystals.

Circuits that demonstrated to work

- Mi-ASIC with external feed-back components
- Agata warm preamplifiers with cold FET (minimize and background  $M_{tot}$  <sup>inner electronics</sup> ~ cables), demonstrated to be feasible, superior performances presented 1 year ago and pubblished. (see GERDA Scientific Report Oct 2005)
- AMPTEK A250 + BF862
- Hd J. Kiko preamp.

Test program for comparative analysis of various FE solutions @ same conditions TBD

- Where : LNGS
- When : first time slot: 1-15 december
- What? ..... TBD within TG3

Needs to integrate with ASIC program