GERDA GeDDAQ

Status, operation, integration

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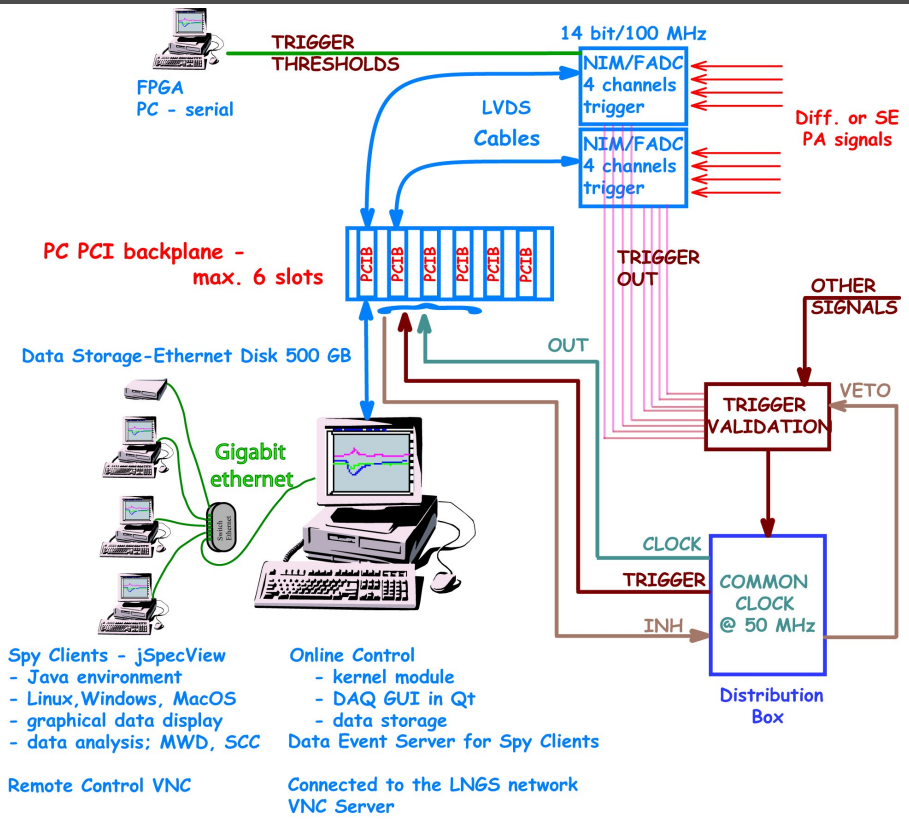
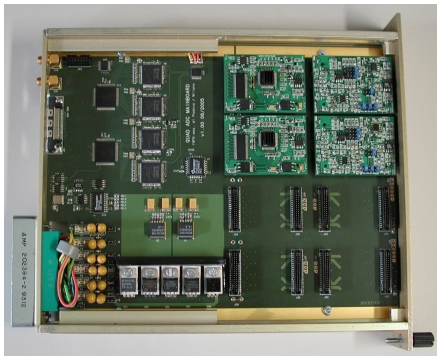
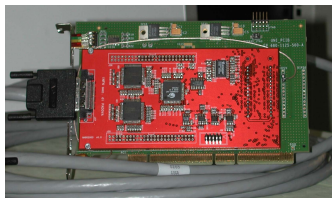
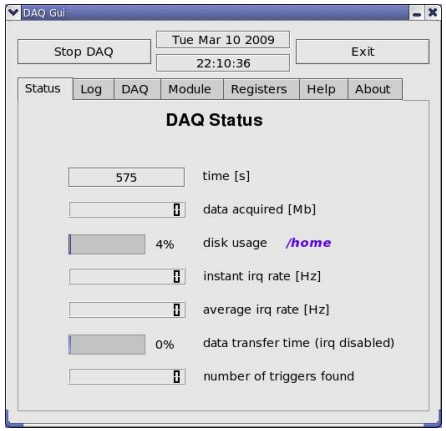
The GeDDAQ System

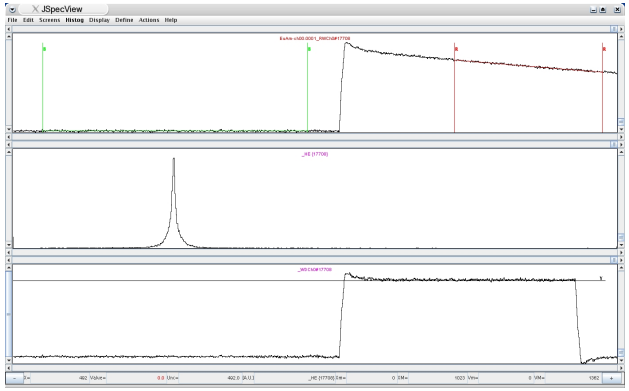


Channels	4/module
FADC bits	14
FADC rate (MHz)	100
Internal trigger	yes
Trace length (samples)	1024 @ 25 MHz 512 @ 100 MHz
Control & i/f	NIM/PCI
Data transfer DMA	PCI 32bit/33MHz
Max output rate (MB/s)	132 (no write) 60 (write)









ChangeLog – new features&fixes

- Implementation of the internal trigger HW/SW
  - firmware Xilinx FPGA on NIM boards
  - modified the NIM boards
  - programming of the thresholds RS232
  - TTL ouput trigger signals
- Implemented the baseline monitor
  - not yet tested
- Stabilized the data transfer in DMA
  - 33MHz PCI
  - revised firmware Altera FPGA – master/slave
- Rewrite the acq. codes
  - more stable
  - faster
  - readable

Internal Trigger

Trigger algorithm (triangular filter)
each channel separately

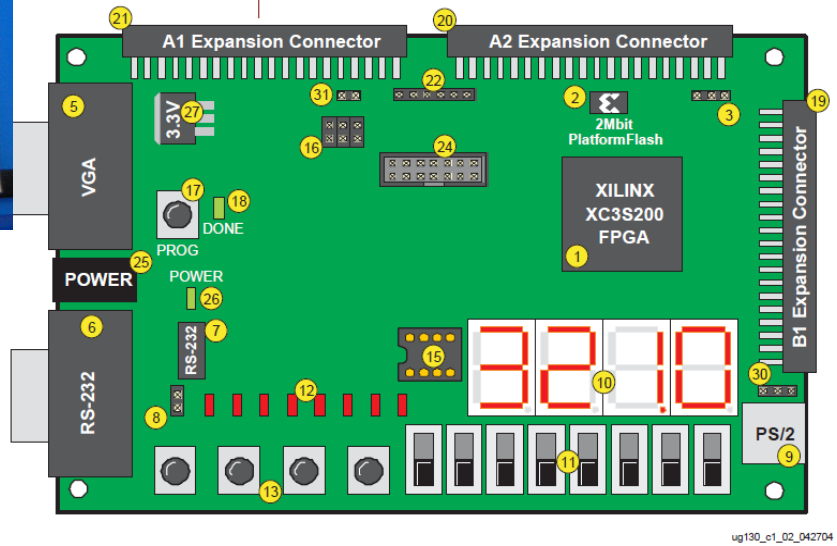
Trigger logic

4 x TTL

or

(to be done)

OR



GUI
(to be done)

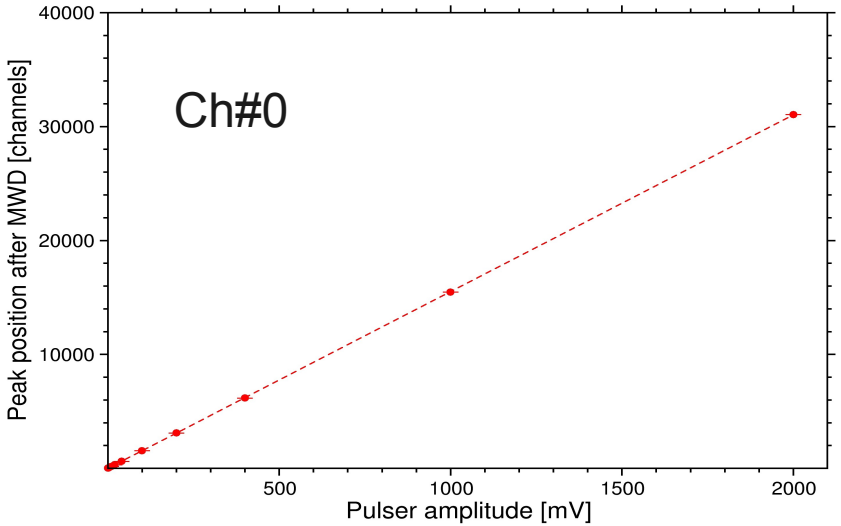
P
C

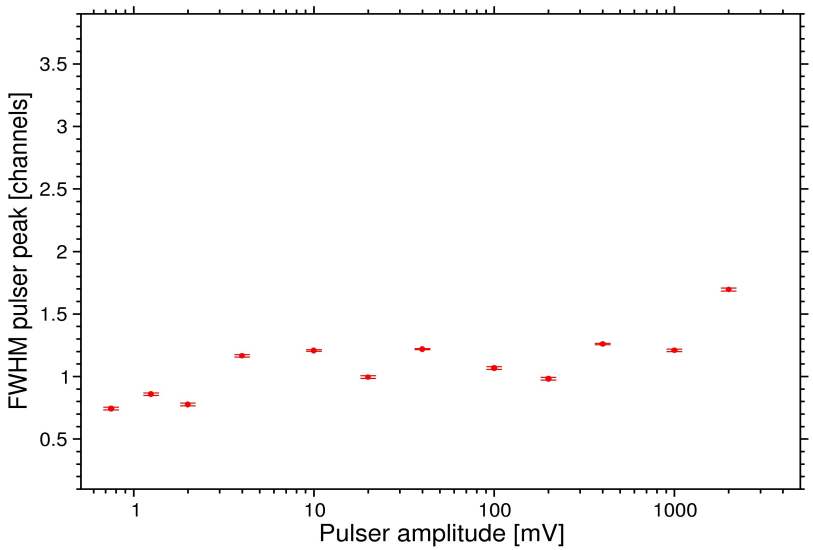
Rx/Tx

Figure 1-2: **Xilinx Spartan-3 Starter Kit Board (Top Side)**

Tests in the Rimessa Lab

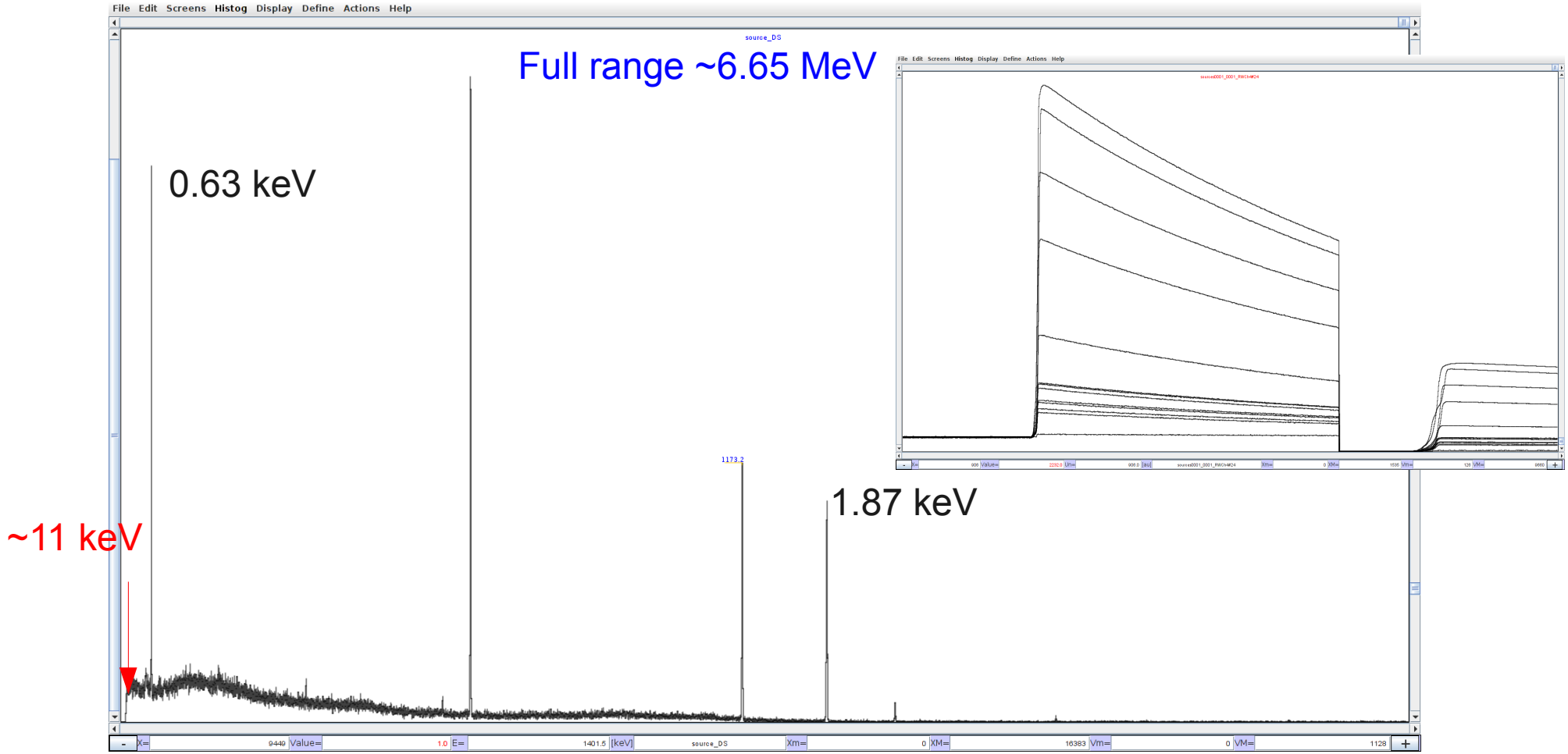
- Tests with pulser – two NIM modules (8 channels)
  - 50 ns rise time, 50 µs decay time
  - variable amplitude
  - trigger 750 µV on a 2V range





Tests in the Rimessa Lab

- Tests with sources (^{60}Co, ^{137}Cs and ^{241}Am)
  - LNGS BEGe detector @ ~1.5 kHz
  - MWD ~7 µs



Data Format

Data are saved on disk
- run number
- files of max. 2 GB length (or a preset value)
- automatic version increment

Each file contains:

```
***************
HEADER  (ASCII)
***************
?PCIDAQ0  data label
?CHN0004  number of enabled channels
?WVN0002  number of waves for each channel (1 or 2)
?P101024  number of bins in the first wave (fixed)
?P200512  number of bins in the second wave
?D103000  how many 10 ns after trigger in the first wave
?D200450  how many 10 ns after trigger in the second wave
?SPR0016  output sample precision in bits
?BIT0014  number of FADC conversion bits
?FRQ0100  sampling frequency in MHz
?LTR0024  event trailer length in bytes
?CH10002  channel #1 Enable Pattern 0000000010
.........(channel #1 of card #2 is enabled; card #1 is LSB)
?CH20000  channel #2 Enable Pattern 0000000000
.........(no channels #2 enabled)
?CH30001  channel #3 Enable Pattern 0000000001
.........(channel #3 of card #1 is enabled)
?CH40002  channel #4 Enable Pattern 0000000011
.........(channel #4 of card #2 is enabled
?JHZ0100  frequency of jiffies (100 Hz) depends on the OS
?RUN0007  run number
?ORIGDAT  original data
?U000029  user comment length (in bytes)
"Data Conmment with User Comment Text"
"new lines"
"..............." up to 512 characters
?ENDHEAD end of header
```

Data Format

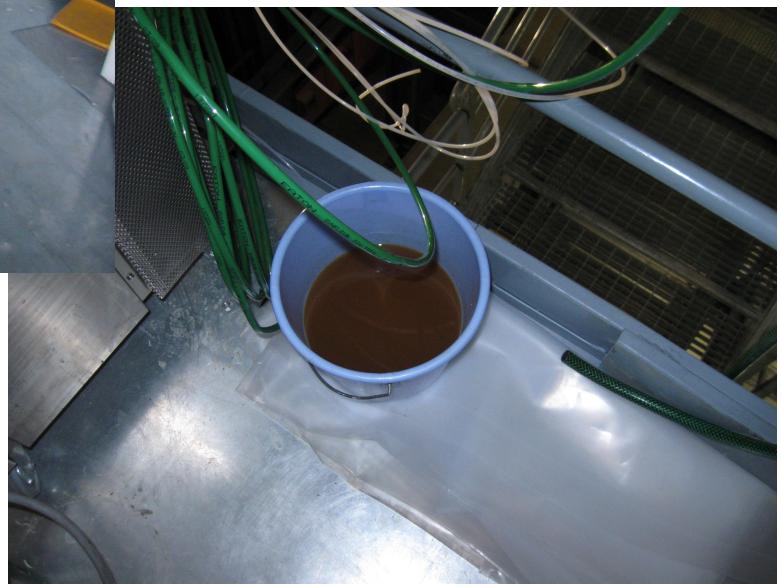
```
***************
DATA BLOCK
***************
1st Event:
 Number_of_Channels_Enabled * ......................... 4
 Number_of_Points_wave_1 * sizeof(u16) + ...... 1024 * 2
 Number_of_Points_wave_2 * sizeof(u16) + ....... 512 * 2
 Event_Trailer_Lentgh = ............................... 24
 Event_Length = ....................................12312 bytes

Event Trailer Format - 6 x u32 integers = 24 bytes
 #0 = Trigger counter (Event ID)
 #1 = Time stamp high (lowest value)
 #2 = Time stamp low
 #3 = Difference of time stamps for each card
 #4 = Data acqusition time measured in jiffies (10 ms)
 #5 = End Of Event = 0xFFFFFFFF

2nd Event: ....
```

Present Status

Saturday morning



Present Status

Saturday evening

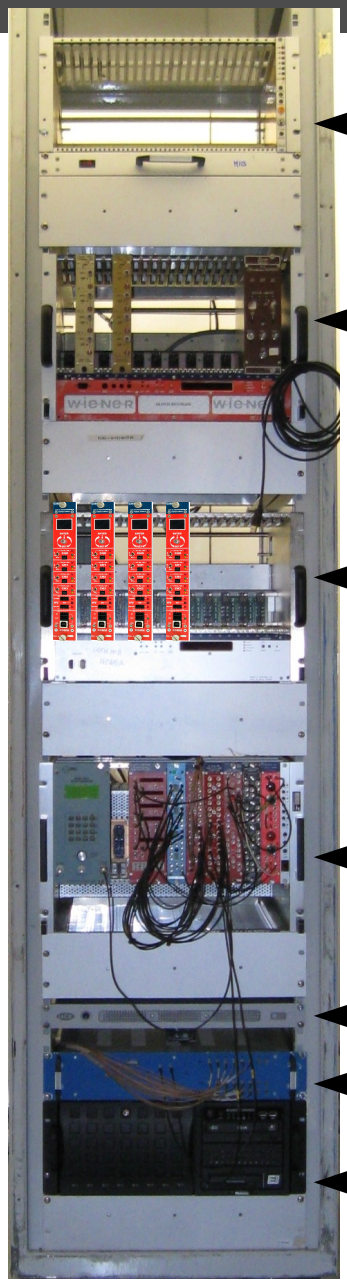
Present Status

System installed underground and ready to run in standalone mode

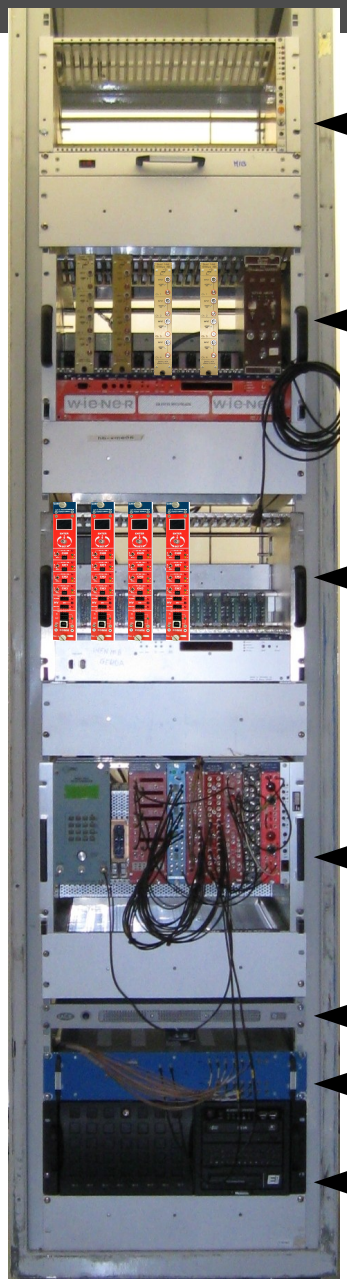
Sunday evening

The Electronic Cabinet

The Electronic Cabinet



The Electronic Cabinet



Analogue Electronics

Digitizers

Ge HV Power Supplies

Trigger Logic

Ethernet HD

Trigger Box

DAQ Computer

Minimum Working Conditions

- Chiller operational and controlled
- Temperature control of the cabinet
- Emergency stop system if
  - chiller stops working
  - temperature goes above alarm level
- Connection to the internet for remote control of the DAQ

Work still to be done

- GUI for the Ge energy threshold programming
- Test of the Ge signals baseline monitor and transmission to the SC
- Producing the OR of the trigger signals in the FPGA
- Logging the temperature of the cabinet for stability analysis
- Logging the Start/Stop of the acquisition for SC
- Synchronization with the muon veto

Synchronization with muon veto

- Distribute the same sampling clock
  - muon veto → GeDDAQ (50 MHz)
  - re–shaping the signal
- Trigger & START signal
  - GeDDAQ → muon veto
  - TTL signal from PC parallel port (START)
- BUSY signal
  - muon veto → GeDDAQ
  - GeDDAQ ignores it in standalone mode
- Synchronization with analogue pulser of variable amplitude on dedicated channels of both systems
- Check for synchronization in real–time
  - Who? how?