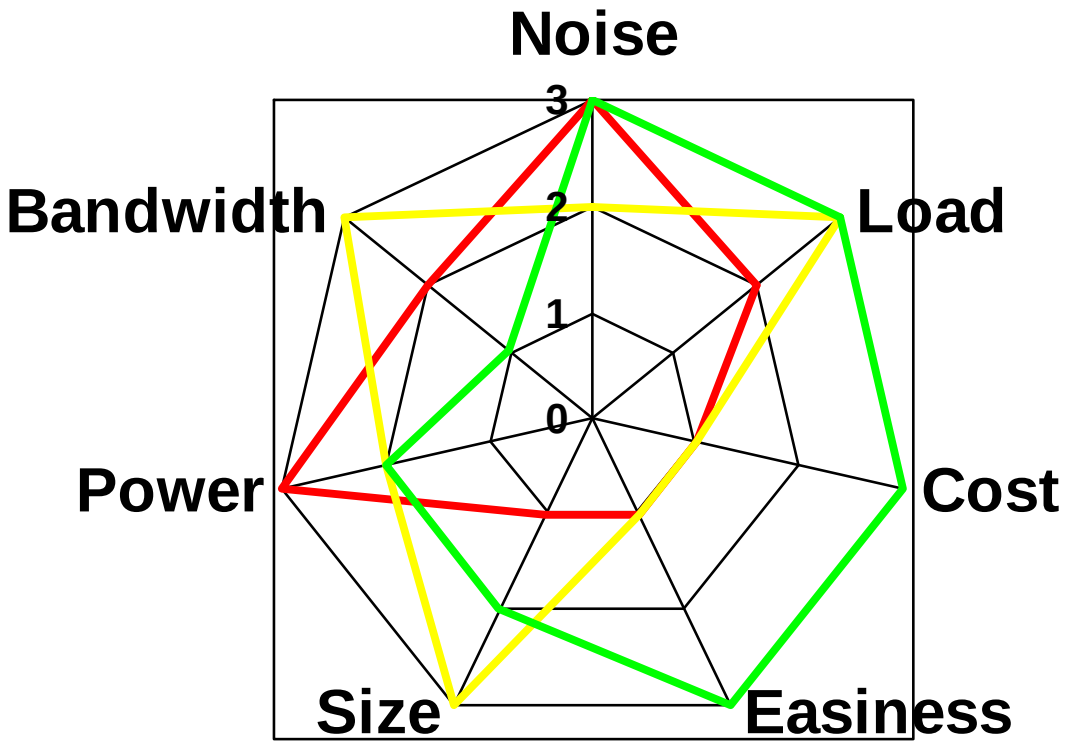
GERDA Meeting at LNGS - 2 / 2010

CC2 Charge Sensitive Preamplifier: Experimental Results and Ongoing Development

Stefano Riboldi, Alessio D'Andragora,
Carla Cattadori, Francesca Zocca, Alberto Pullia

Starting point (previous meeting)

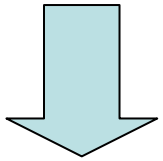


- PZ0 : BF862 + ASIC CMOS
- SR1 : ASIC CMOS
- CC2 : BF862 + CMOS Commercial Op. Amp.

Improvements

Modified schematic and Bill Of Materials (BOM)

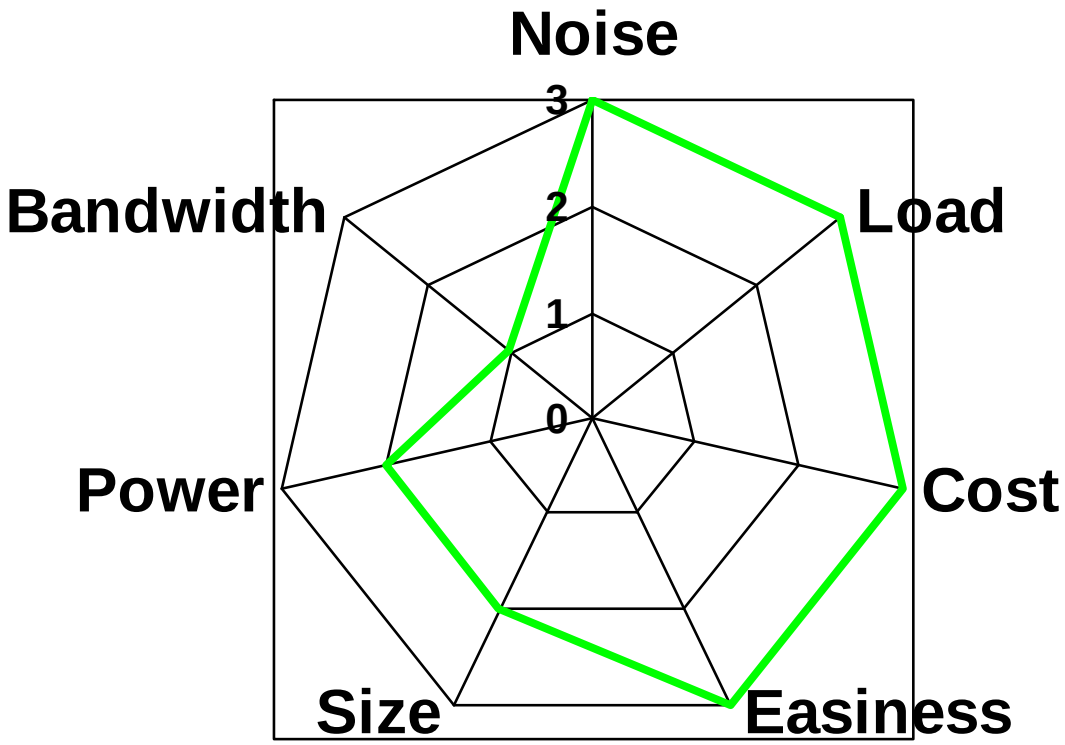
Redesigned printed circuit board



Bandwidth (no more slew-rate limited)

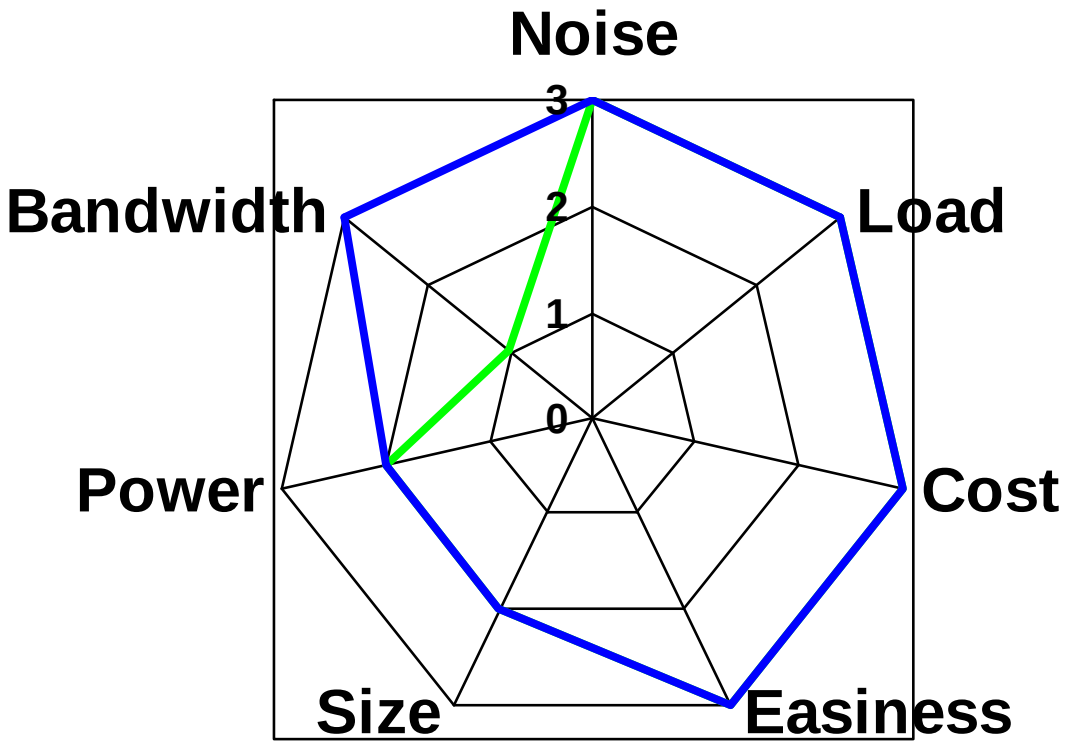
Radio Purity

Improvement on Bandwidth



- CC2 : as it was at the last “GERDA Meeting”

Improvement on Bandwidth



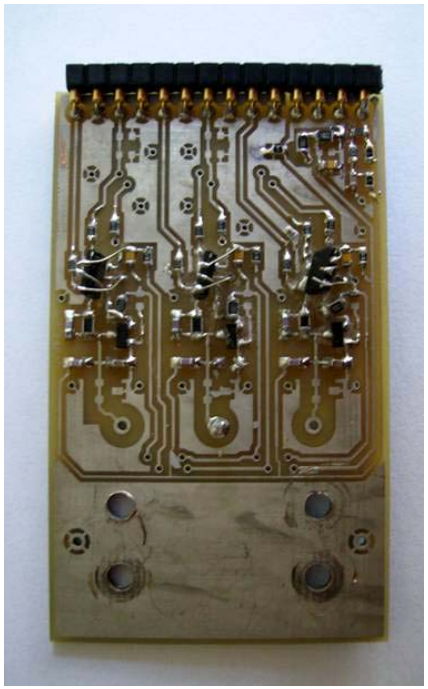
- CC2 : as it was at the last “GERDA Meeting”
- CC2 : as it is now

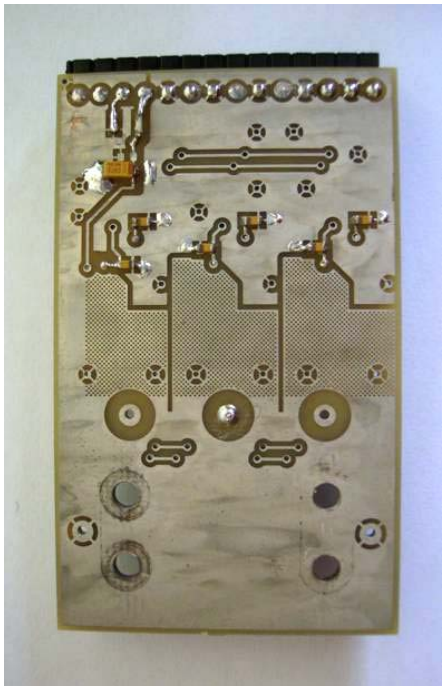
Test in Milano with SUB Detector

(A. D'Andragora, S. Riboldi, C. Cattadori)

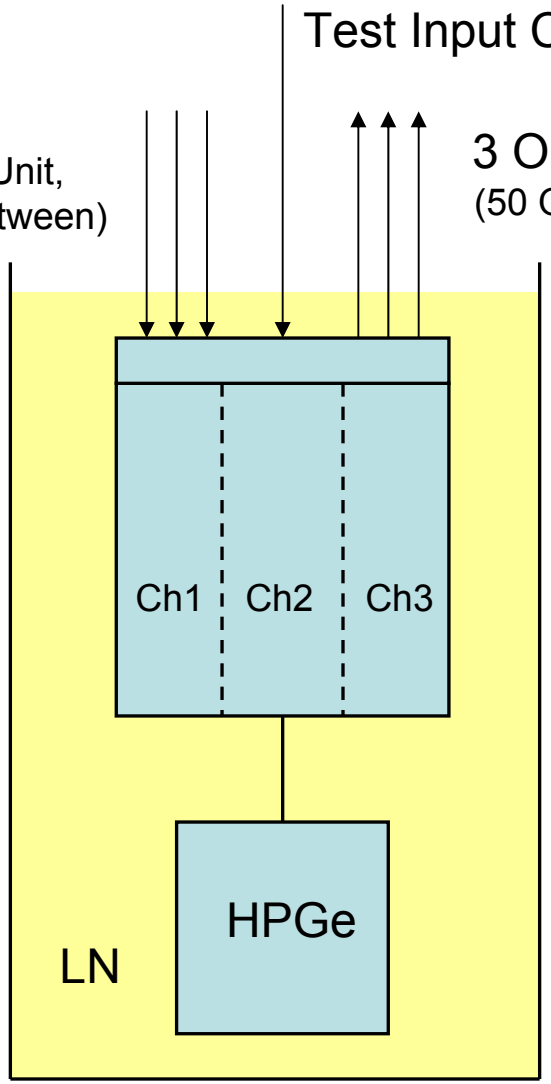
Three weeks of almost continuous operation: from 18/01 to 05/02

- PCB manufactured in FR4 material (2 layers)
- Same size as PZ0 for compatibility purpose (65 mm x 40 mm)





Experimental Setup



JFET Power Supply = 6 - 12 v

LV Power Supply = ± 2.5 v

Power Consumption < 140 mW

Dynamic Range > 15 Mev

- 7 cables used
- All cables 10 meters long
- Ch1 and Ch3 : 33 pF cap.
- Ch2 : SUB HPGe detector
- HV (Caen) set to +2500 v
- Tested HV filter (Caen)
- Acquired data with both MCA and Flash ADCs (Caen)

CC2 CSA tested for:

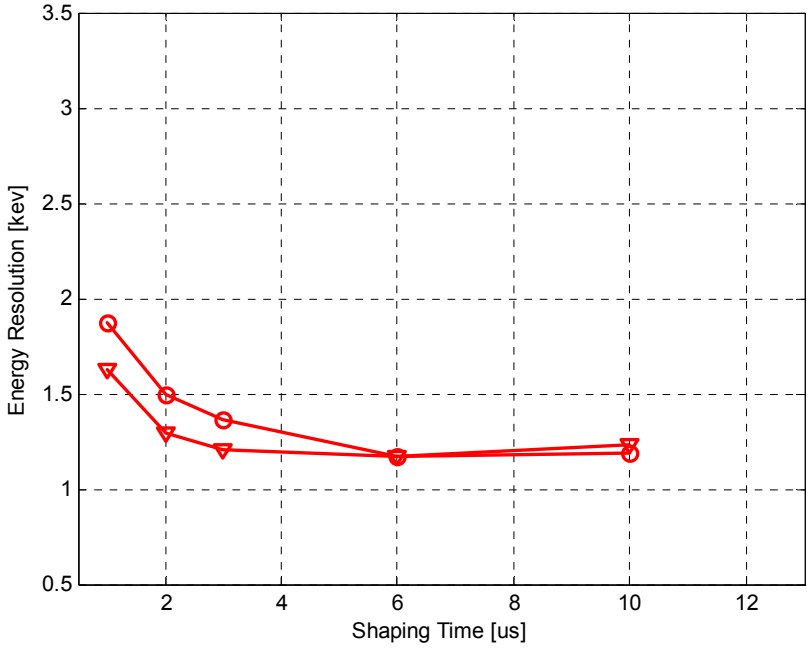
- Intrinsic Energy Resolution (vs shaping time and LV power supply)
  @ Room Temperature
  @ LN Temperature

- Bandwidth (i.e. CSA rise time vs energy of events, short and long cables)
  @ LN Temperature

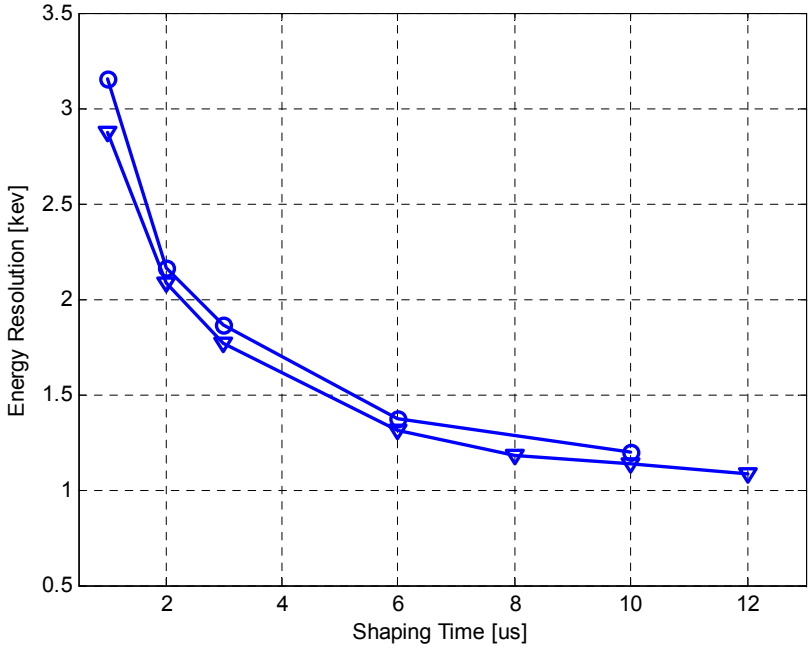
- Spectroscopy with Analog Electronics + MCA & Flash ADC
  @ medium counting rate (15 events/s radioactive source), for short time
  @ low counting rate (natural background only), overnight

- Cross-talk between Channels (as the result of two separate phenomena)
  - CSA Output to Input Cap. Coupling between Channels (opposite sign)
  - Effect of disturbances of shared LVPSs on CSA Outputs (same sign)

CSA Intrinsic Energy Resolution



Room Temperature



LN Temperature

Circle : 6 V JFET Power Supply Triangle : 12 V JFET Power Supply

Cdet = 33 pF

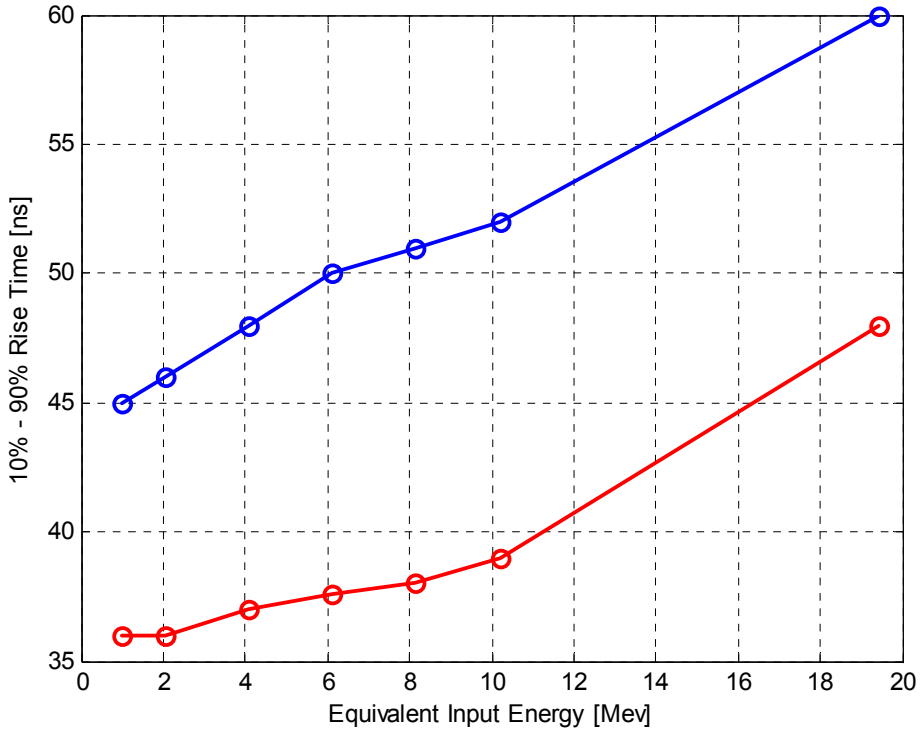
CSA Rise Time

- Blue line:
  CSA + 10 m long output cables
  (50 Ohm terminated)

- Red line:
  CSA + 1 m long output cables
  (50 Ohm terminated)

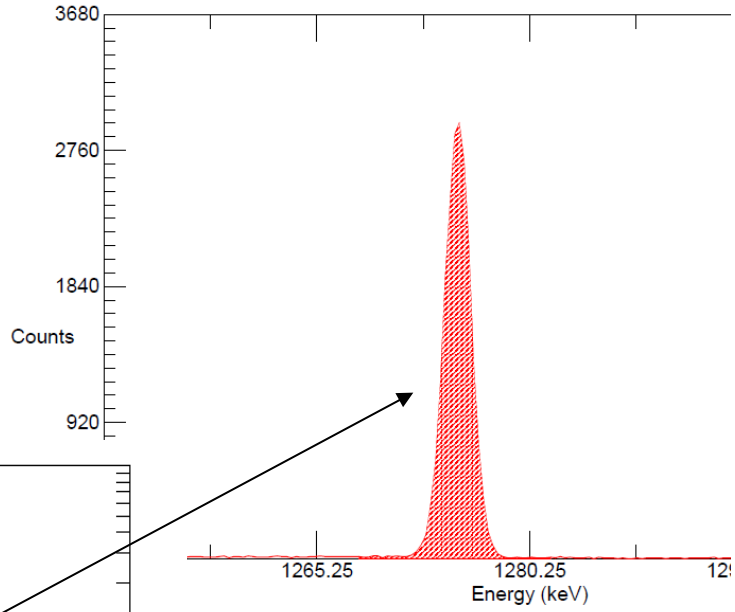
- Pulser signal 5 ns rise time

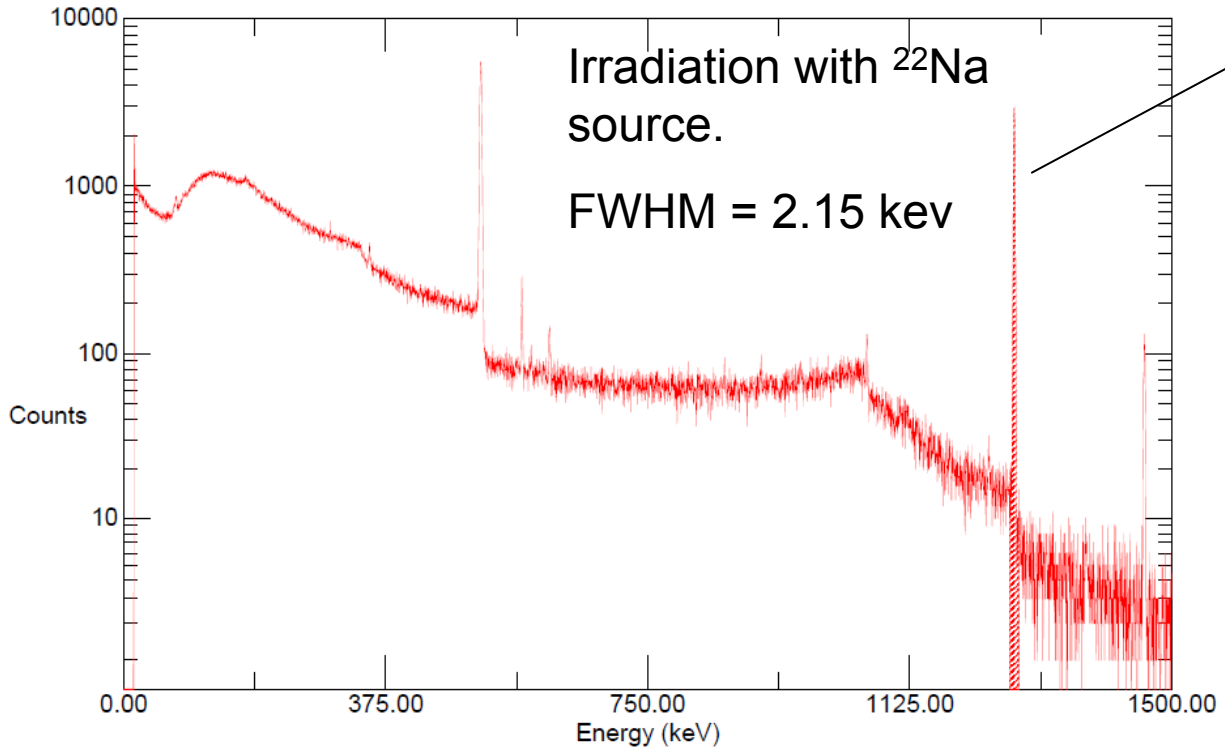
- Rise time defined as
  time interval between 10% and 90%
  of CSA output signal



Spectroscopy with CC2 CSA

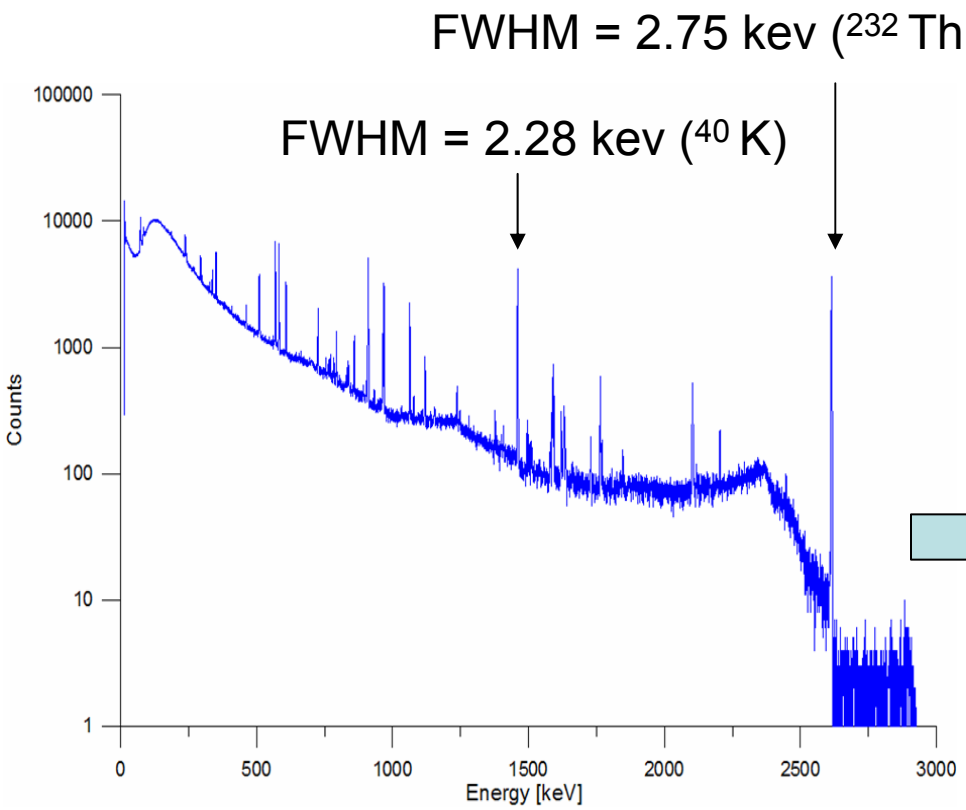
- Analog Amplifier (10 us Shaping Time)
- MCA
- Reproducible Energy Resolution
  (σ = 0.03 kev over 20 short measurements)

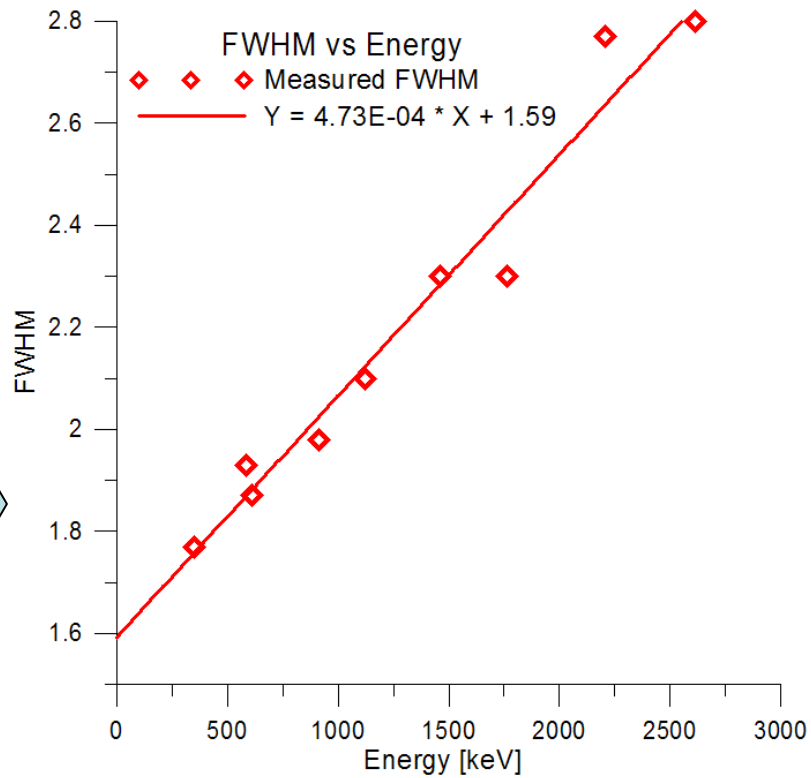




Spectroscopy with CC2 CSA

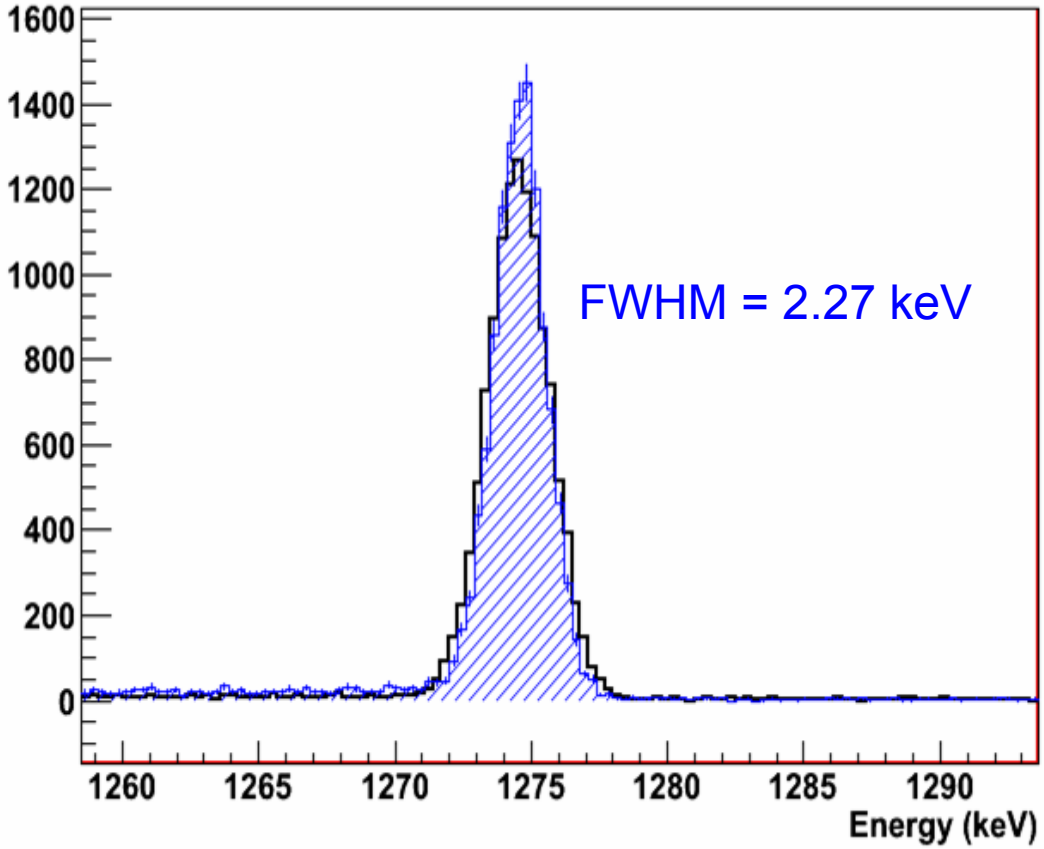
- Analog Amplifier (10 us Shaping Time)
- MCA
- Background long acquisition (over the night)





Digital Spectroscopy with CC2 CSA

- CAEN FADC
- Off-line processing
- Digital FIR filtering with symmetric weighting function for baseline
- CSA output signals with 700 us decaying time (from 10% to 90%)
- Good agreement with single-pole exponentially decaying pulse model



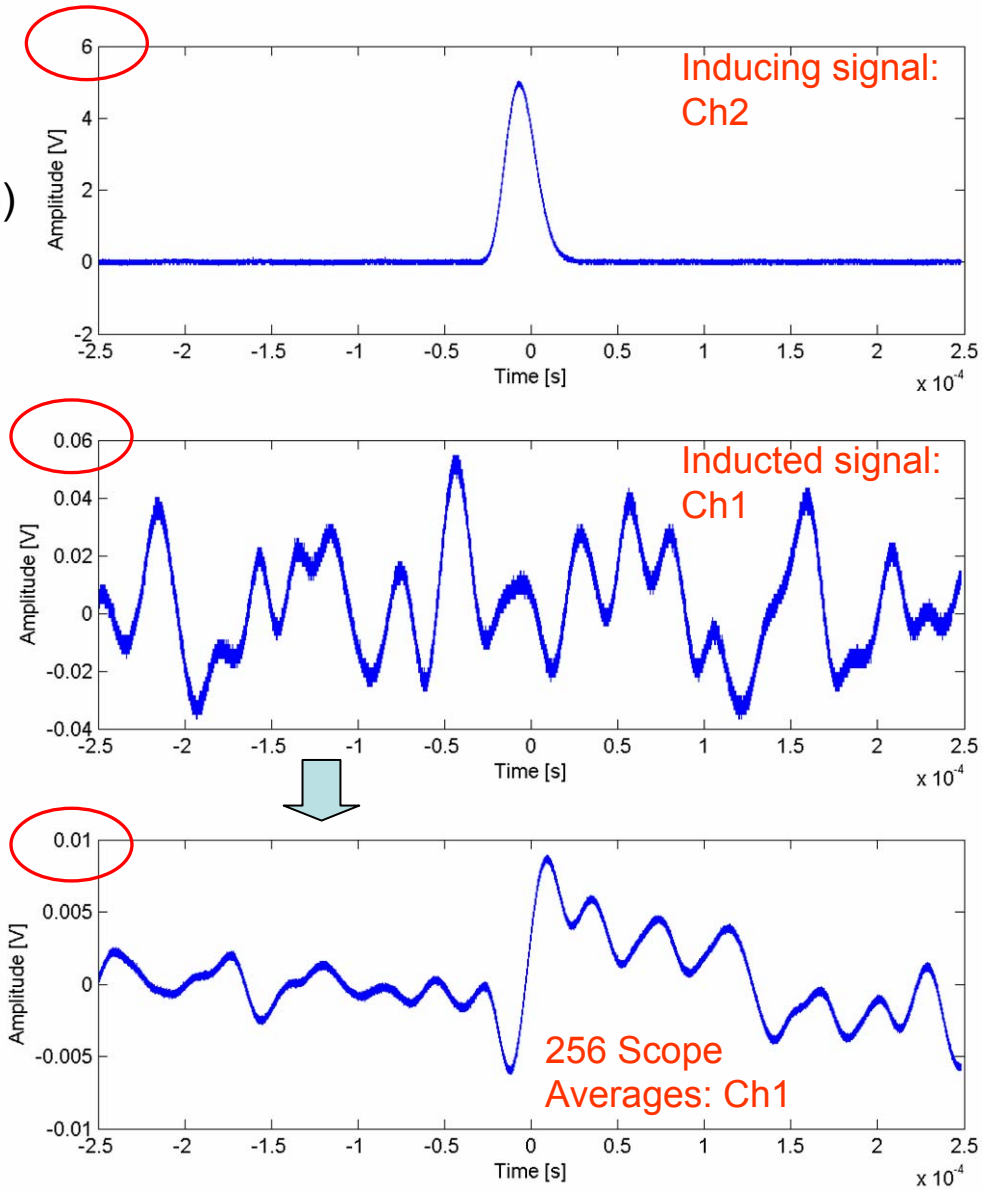
Crosstalk between Channels

- Between Ch2 (detector) and Ch1
- Same procedure as for PZ0:
  Ch1 and Ch2 through analog shaper (10us)
  Gain amplification for Ch2 = 200
  Gain amplification for Ch1 = 1000
- Experimental Result:

  ΔCh1 / ΔCh2 = (15 mV / 5 V) / 5 = 0.06 %

- Very similar results for cross-talk measurement between Ch2 and Ch3
- Because cross-talk is low, it is also difficult to estimate because of the electronic noise
- As a conservative assumption :

  Cross-talk < 0.1%



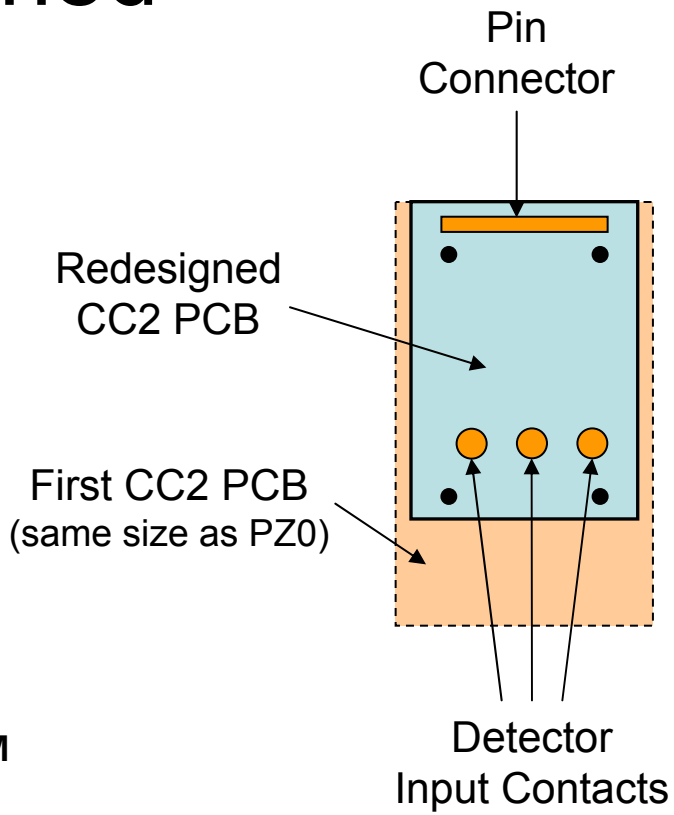
CSA Power Supply Rejection Ratio

- Important parameter to be evaluated
  (because of unavoidable LVPS variation across
  long and resistive cables)
- Low PSRR may cause:
  cross-talk between channels
  noise on output signals as a result of disturbances on LVPS
- In order to practically estimate the CSA PSRR:
  we measured the ^{22}Na peak shift on the energy spectrum
  for ± 10% variation of each LVPS

Less than 1/4000 shift of the centroid of the peak (5k counts)

PCB Redesigned

- Reduced PCB Size (38 mm x 50 mm)
- Mechanical Stability (4 distributed holes: M25)
  (no need for Teflon Layer in Copper Shield)
- Reduced Connector Pin Number (11 vs 14)
- Eliminated Feedback and Test Capacitors
  (implemented with PCB copper traces, after Alessio's work)
- Various BOM configurations to trade-off between:
  Radiopurity and Channel Crosstalk



Actual CSA BOM (as tested in Milano)

3 JFET
3 Operational Amplifiers
11 Tantalum Capacitors (LV decoupling)
22 Resistors
3 Discharge Protection Devices (JFET)
6 NP0 Capacitors (feedback, test)

⇩

Less than 0.1% measured crosstalk

Minimum CSA BOM

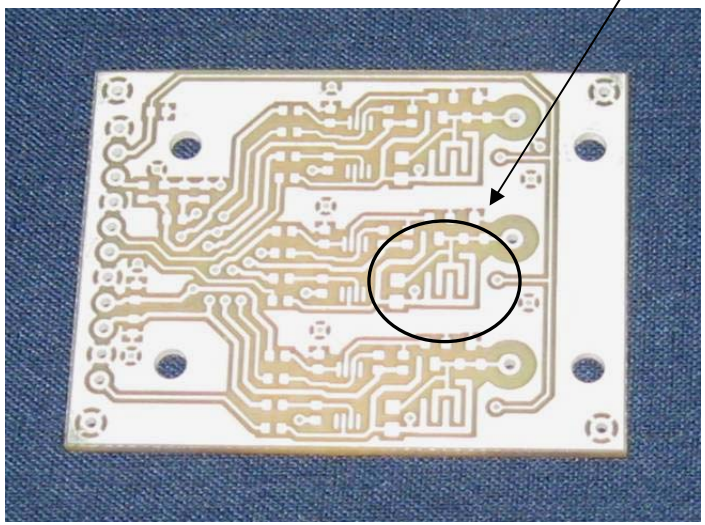
3 JFET
3 Operational Amplifiers
3 Tantalum Capacitors (LV decoupling)
13 Resistors
3 Discharge Protection Devices (JFET)

⇩

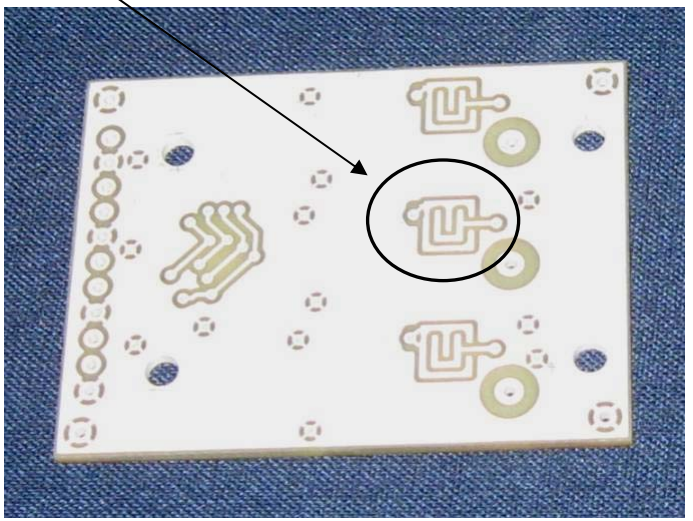
Crosstalk ? ? ?

PCB Redesigned

PCB capacitors



Component layer



Bottom layer

- Still needs to be populated, electrically debugged and tested

Radioactivity issues

- CC2 CSA expected to improve the radioactivity issues related to the FE electronics
- Radioactivity budget estimated on the base of already measured components is:

< 150 μBq / PCB (for both Th & Ra)

as a result of:

- 3 BF862 JFET (^{228}Th= 15 ± 4 μBq / PCB, ^{226}Ra= 14 ± 4 μBq / PCB)
- 3 OpAmp (not yet measured, ~3 times JFET volume, same materials as JFET)
- 0 NP0 Ceramic Capacitor (for test and feed-back) replaced by PCB Capacitors
- 11 max. (down to 3 min.) Tantalum Capacitors for LVPS decoupling (^{228}Th= 88 ± 22 μBq / PCB , ^{226}Ra= <33 μBq / PCB, ^{40}K=770 ± 330 μBq / PCB)
- Cuflon for PCB (^{228}Th <12 μBq / PCB , ^{226}Ra <3 μBq / PCB, ^{40}K =200 ± 62 μBq / PCB)
- 22 max. (down to 13 min.) resistors (3 for feed-back; 19 for polarization and LVPS decoupling) Only upper limit available, but from integral radioactivity of PZ0 are not dominant
- 7 (for signals) + 4 (for ground) PCB Pins for cable connection (^{228}Th = 42 ±14 μBq / PCB , ^{226}Ra= < 53 μBq / PCB, ^{40}K= 280 ± 140 μBq / PCB) but research of better pins in progress

Possible Realistic Roadmap

1a) Copper shields, connectors, etc. manufactured (at LNGS mechanical workshop)	2 weeks	concurrent
1b) Radio-pure PCB manufactured: (minimal or no change with respect to current design)	2 weeks	
2) PCB populated: (relatively fast, no bonding wires required)	1 week	
3) PCB tested: (for functionality and performance)	2 weeks	
4) Final assembly and test:	1 week	
5) Test for CSA radio-purity	2 weeks	
6) Redesign of CSA and PCB to separate the JFET (probably 1 more cable for LVPS)	4 weeks	

Summary of CC2 characteristics

Best energy resolution @ LNT : 0.7 kev FWHM (0 pF Cdet)
1.1 kev FWHM (33 pF Cdet)
(with 1 Mev pulser signal, 12 us shaping time)

Best energy resolution @ LNT : 1.96 kev FWHM for ^{22} Na
(12 us shaping time, 5k counts acquisition)

15 Mev guaranteed energy dynamic range

50 Ohm drive capability with 10 m long cables

Power consumption < 140 mW (down to 100 mW for 10 Mev dynamic range)

Rise time : less then 55 ns with 50 Ohm terminated, long cables and energy up to 15 Mev

Cross-talk : < 0.1%

Power Supply Rejection Ratio : should allow HPGe spectroscopy within the Gerda setup

Expected reduction on CSA radio-activity : around 50%

Operated (in Milano) with 7 cables (3 for power supplies, 3 for outputs, 1 for input test)

Small size, no bonding wires, no PCB copper shield, no LVPS “filters box”