

GERDA: Status report e richieste finanziarie 2010

C. M. Cattadori - MiB



Sommario



- Status of PZ0 3 ch
 - V1 compensated at 1 pF
 - V2 compensated at 1.4 pF to take care of capacity of long output cables (~ 1 nF)
 - Status of production and CSA availability for the GERDA exp.
 - Next ASIC production run at foundry
- Status of CSA based on Commercial CMOS OPAMP (CC)

- Status of search of Radiopure capacitors
- Issues related to Pogo-pin Matrix

Status of PZ0 3 ch circuit



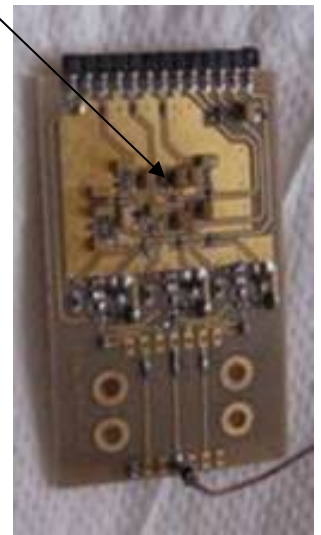
■ Available in 2 versions

- V1: 1 pF compensated (at the amplifying node), $C_f=0.2$ pF, Dynamic Range=4.5 MeV, suitable for short cables
 - Used in GDL tests with prototype detector (1 ch boards)
 - Used in preliminary tests at HdM (green board)
- V2: 1.4 pF compensated to take into account the capacitive load of the 10 m long Habia Cable, that caused some instability for signal > 2 MeV with long (12 m) cables. $C_f=0.3$ pF,
 - Dynamic Range ~ 7.9 MeV for $V_{ee} = -2.0$ V
 - Dynamic Range ~ 9.8 MeV for $V_{ee} = -2.4$ V
 - Used in HdM test available only in 3 ch version (yellow boards)
- V1 & V2 have the \sim same noise performances (1.3-1.5 keV at pulser with long cables) but V2 is somehow slower (response to voltage step ~ 40 ns)



Status of PZ0 3 ch circuit

- Important: PZ0 needs ultrastable LV PS; to minimize the voltage drop of the PS ($R_{\text{cable}} \sim 10 \Omega$) when the circuit is instantaneously drawing current to push the output pulse through the output line
 - Need high value ($\sim 10 \mu\text{F}$) buffer capacitors (T_a) to keep the $V_{\text{cc}}, V_{\text{ee}}$ as stable as possible
 - Power the circuit through 3 cables in parallel ($R_{\text{cable}} \cong \sim 3 \Omega$)



Performances of v2 measured with SUB in Milano (all 12 m long cables), Ta capacitors.



Configuration:

- Ch 1 & Ch 3, $C_{det}=33\text{pF}$: performances as measured at cold test bench
- Ch 2 connected to detector:
- $V_{FET} = 3.7\text{ V}$ $V_{CC} = 3.1\text{ V}$ $V_{EE} = -2.0\text{ V}$
- Offset $\approx -50\text{mV}$
- V_{EE} can be raised up to -2.4V

■ $V_{EE} = -2.0\text{ V}$:

- FWHM @ ^{60}Co : $\sim 2.4 - 2.5\text{ keV}$ @ 1332 keV
- FWHM @ pulser: $\sim 2\text{ keV}$ @ 1230 keV
- FWHM @ 2.6 MeV : $\sim 2.95 - 3\text{ keV}$ @ 2614 keV
- Dissipated power (for 3 chs): $\sim 40\text{ mW}$
- Measured dynamic range: $\sim 7.9\text{ MeV}$

■ $V_{EE} = -2.4\text{ V}$:

- The same as above

- Measured dynamic range: $\sim 9.8\text{ MeV}$

PZ0 3ch v2: the cross talk among the 3 chs



Cross-talk (measured in MIB may '09) on ch1 & ch3 with SUB detector on ch2

LV PS cables 12.5m (3 cables in parallel for V_{CC} & V_{EE})

- measurement on the scope 1 M Ω terminated

cross talk is mainly capacitive (opposite sign of ch2 pulse)

$$\frac{OUT\ 1}{OUT\ 2} \approx -1.8\ \%$$

$$\frac{OUT\ 3}{OUT\ 2} \approx -0.3\ \%$$

- measurement on the scope 1 k Ω (shaper load) terminated
cross talk pulse same sign of ch2 pulse

$$\frac{OUT\ 1}{OUT\ 2} = +1.2\ \%$$

$$\frac{OUT\ 3}{OUT\ 2} = +2.7\ \%$$

- The effect of 1k Ω load introduce a cross talk of $\sim+3\%$ that superimpose to the mainly capacitive one

PZ0: the production process of PCBs.



- chips are available ~25 samples: each chip will serve 3 chs
- 4 (3 chs circuit) are available; 1 @ LNGS + 3 in MI produced in july by MIPOT company
- Some mortality occurred: technology adopted up to april 2009
 - Glue the chip on board → adopt softer glue
 - Seal the Cu protective "hat" (EM & mechanical): if the sealing is not perfect after instantaneous warming up we had explosion of some Cu hats or break of the bonding wires caused by the gas stream through the hole (or vias)
- In june/july we had the production (bonding, gluing & sealing) at the MIPOT company of 3 more CSA circuits (3 ch) adopting a softer glue and the best tested sealing (solder the Cu hat along the perimeter and solder seal all the vias)

The radioactive capacitors



Radionuclide concentrations per PCB

item	mass	^{226}Ra	^{228}Ra	^{228}Th	^{40}K
PCB	6.5 g	6.3 ± 0.5	0.21 ± 0.13	0.19 ± 0.08	2.2 ± 0.7
Cuflon	4.4 g	$< 3.5 \text{ E-3}$	$< 12 \text{ E-3}$	$< 7.9 \text{ E-3}$	0.19 ± 0.06
solder	~2 g	$< 9.6 \text{ E-3}$	$< 9.2 \text{ E-3}$	$< 13 \text{ E-3}$	< 0.10
FET	0.05 g	$31 \pm 8 \text{ E-3}$	$< 26 \text{ E-3}$	$33 \pm 8 \text{ E-3}$	< 0.12
Big res.	0.03 g	$< 22 \text{ E-3}$	$< 20 \text{ E-3}$	$< 20 \text{ E-3}$	< 0.21

unit in mBq

Capacitors



Item	Number/PCB	^{226}Ra	^{228}Ra	^{228}Th	^{40}K
X5R	20	3.8 ± 0.3 mBq/PCB	< 0.97 mBq/PCB	0.84 ± 0.18 mBq/PCB	< 2.9
X7R	1	0.99 ± 0.14 mBq/PCB	< 0.36 mBq/PCB	0.34 ± 0.09 mBq/PCB	< 0.69 mBq/PCB
Resistors	24	< 0.14 mBq/PCB	< 0.36 mBq/PCB	0.22 ± 0.07 mBq/PCB	< 1.4 mBq/PCB
C (Ta)	10	< 30 $\mu\text{Bq/PCB}$	< 100 $\mu\text{Bq/PCB}$	80 ± 2 $\mu\text{Bq/pc}$	0.70 ± 0.03 $\mu\text{Bq/PCB}$



PZ0: Next ASIC Run



Next ASIC run:

- use of 0.35 μm CMOS technology (instead of 0.8 μm)
- new version of PZ0 with improved output stage
- more spaced bonding pads in order to simplify bonding procedure

CC2 : a Back-Up Solution for the CSA Front-End Electronics



- What does CC2 stand for?

CC2 (CSA) => Commercial Cmos (CSA) rel.2

- Why may we need a Back-Up Solution now?

To provide "Robust, Fast & Cheap to Get" Electronics to run long and not critical tests (e.g. on the DAQ system)

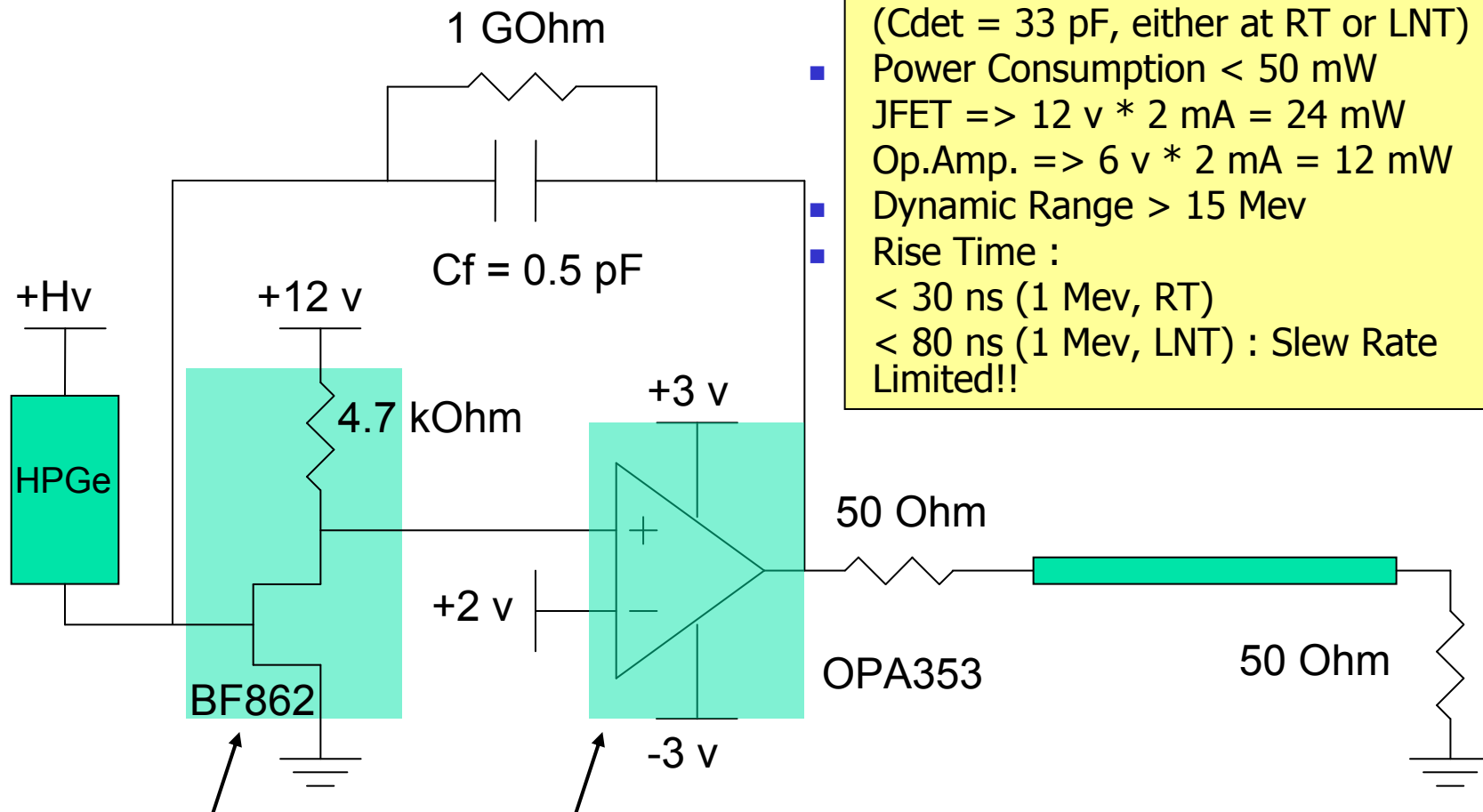
- Why it is available only now?

CMOS Operational Amplifiers with enough BW (20 MHz) have been released (e.g. by Texas Instrument) in 2007

- How to choose between CMOS Op.Amps?

7 devices of the OPA35x family (pin-to-pin compatible) have been tested... OPA353 seems the most promising

CC2 CSA Design & Results



- Noise < 1 keV FWHM (12 μ s sh.t.) (Cdet = 33 pF, either at RT or LNT)
- Power Consumption < 50 mW
JFET => 12 v * 2 mA = 24 mW
Op.Amp. => 6 v * 2 mA = 12 mW
- Dynamic Range > 15 Mev
- Rise Time :
< 30 ns (1 Mev, RT)
< 80 ns (1 Mev, LNT) : Slew Rate Limited!!

Low Noise JFET

High Gain, Current Capable, Tiny

Non Inverting Input Stage

Non Inverting CMOS Stage

28-30 Settembre 2009

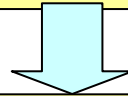
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A few things we learned (not to forget)



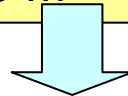
As a “matter of fact” very small coaxial cables are not ideal because of :

- High Resistivity (1 Ohm / m)
- High Capacitance (100 pF /m)



Because of non-zero resistivity of cables, CSA power supply voltage is not exactly the one imposed at the far-end of the cable, but also depends on the instantaneous current drawn through the cable :

“Voltage Noise” = “Current Variation” * Cable Resistance
(e.g. 10 mA * 1 Ohm / m * 10 m = 100 mV)



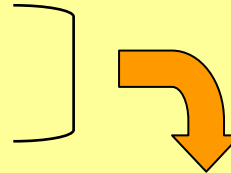
This is a far-from-ideal condition, not so often affecting real experiment set-ups and it caused in the past some unexpected behavior of the PZ0 CSA

CC2 CSA Design Improvements



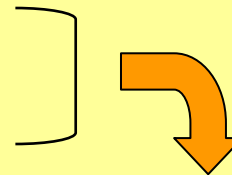
CSA Output Signal Integrity may be Affected by :

- Backward Reflections at Load Point
- Slow Charge of Large Cable Capacitance



Coaxial Cable 50 Ohm Termination

- Self – Induced Distortion of Pulse Shape
- Cross – Talk among Board Channels



Minimize Effect of Power Supply on CSA Output
Minimize Capacitive Coupling between Channels

How the improvements work

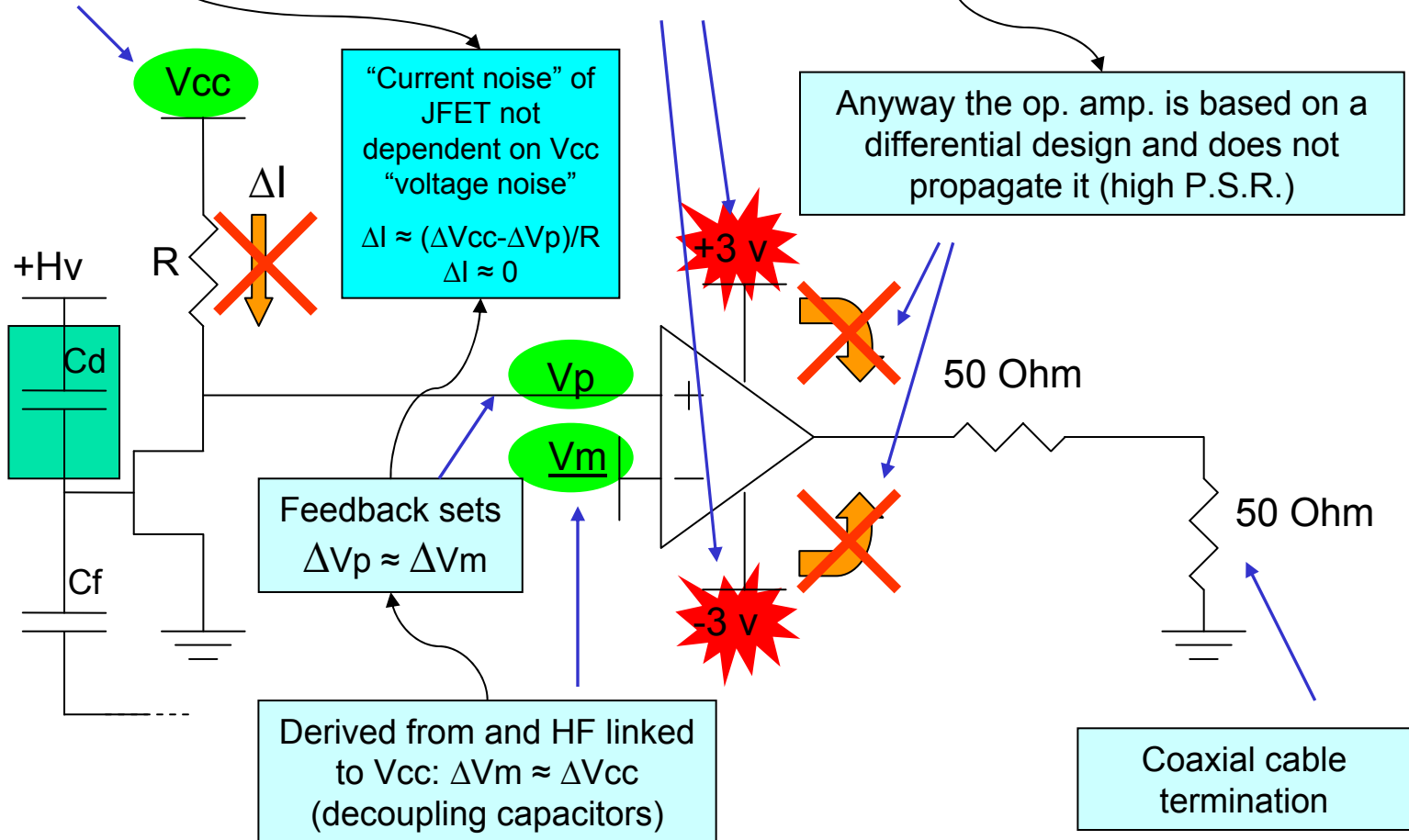
This power supply is "quiet" because the absorbed current is small and constant

These power supplies are "noisy" because of large variation of current into terminated load

"Output noise" of CSA depends on JFET drain "current noise" according to:

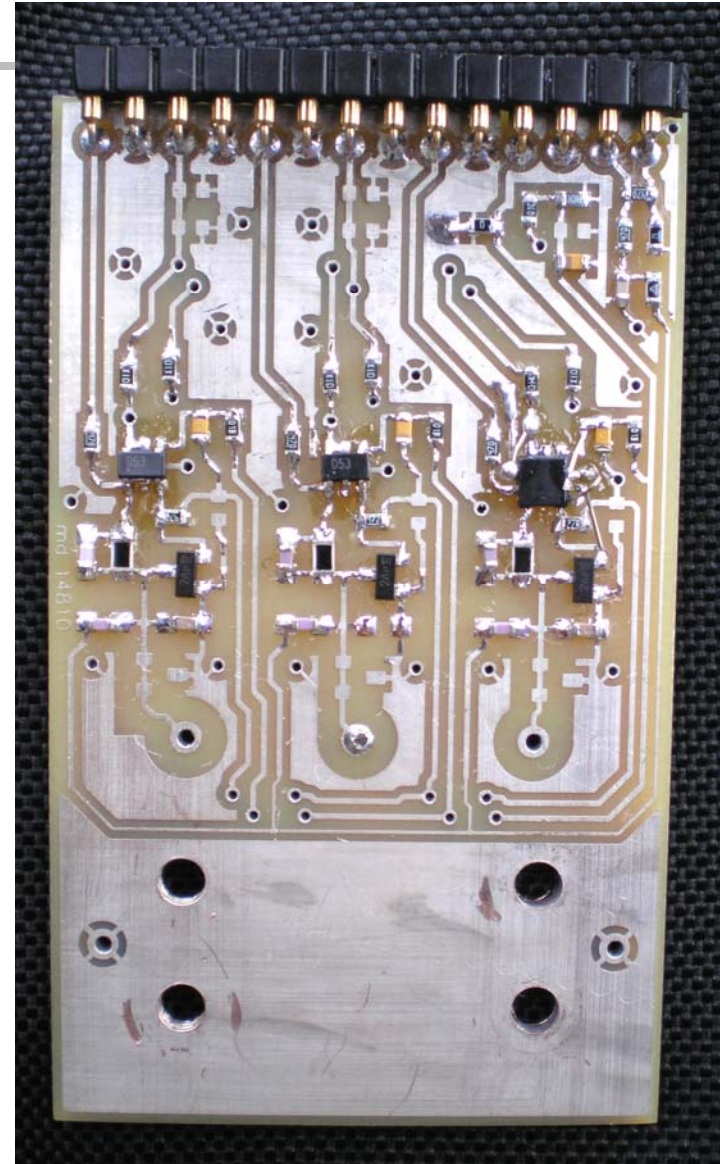
$$\Delta V \approx \Delta I / g_m * (C_d / C_f)$$

$\Delta V \approx 0$

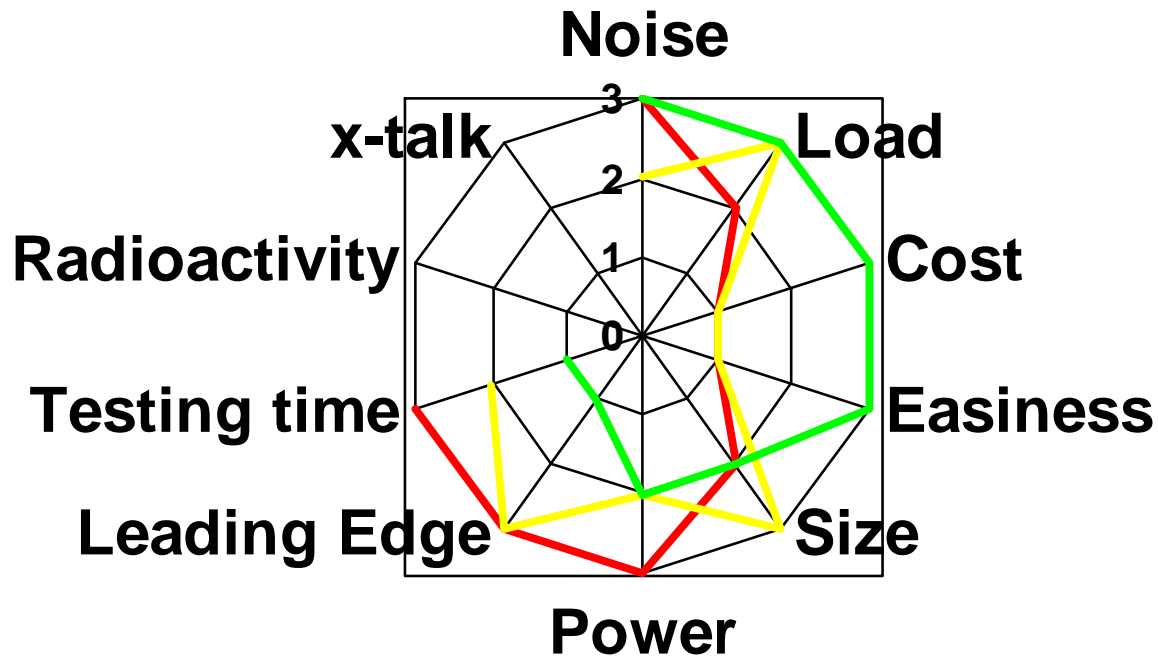


Component list:

- 3 JFET BF862
- 3 OPA35x
- 3 JFET tbd (protection device)
- 9 Tantalum Capacitors (10 μ F, 4v)
(down to 4?)
- 6 NP0 Ceramic Capacitors (1pF)
- 19 Resistors (down to 11?)



The three CSAs compared



- PZ0 : BF862 + ASIC CMOS
- SR1 : ASIC CMOS
- CC2 : BF862 + CMOS Commercial Op.Amp.

Conclusions about FE



- 3ch CSA based on ASIC PZ0 v2 glued and bonded on board is available. One of them has been used in HdM after extensive tests with SUB with long cables. The circuit has very good noise figure, should be improved in the output stage for PSRR. New ASIC production run are foreseen within this year, in $0.35\mu\text{m}$ technology.
- 4 x 3chs CSA circuits are available. The 3 newly (3 in july) circuits URGENTLY need γ -spectrometry measurement to check that with new Ta capacitors the overall ^{232}Th budget is below $200\mu\text{Bq}$
- The technology to glue the chip on-board, seal the Cu cover hat & cool down and warm-up procedures is hopefully now safest (for circuit life).
- A new CSA (same approach of PZ0 CSA i.e. non integrated front-end JFET and feedback component) based on Commercial CMOS OPAMP has recently been designed and tested both with SUB and at HdM with capacitors. Very promising, can drive $50\ \Omega$ load but limited in the actual design in slew rate. Improvements are possible and foreseen, need more experimentation with SUB, and then in HdM.
- A full comparison between the two circuits is not yet possible as for CC2 crosstalk and radioactivity measurements tbd.

The Pogo-pin matrix

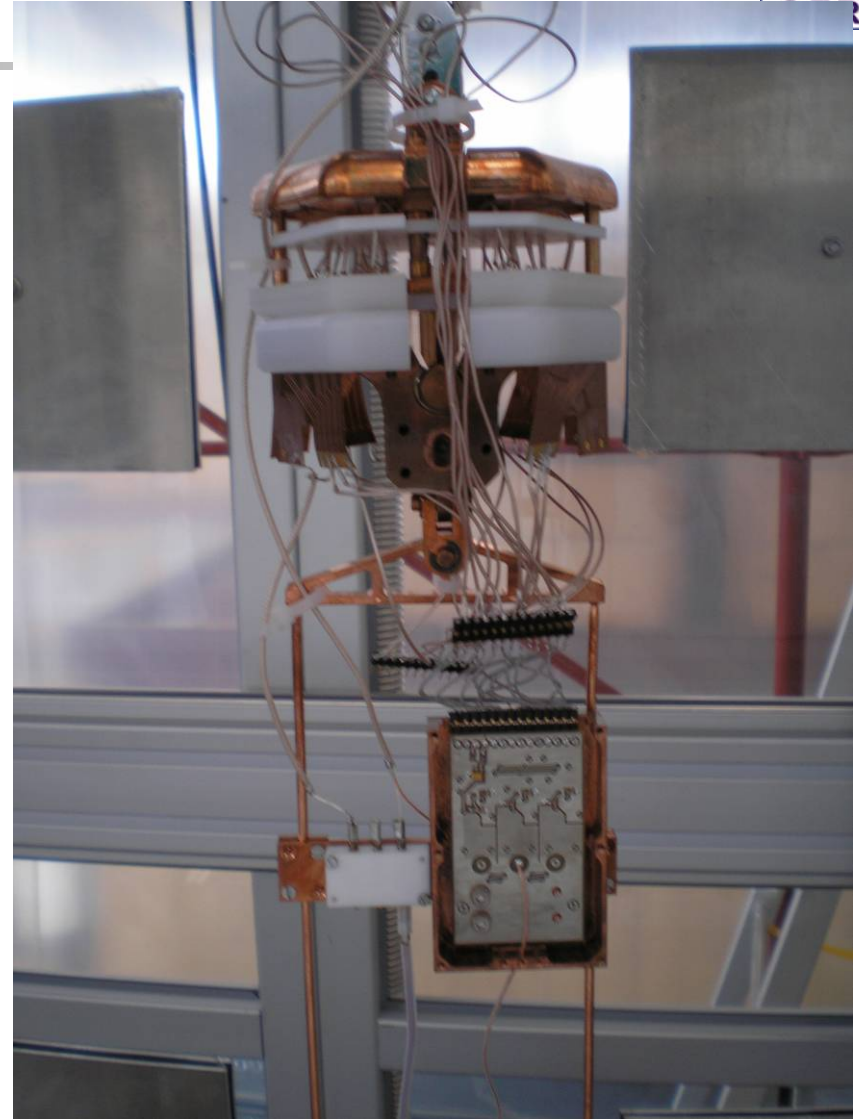
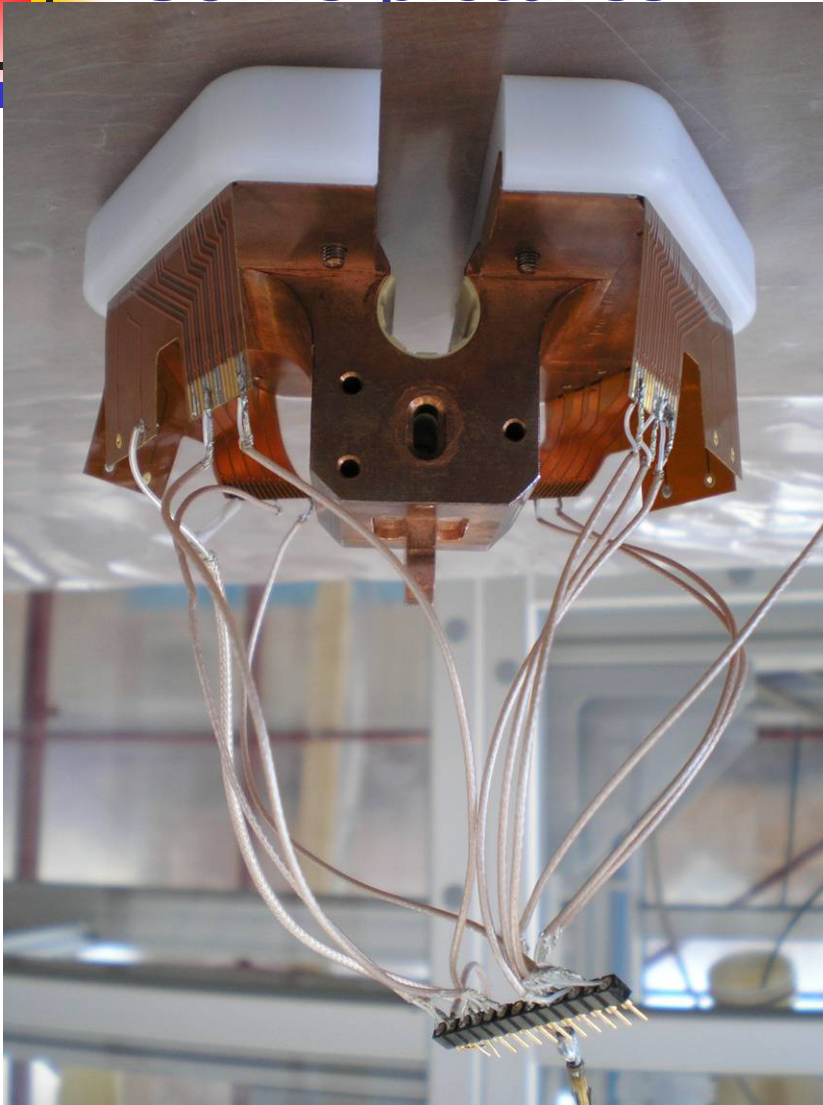


- Problem encountered: very end of august after few (3-4 cooling cycles) several contacts were lost
 - Test pulse contact (middle august)
 - 2 outputs (one after the other)
 - GND of HV3 not good
 - Observed deformation of pulse leading edge during CC2 test



- Decided to use the 9 spare cables in the cable bundle (not welded to top PPM) and bypass the PPM with 9 short piece of coaxial cables (3LV,1HV,3OUT,1TestIN). To do this reopen the feedthrough flange and solder the spare cables to the feedthrough instead of cables connected to PPM.
- Realized a modified version of PPM bottom part to avoid use of kapton cable, drilling copper and using solder-spring loaded pogo pins. We agreed on this modification in january 2009!
- To be tested at cold very soon

Some pictures



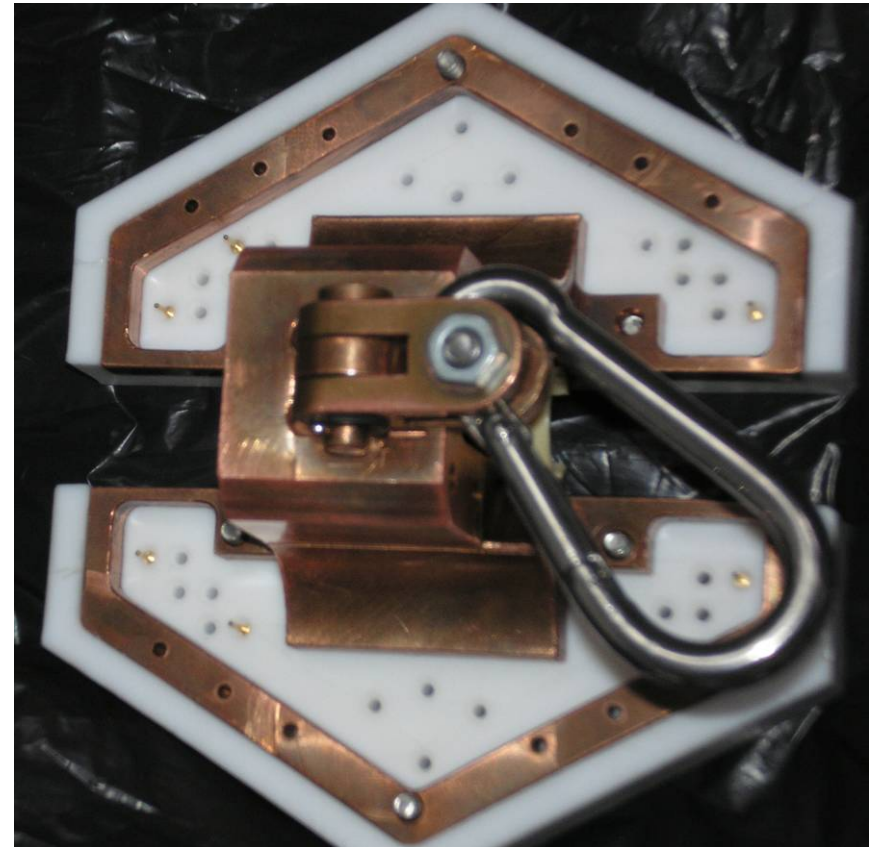
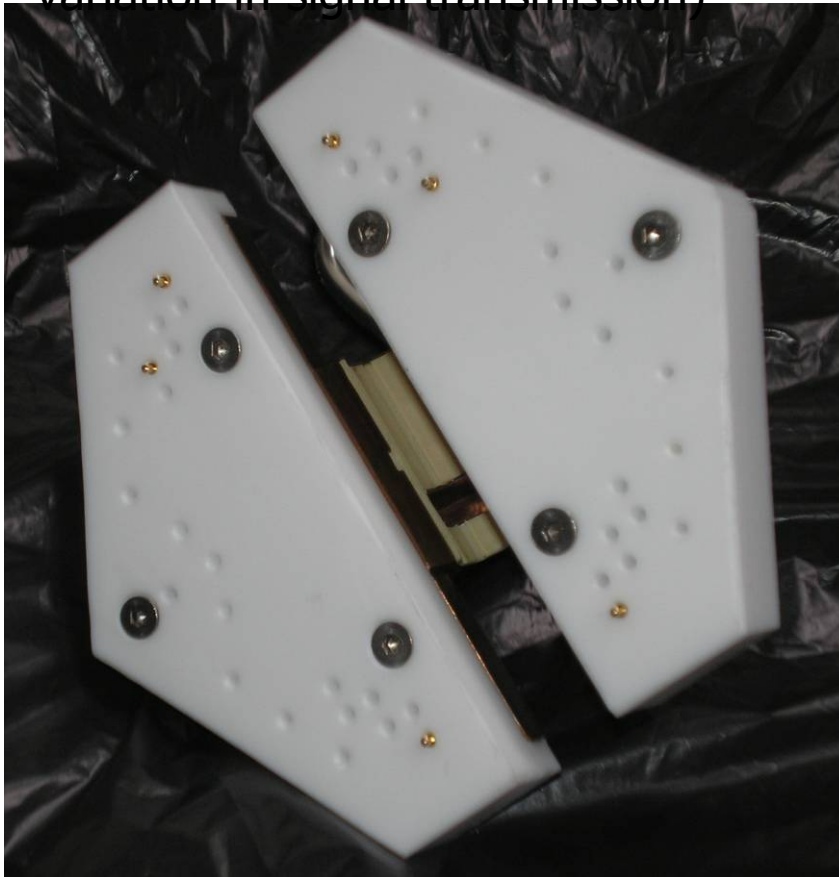
LNGS, GERDA meeting
28-30 Settembre 2009

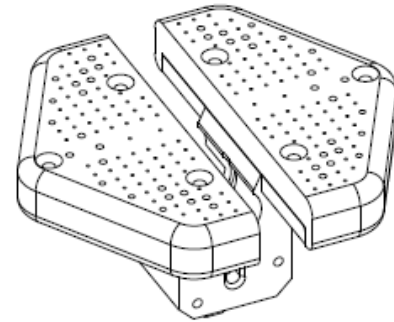
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The modified PPM bottom part to receive coaxial cables

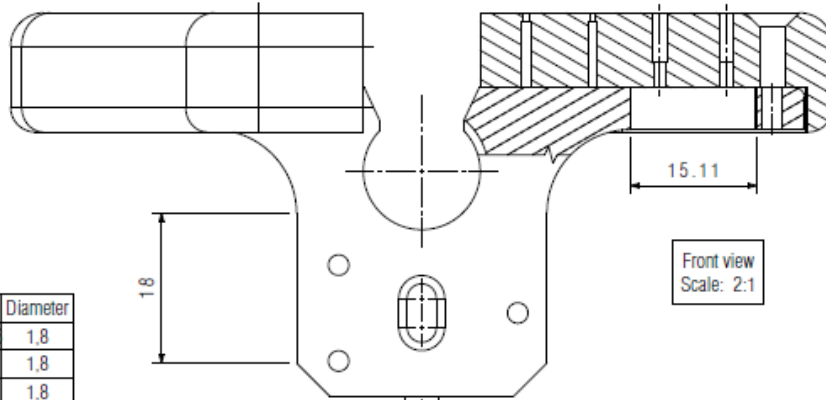


Modification to avoid use of flat kapton cable (radioactive+ avoid possible bad contacts between spring loaded pin and kapton+ avoid impedance variation in signal transmission)



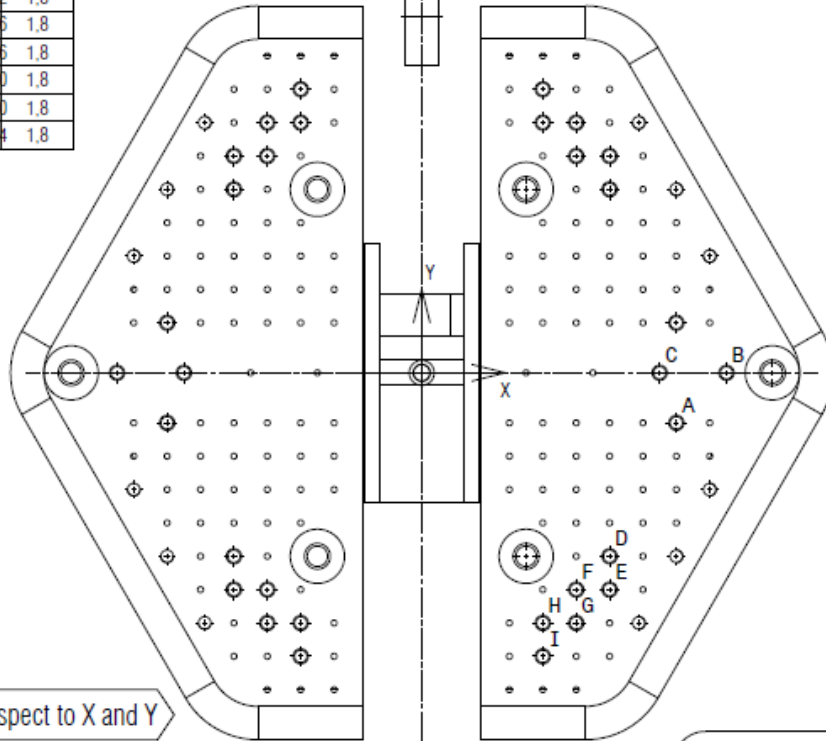


Isometric view
Scale: 1:1



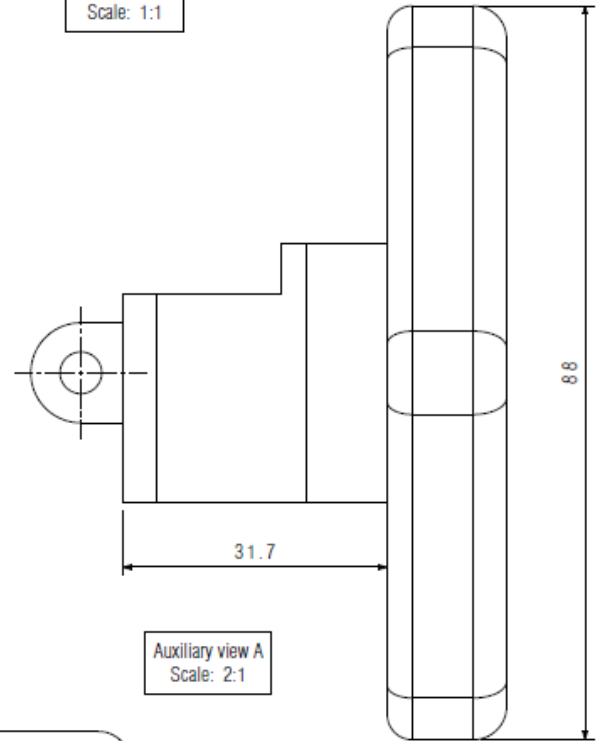
Front view
Scale: 2:1

REF.	X	Y	Diameter
A	30,5	-6	1,8
B	36,5	0	1,8
C	28,5	0	1,8
D	22,5	-22	1,8
E	22,5	-26	1,8
F	18,5	-26	1,8
G	18,5	-30	1,8
H	14,5	-30	1,8
I	14,5	-34	1,8



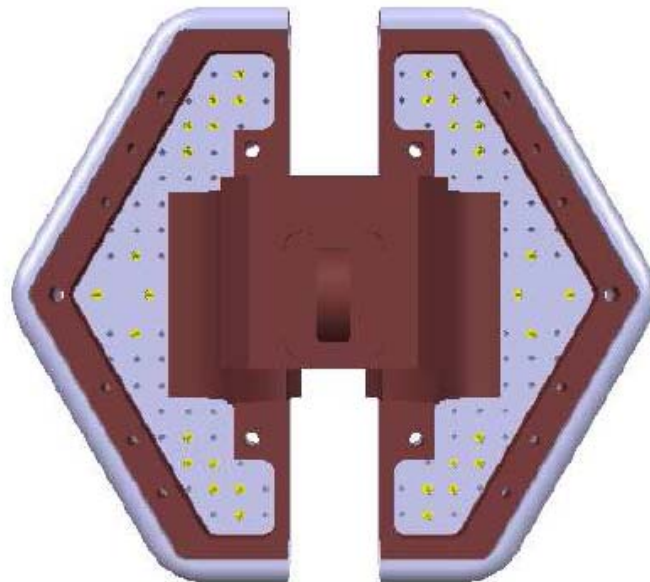
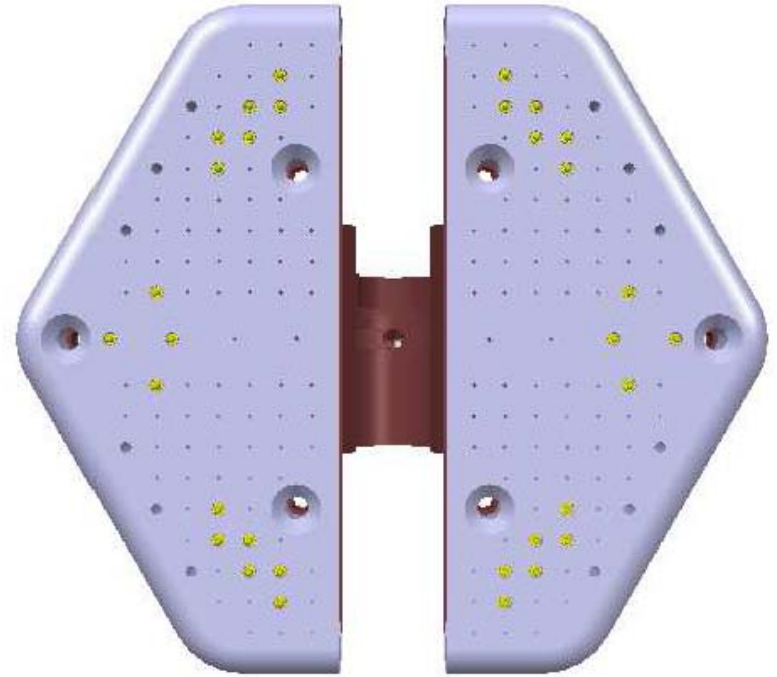
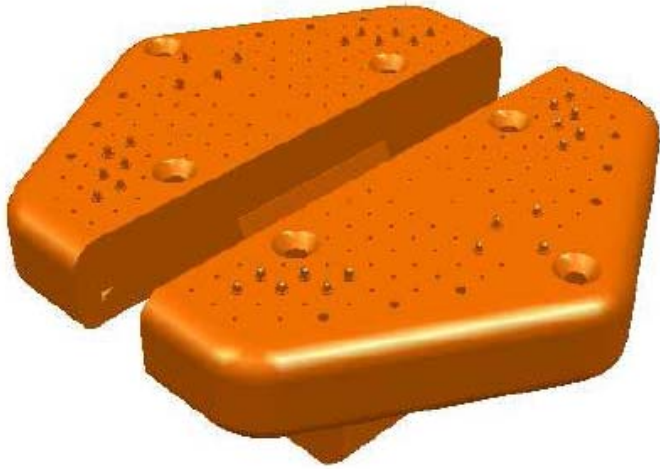
Top view
Scale: 2:1

Symmetric respect to X and Y



Auxiliary view A
Scale: 2:1

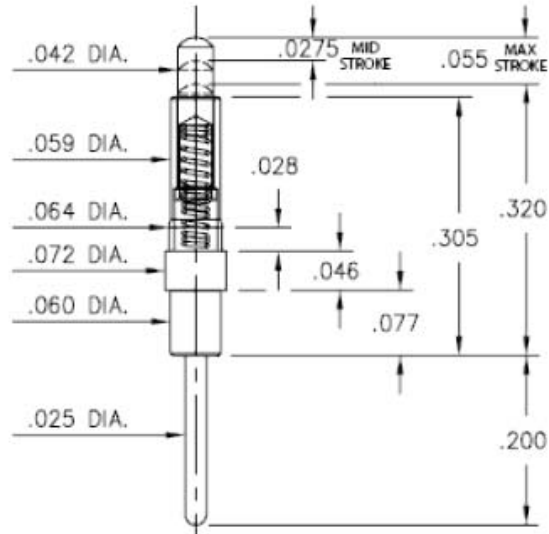
GERDA POGOPIN MODIFIED
Made by INFN LNGS Mechanics Service



LNGS, GERDA mer
28-30 Settembre 2

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Product Number: 0922-0-15-20-75-14-11-0



Description:

0922 - Spring-Loaded Pin

Packaging:

Packaged in Bulk

0922-0-15-20-75-14-11-0

Standard stroke

Solder mount in .027 min. mounting hole

Mill-Max Part Number	Shell Plating	Contact Plating	RoHS Compliant
0922-0-15-20-75-14-11-0	20 Åµ" Gold over Nickel	10 µ" Gold over Nickel	

SHELL MATERIAL:

BRASS ALLOY (UNS C36000) per ASTM B 16

Properties of BRASS ALLOY:

- Chemical composition: Cu 61.5%, Zn 35.4%, Pb 3.1%†
- Hardness as machined: 80-90 Rockwell B
- Density: .307 lbs/in³
- Electrical conductivity: 26% IACS*
- Melting point: 900°C/885°C (liquidus/solidus)

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