Synchronization of Muon + Padova DAQ

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Padova Ge system:
 - FADC data in memory on PCI cards
 - every PCI card has 64 bit counter which increments with system clock 100 MHz
 - this counter is latched when a trigger arrives --> data stream
 - PCI cards are initialized by CPU → all counters start at a different time
 - in addition: 32 bit trigger counter

Muon system:
 - FADC data in memory on FADC board (SIS3301) (~12 boards)
 - every FADC generates a trigger signal
 - MPIC card takes ~12 trigger signals and generates a common STOP
   (e.g. if 3 FADCs have triggered within 50 nsec)
 - FADC get synchronous clock and STOP
 - MPIC card has 48 bit counter which increments with system clock 100 MHz
 - this counter is latched when a trigger arrives / is generated --> data stream

Synchronization:
 - all counters use the same 100 MHz clock
   → up to an offset due to different reset times all counters are identical
 - after start of DAQ send a dummy trigger
 - for all later events store the time (number of counts) since this dummy trigger
   → relative timing with 10 nsec resolution identical everywhere
 - in addition store computer time or GPS time in the data stream
 - offline veto between Ge and Muon

event controller

start &
enable trigger (Ge and muon)

start &
enable trigger (Ge only)

status

status

muon DAQ

Ge DAQ

trigger

test pulse

system clock