Final FE electronics,flanges,cabling

- Will be tested at HdM with naked detectors after SUB test: 3ch PZ0 circuit
- Availability: 3 circuits + 3 to be mounted and bonded by company with “best” sealing procedure (soldering)
- Performances: Circuit with 1.4 pf compensating capacitor (integrated in ASIC): 2.7 keV

- Performances with SUB (all 12 m long cables)
- Canale 1 e 3 con Cdet=33pF: prestazioni uguali a quelle misurate al banco
- Canale 2 collegato al detector:
- VFET = 3.7 V VCC = 3.1 V VEE = - 2.0 V
- Offset ≈ - 50mV
- VEE can be arised up to -2.4V)
- VEE = - 2.0 V:
- FWHM @ 60Co: ~ 2.4 - 2.5 keV @ 1332 keV
- FWHM @ pulser: ~ 2 keV @ 1230 keV
- FWHM @ 2.6 MeV : ~ 2.95- 3 keV @ 2614 keV
- Dissipated power (for 3 chs) : ~ 40 mW
- Measured dynamic range: ~ 7.9 MeV
- VEE = - 2.4 V:
- The same as above
- Measured dynamic range: ~ 9.8 MeV