Istituto Nazionale
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Status of new 3-channel FE circuits for detector string readout

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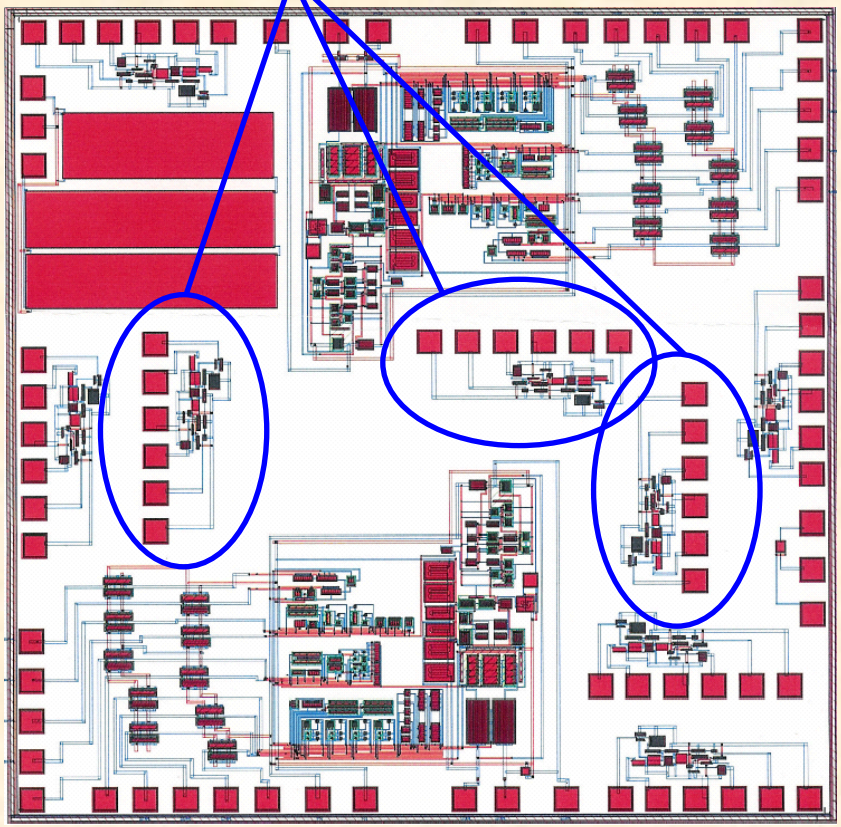
GERDA meeting at LNGS, 10-12 Nov. 2008

Outline

- 3-channel Milano PZ-0 ASIC (PZ-0 found as the best candidate preamplifier for Phase I)
- Design of the “T1” PCB for 3-channel PZ-0
- 3-channel PCB features
- 3-channel PCB open issues (to be tested)
- Design of a new “S2” PCB for 1-channel PZ-0
- Time schedule for PCBs production and testing

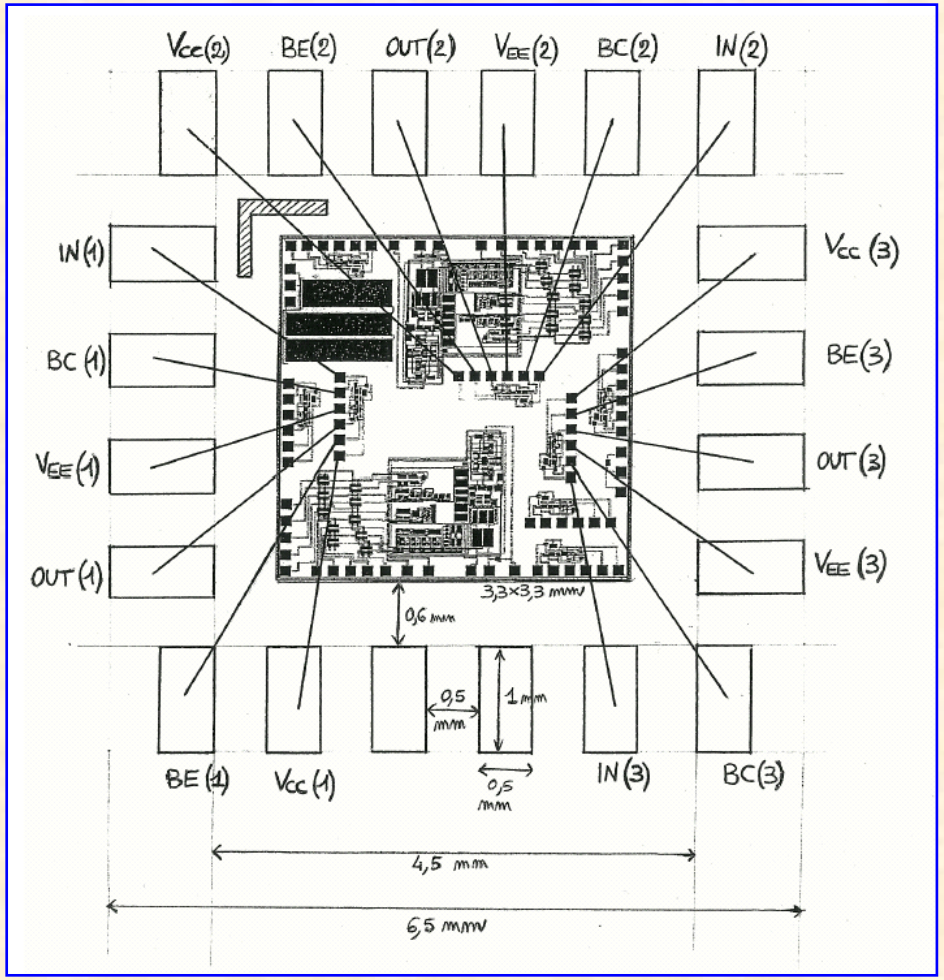
3-channels PZ-0 ASIC

Layout of the ASIC with
the three PZ-0 channels

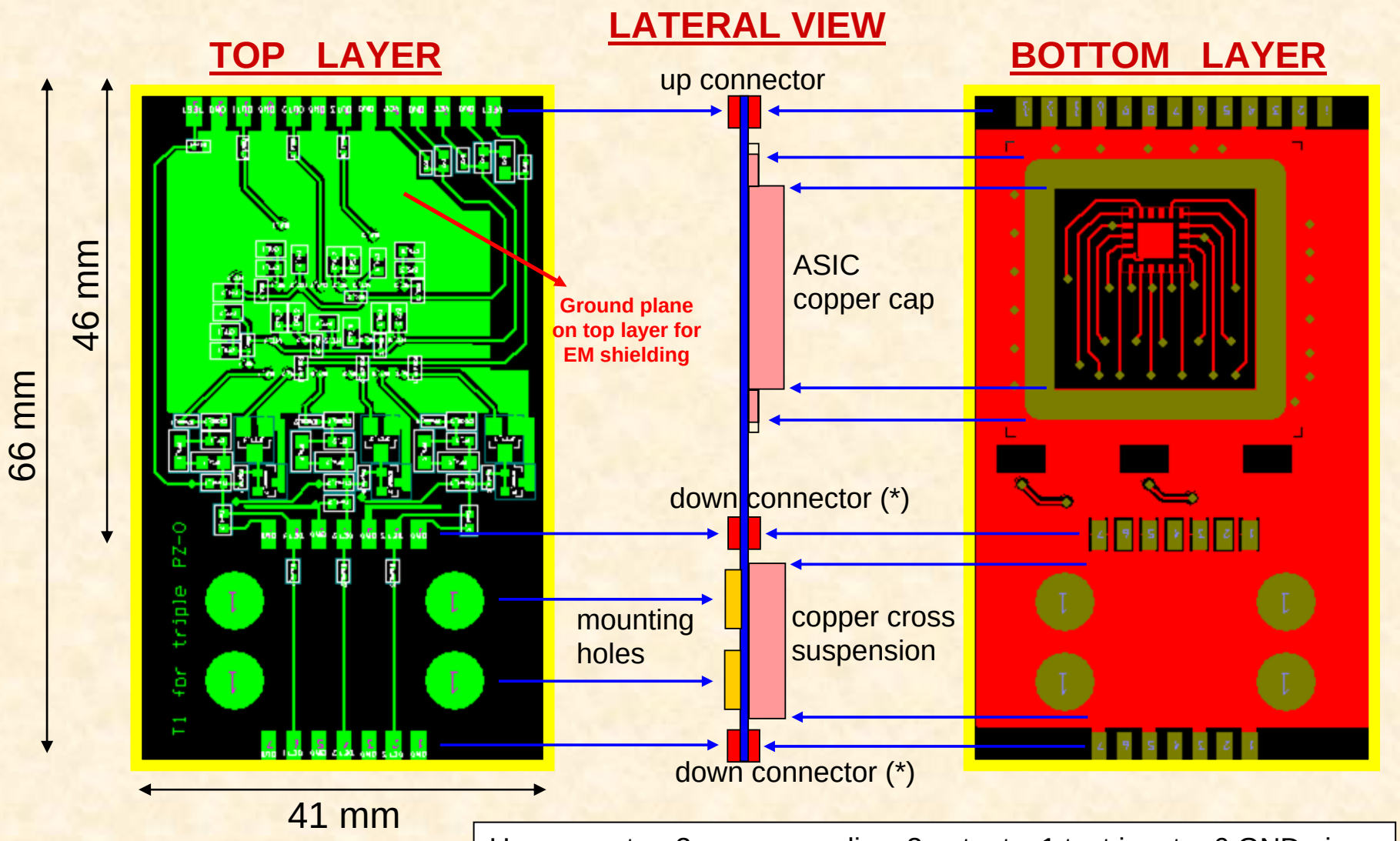


Chip dimensions: 3.3 x 3.3 mm
Bonding pads: 90 x 90 μm

Bonding scheme (directly on the PCB,
no ceramic carrier)



“T1” PCB for 3-channels PZ-0



Up connector: 3 power supplies, 3 outputs, 1 test input + 6 GND pins
Down connector (* two possibilities): 3 detector inputs + 4 GND pins

“T1” PCB: features

- **No improved performances are expected in terms of noise, bandwidth and termination resistances (150 Ohm).** For each of the three channels the preamplifier structure is that of the single PZ-0: the expected performances are the same obtained with the SUB and with the prototype detectors in LNGS.
- **Enhanced radio-purity**: no ceramic carrier is used for the ASIC. Bondings will be made directly on the PCB. A radio-pure sealed copper cap should provide EM shielding and isolation of the ASIC from liquid Ar. All resistances are of 0402 size (smallest).
- **Enhanced FET’s breakdown hardness**: protection diodes added at the FET input. During tests with prototype detectors at LNGS the input FETs burned out several times (probably owing to a strong breakdown of the gate-to-channel junction)
- **Improved scheme for input/output connections**: “up-connector” for 3 power supplies, 3 outputs and 1 test input, “down-connector” for 3 detector inputs.

“T1” PCB: open issues (1)

- **Sealed** (or not sealed?) ASIC **copper cap**

If it is sealed (as we strongly recommend):

- It must be manufactured as one single piece
- PCB vias under the cap must be closed
- It acts as EM shield and provides isolation of the ASIC surface from liquid argon

If it is NOT sealed:

- It can be manufactured as a simple “open” structure
- PCB vias under the cap can be left open
- It acts as EM shield ONLY and does not physically protect the ASIC surface from liquid argon

“T1” PCB: open issues (2)

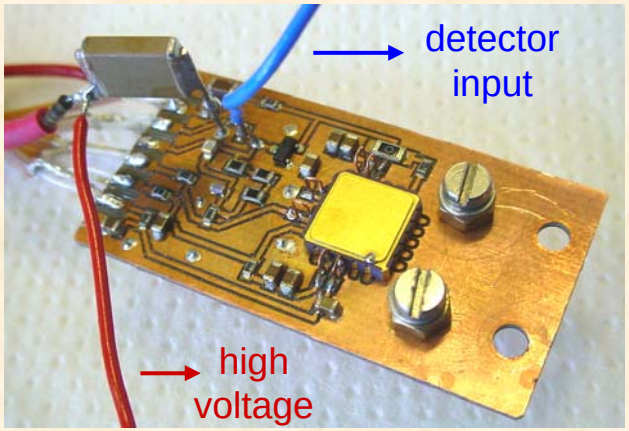
- **Mechanical stress** on the copper cap after one or more thermal cycles has to be tested.

- **Cross-talk** between the 3 channels has to be tested (the PCB has been designed in order to reduce it as much as possible).

- **A possible cut of the filtering capacitances count** (at the expense of the electrical properties) has to be tested in order to enhance radio-purity. Separate filtering of power supplies has been now implemented for each channel of the ASIC.

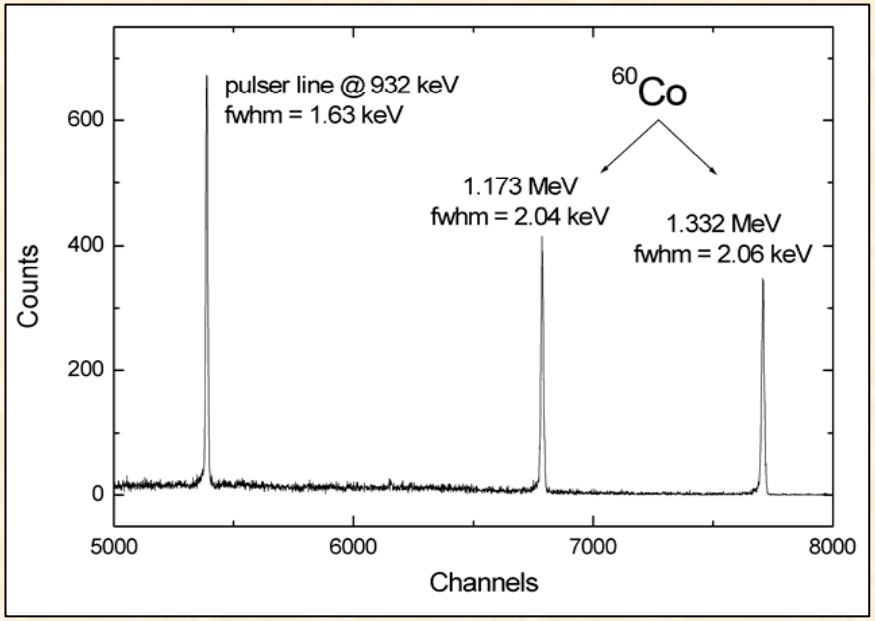
If the noise performance will not be compromised, the overall number of surface mount devices may be reduced of 10.

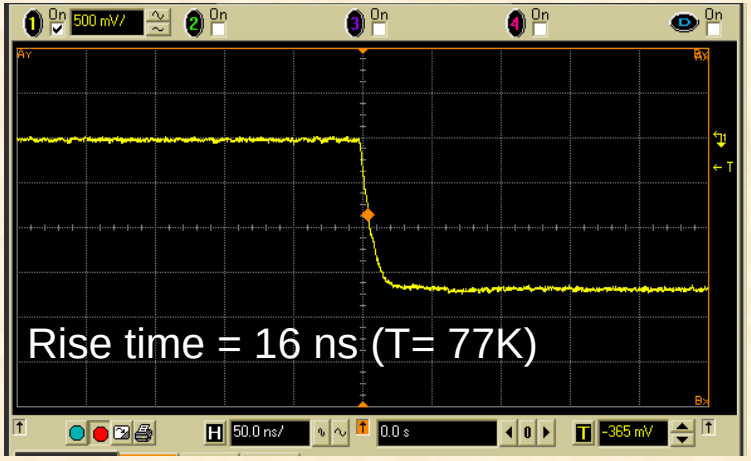
“S1” home-made (Milano) PCB for 1-ch PZ-0



	T = 77 °K
Energy sensitivity (C_F = 0.2 pF)	~ 290 mV/MeV at preamp output ~ 217 mV/MeV after 150Ω termination
Negative output voltage swing	~ 2.5 V
Input dynamic range	~ 8.6 MeV
Rise time	~ 16 ns with ~ 10m coaxial cable
Fall time	~ 250 μs (R_F = 1.2 GΩ)
Resolution at τ = 6μs	2.25 keV @ 1.332 MeV (^{60}Co) 1.6 keV @ 932 keV pulser line
Power required	23.4 mW (V_{FET} = +4V I_D = 3mA V_{CC}= +3.6V V_{EE} = -2.8V)

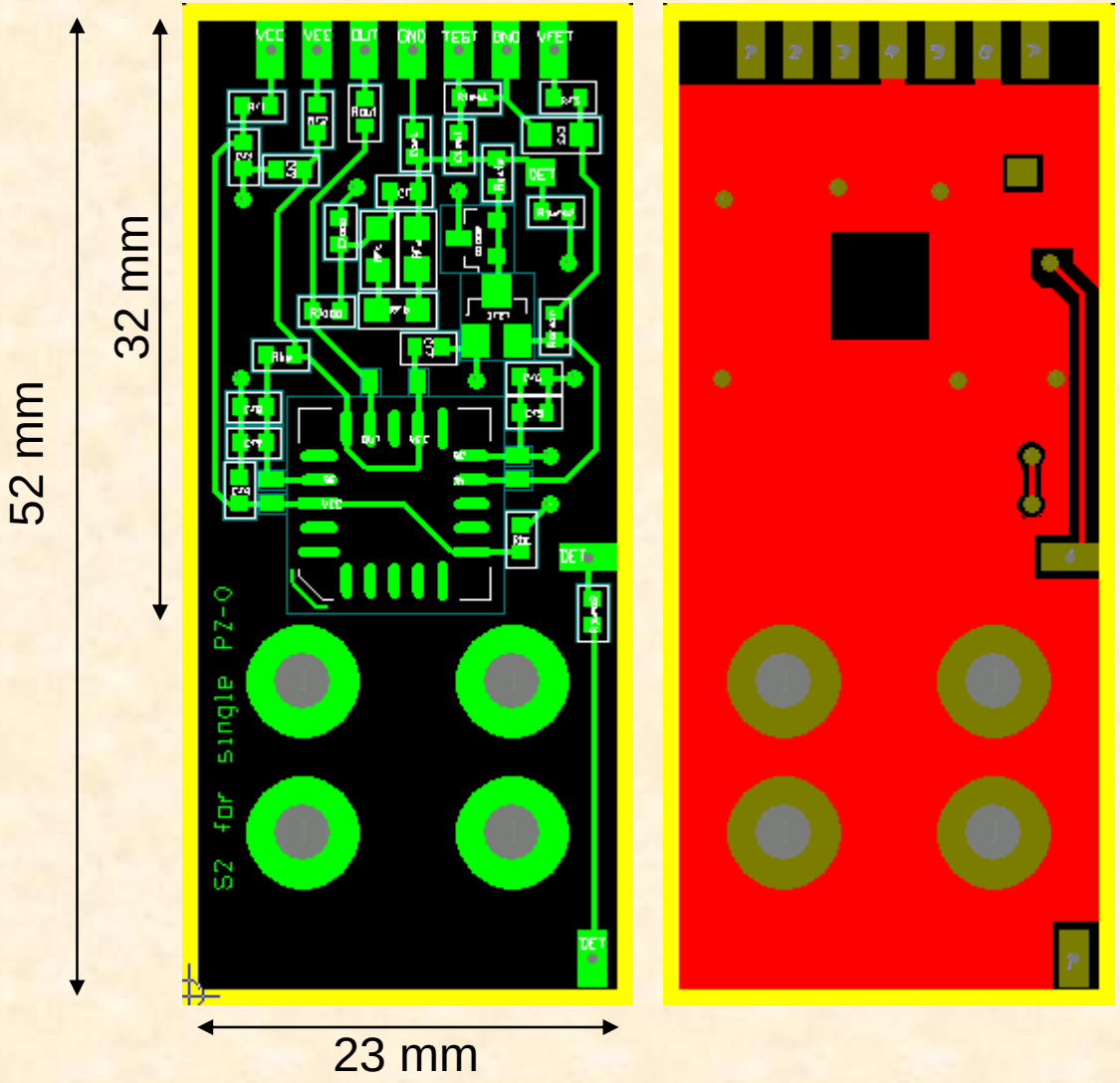
Measurement performed in Milano, April 2008, with SUB detector





New “S2” PCB for 1-channel PZ-0

TOP LAYER **BOTTOM LAYER**



The main structure is the same as old S1 PCB (ceramic carrier for the ASIC)

New features:

- protection diode for the input FET
- new up-connector with ground pins
- new detector input on the lateral or on the bottom side of the PCB
- ground plane removal below feedback resistors (to reduce stray capacitances)

Time schedules

3-channel T1 PCBs:

- 18 Oct. 2008: gerber files of T1 PCB ready. INFN-Mi Bicocca in contact with TVR company for production
- Production of the first 5 samples (for mechanical and electrical tests in liquid nitrogen/argon)
- 2-3 weeks: bench-test of the samples
- Production of 25 3-channel T1 PCBs
- 2-3 weeks: bench-test of all PCBs
- March 2009: PCBs ready

1-channel S2 PCBs:

- 5 Nov. 2008: gerber files of S2 PCB ready. INFN-Mi Bicocca in contact with TVR company for production of 15 PCBs.