PCI based DDAQ

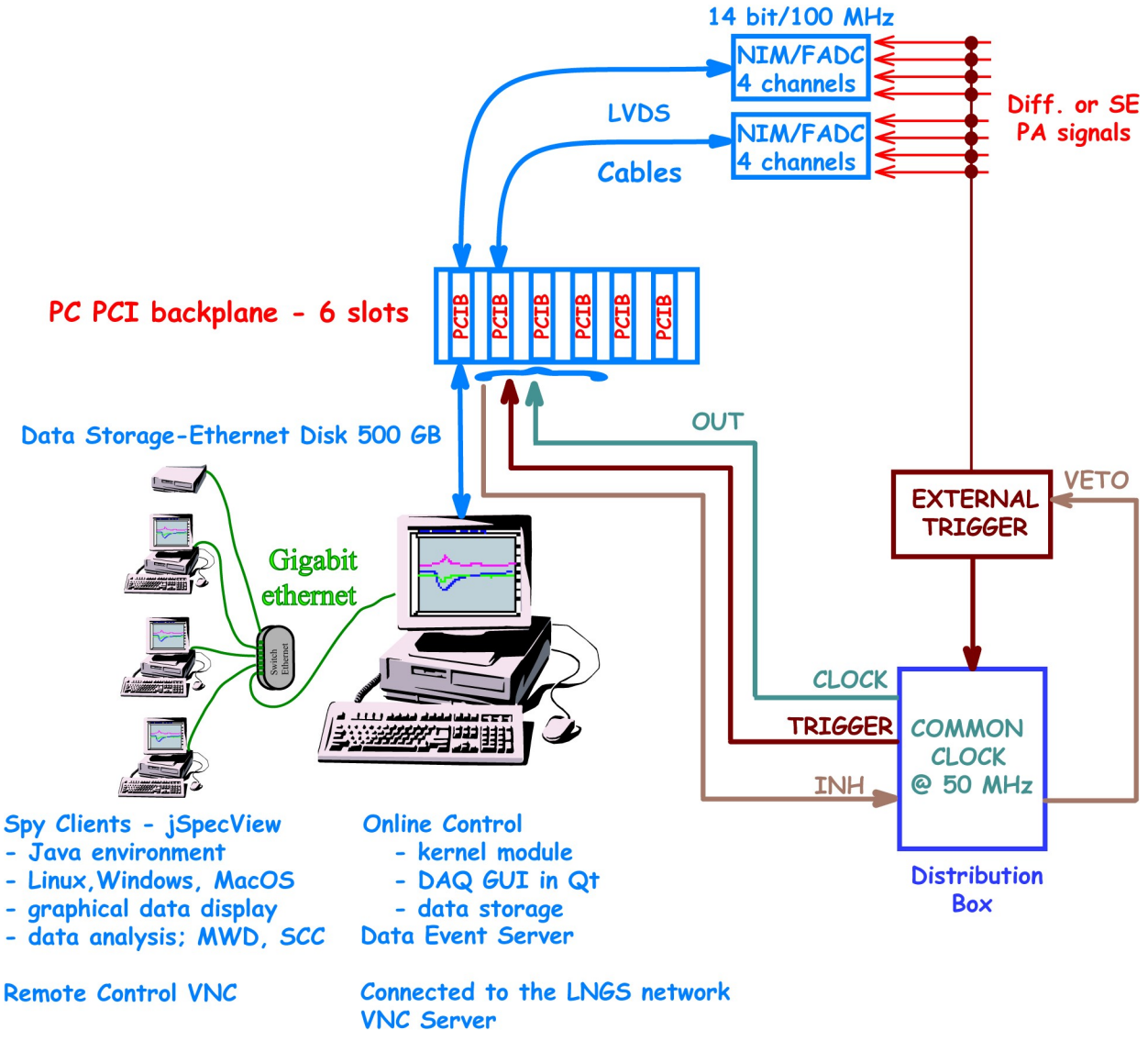
status and perspectives

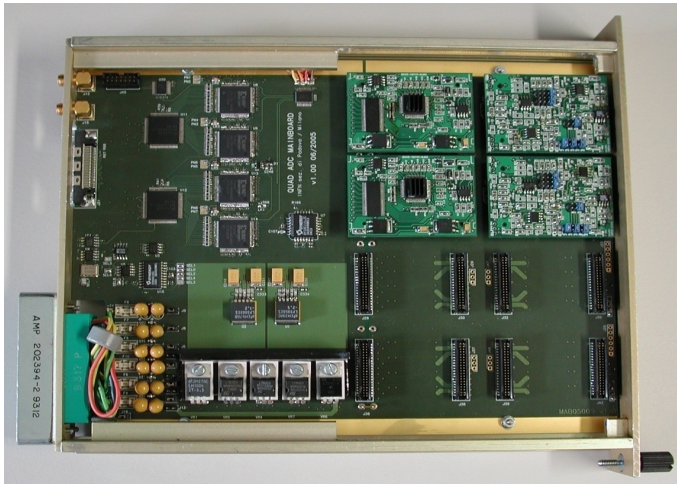
INFN Padova

INFN & University Milano

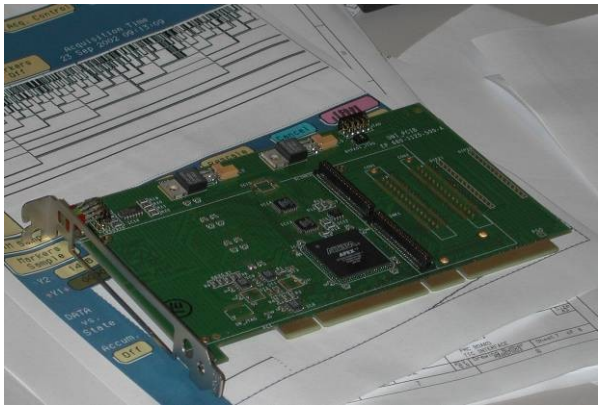
Calin A. Ur

Installed at LNGS



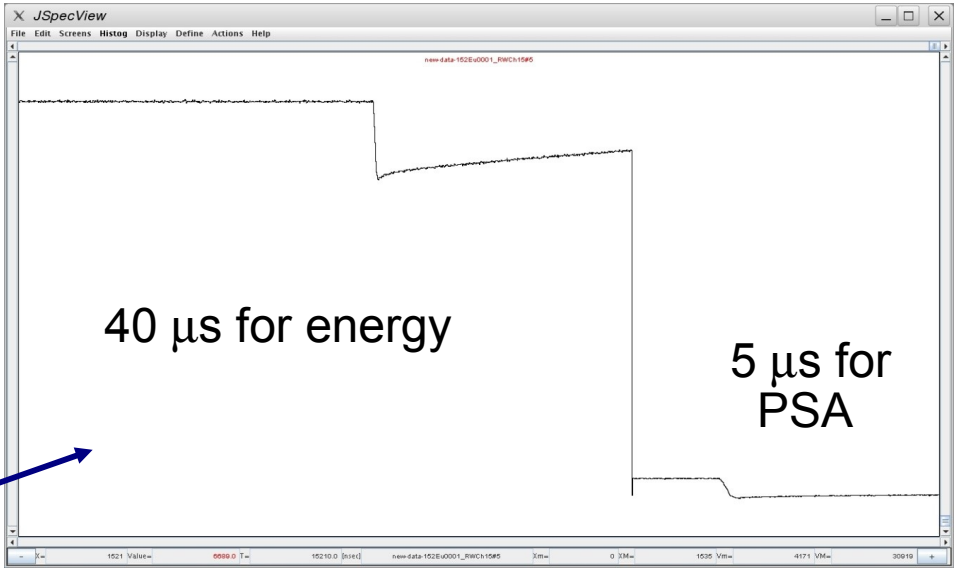


ALTERA APEX
20K200EFC484



Main features

	MD2S Padova
Channels	4/module
FADC bits	14
FADC rate (MHz)	100
FPGA k-gates/ch	100
Internal trigger	no
Trace length (samples)	1024 @ 25 MHz 512 @ 100 MHz
Control & i/f	NIM/PCI
Data xfr	PCI 32bit/33MHz
Max output rate (MB/s)	6



Obsolete Core PCI

Interrupt based RO

Data transfer improved

Upgraded to the latest ALTERA core PCI

- implemented DMA RO → success

- updated the core PCI → PCI transfer at 32bit/66MHz

  → max.output rate > 60 MB/s (calibrations) – limited by the HD write speed

- added: 64 bit clock counter @ 100 MHz / NIM module
  32 bit trigger counter

system running test measurements

- forced synchronization of data transfer from several boards

  → 1 master PCI board – produces the irq request

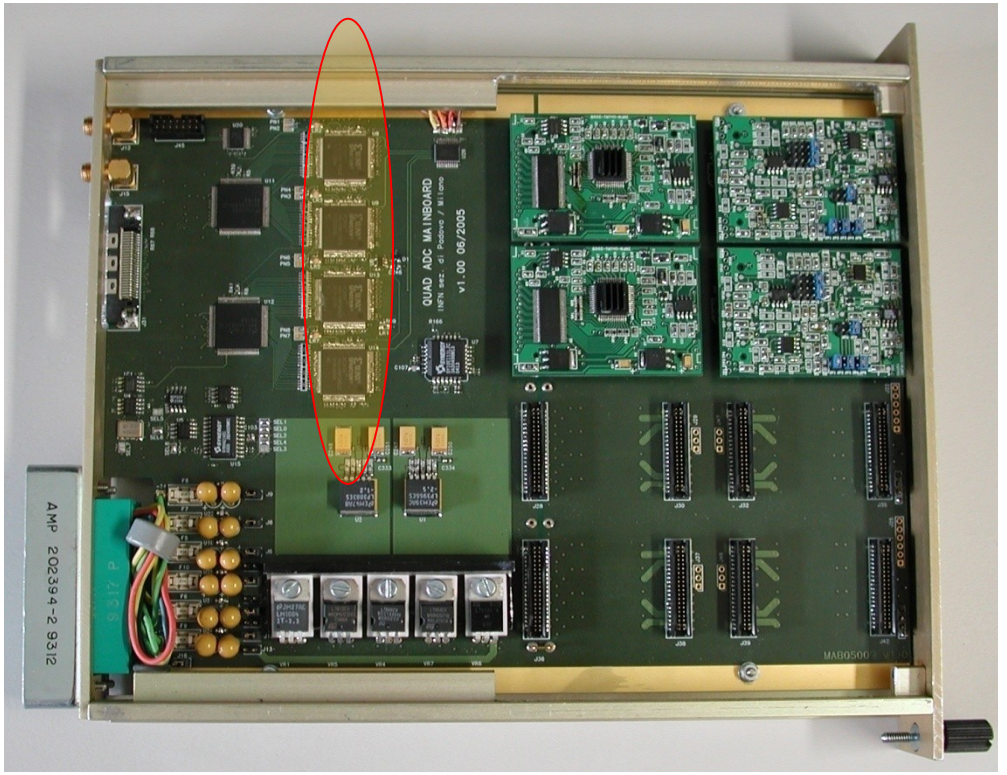
  → slave PCI boards – notify the master board when transfer is finished

Internal trigger

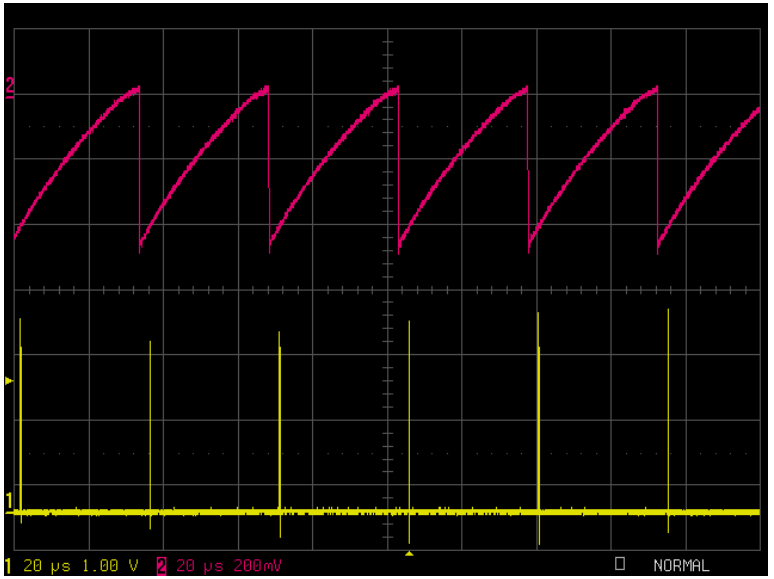
- implemented in the Xilinx FPGA's on the NIM boards
- simple algorithm – dual delay line
  – triangular filter
  – signal offset removal
  – independent of the signal height
  – low energy threshold
- threshold programmed from PC
  via parallel port
- individual output trigger signals TTL

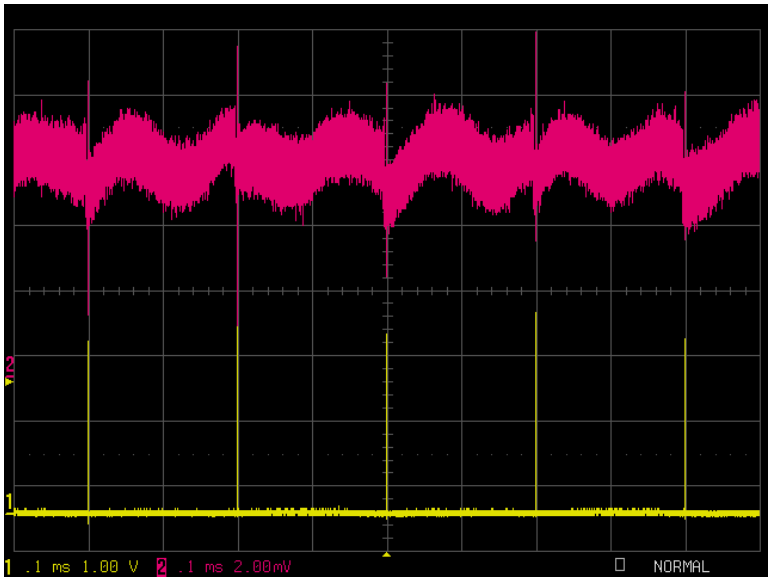
- eliminates the need of splitting the signals from the Ge detectors

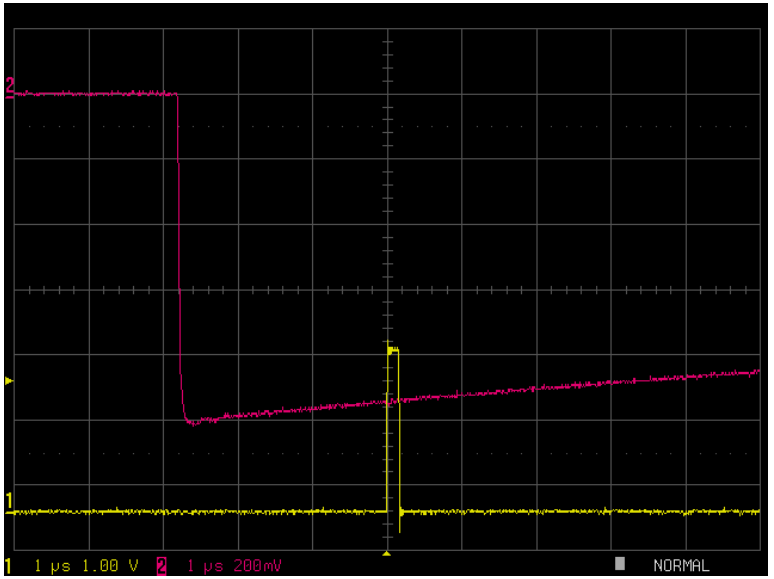
- simplifies the trigger electronics needed for starting the DAQ

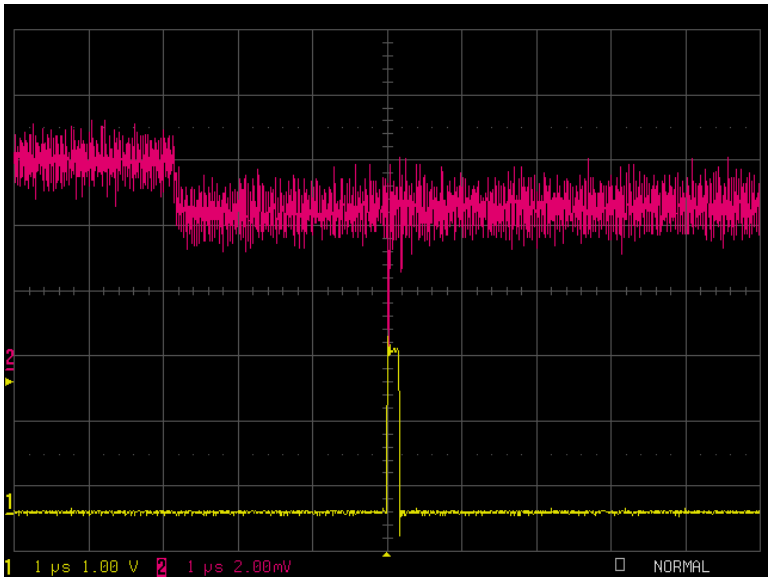


Some sample images

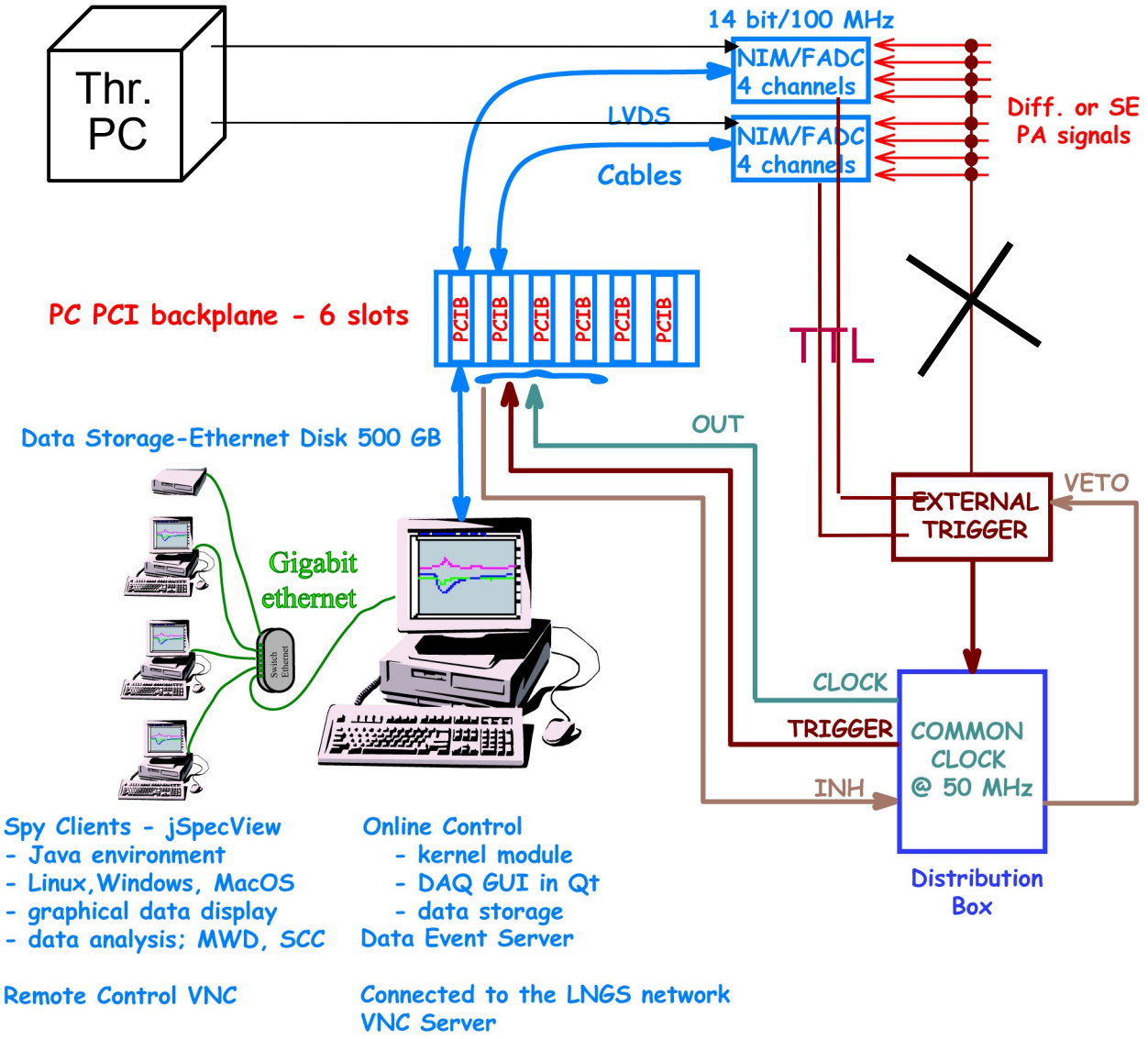








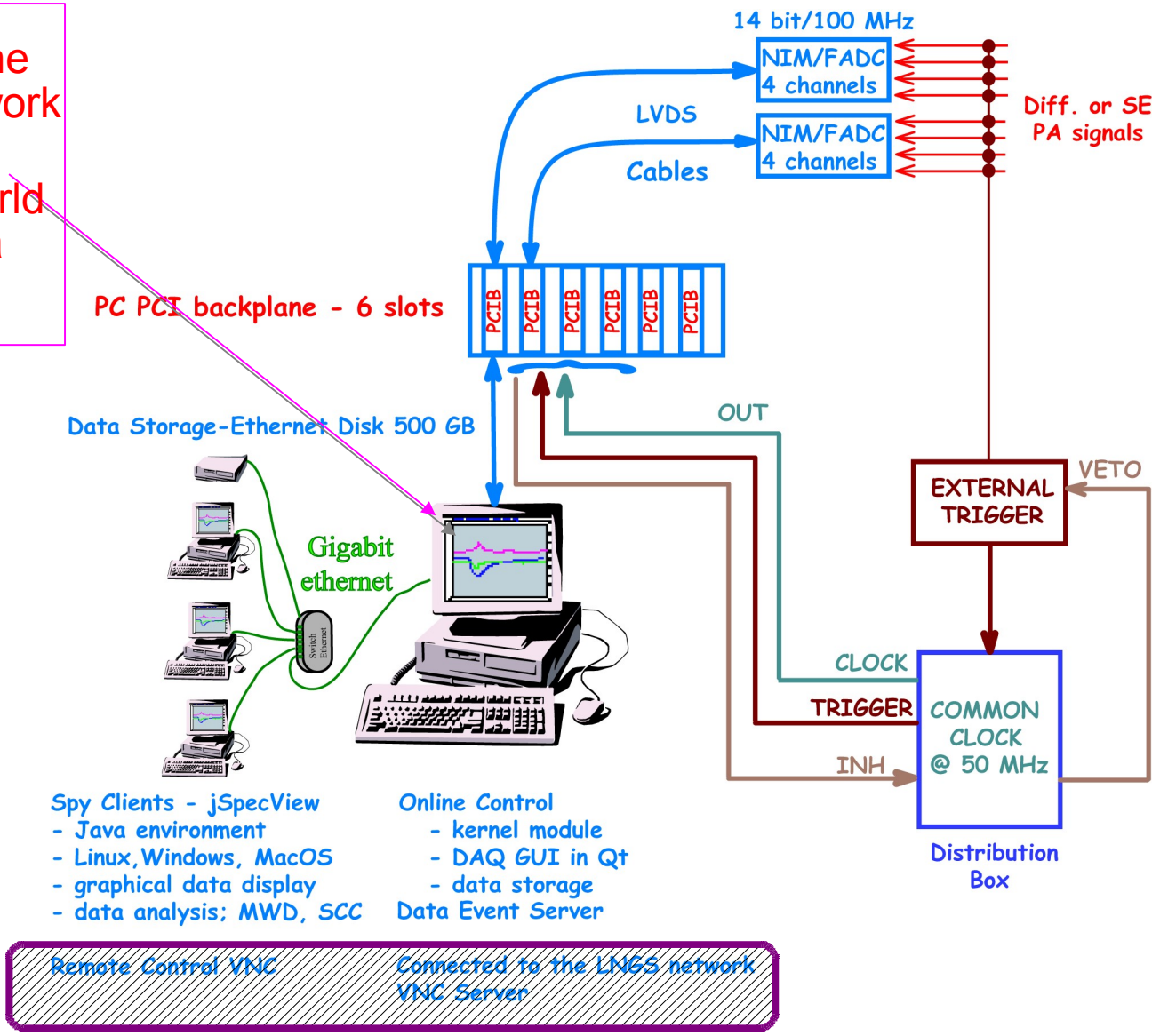
New DAQ layout



Remote control

Visible to the LNGS network

Outside world tunnel via a local PC



Data format

```
***************
HEADER  (ASCII)
***************
?PCIDAQ0  data label
?CHN0003  number of enabled channels
?WVN0002  number of waves for each channel (1 or 2)
?P101024  number of bins in the first wave (fixed)
?P200256  number of bins in the second wave
?D103000  how many 10 ns after trigger in the first wave
?D200450  how many 10 ns after trigger in the second wave
?SPR0016  output sample precision in bits
?BIT0014  number of FADC conversion bits
?FRQ0100  sampling frequency in MHz
?LTR0020  event trailer length in bytes
?CH10002  channel #1 Enable Pattern 0000000010
.........(channel #1 of card #2 is enabled; card #1 is LSB)
?CH20000  channel #2 Enable Pattern 0000000000
.........(no channels #2 enabled)
?CH30001  channel #3 Enable Pattern 0000000001
.........(channel #3 of card #1 is enabled)
?CH40002  channel #4 Enable Pattern 0000000010
.........(channel #4 of card #2 is enabled
?JHZ0100  frequency of jiffies (100 Hz) depends on the OS
?RUN0007  run number
?ORIGDAT  original data
?U000029  user comment length (in bytes)
"Data Conmment with User Comment Text"
"new lines"
"............." up to 512 characters
?ENDHEAD end of header
```

Data format

```
***************
Data
***************
1st Event:
 Number_of_Channels_Enabled * ......................... 3
 Number_of_Points_wave_1 * sizeof(u16) + ...... 1024 * 2
 Number_of_Points_wave_2 * sizeof(u16) + ....... 256 * 2
 Event_Trailer_Lentgh = ............................... 20
 Event_Length = ..................................... 7700 bytes
```

Event Trailer Format - 5 x u32 integers = 20 bytes
#0 = Trigger counter (Event ID)
#1 = Time stamp high
#2 = Time stamp low
#3 = data acqusition time measured in jiffies (10 ms)
#4 = End Of Event = 0xFFFFFFFF

2nd Event: ....

Future work

- modify all the boards for the trigger signals extraction
  - electronics workshop – INFN Padova

- thorough tests of the newly implemented features

- define the event format

- integration: – muon – veto system

  – ^{nat}Ge veto

Collaborators

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Electronics workshop – INFN Padova