Results of cold charge sensitive preamplifiers tests with SUB detector.

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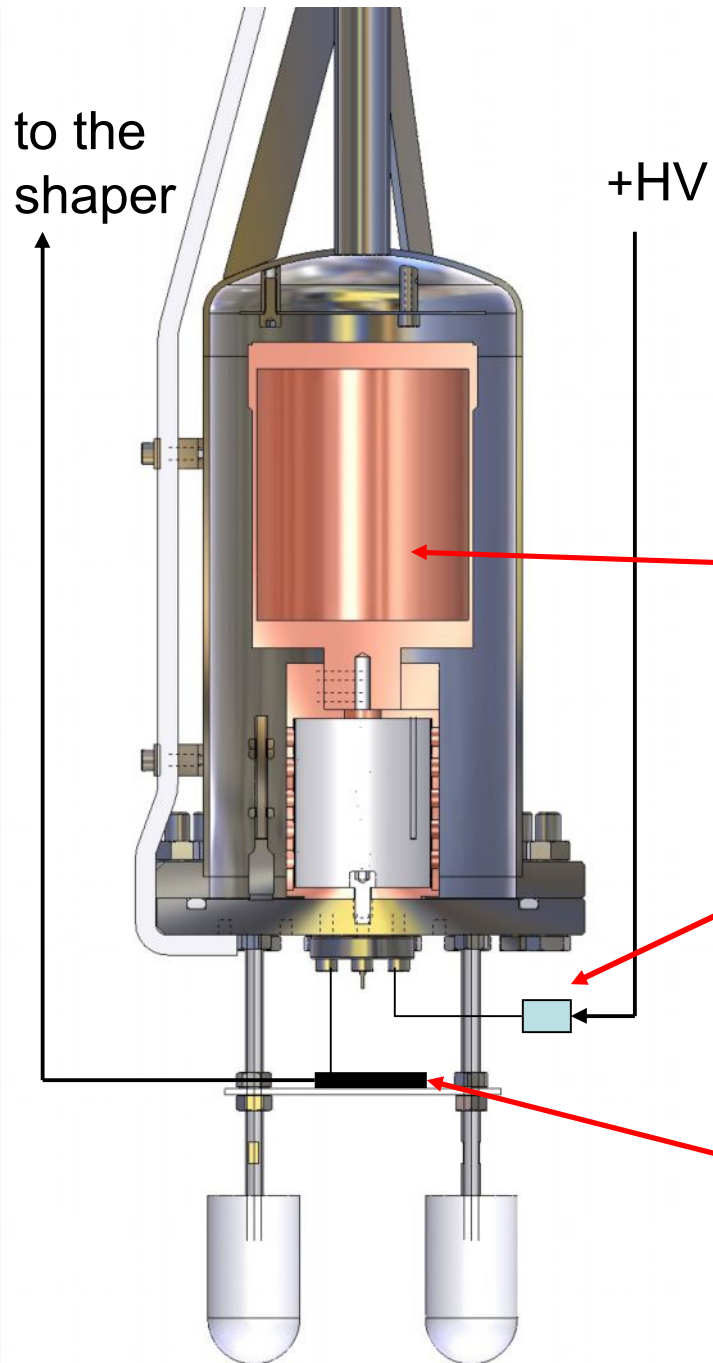## Outline

•Purpose of the work: Test of FE circuits in the same condition for comparison and final choise
• Circuits tested:

-IPA 4
-CSA 77
-PZ 0
-SR 1
} Phase I candidate preamplifiers

• Description of front-end circuits: technology, electrical characteristics and components
•Test performed: cold FE electronics readout at INFN Milano with the SUB detector
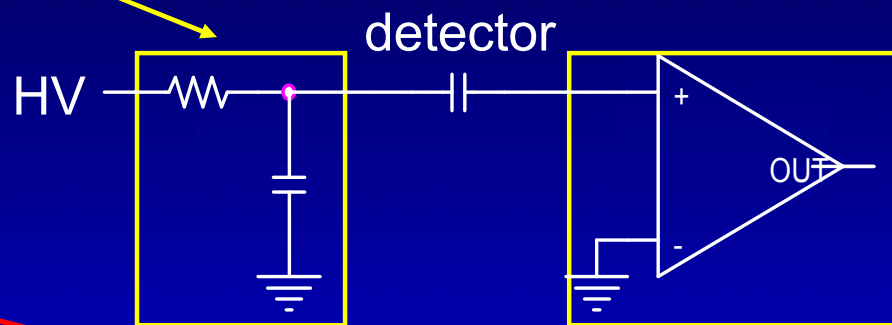
The SUB bench Test

Cryogenic setup:
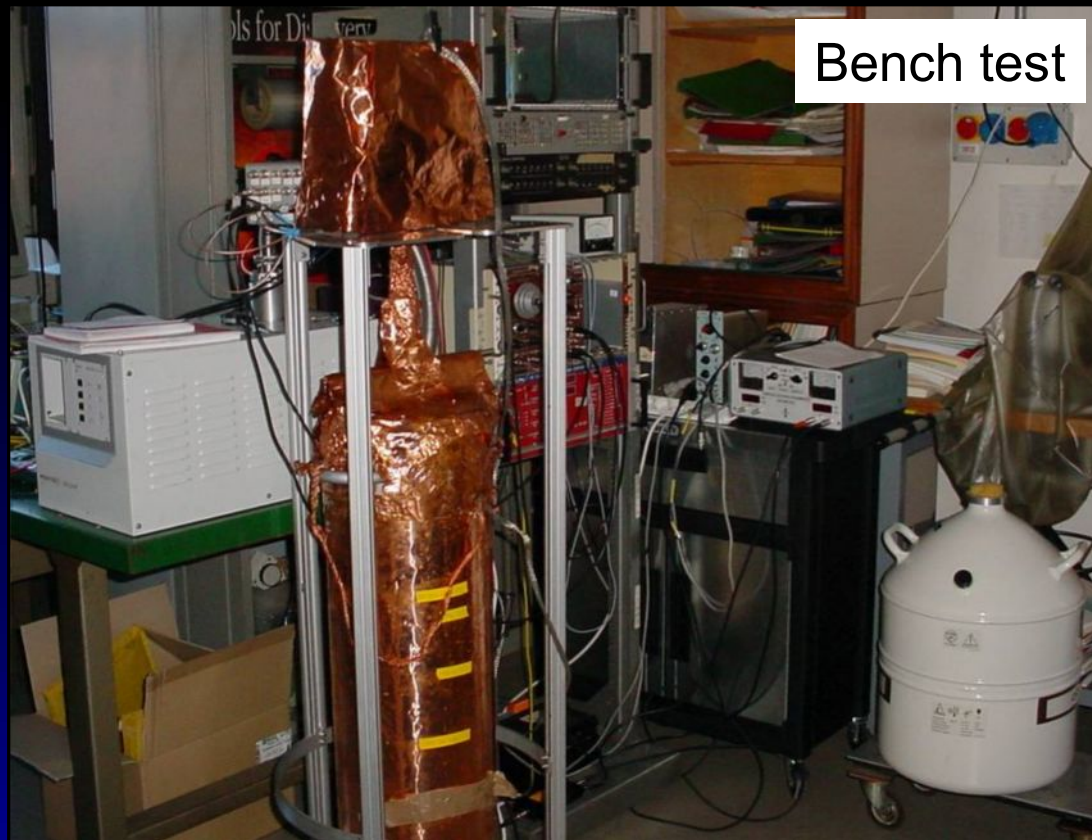both Cryostat and FE electronics directly immersed in LN

- HPGe Detector, p-type
- Outer contact: HV=2500V
- Inner contact: Read-out electrode
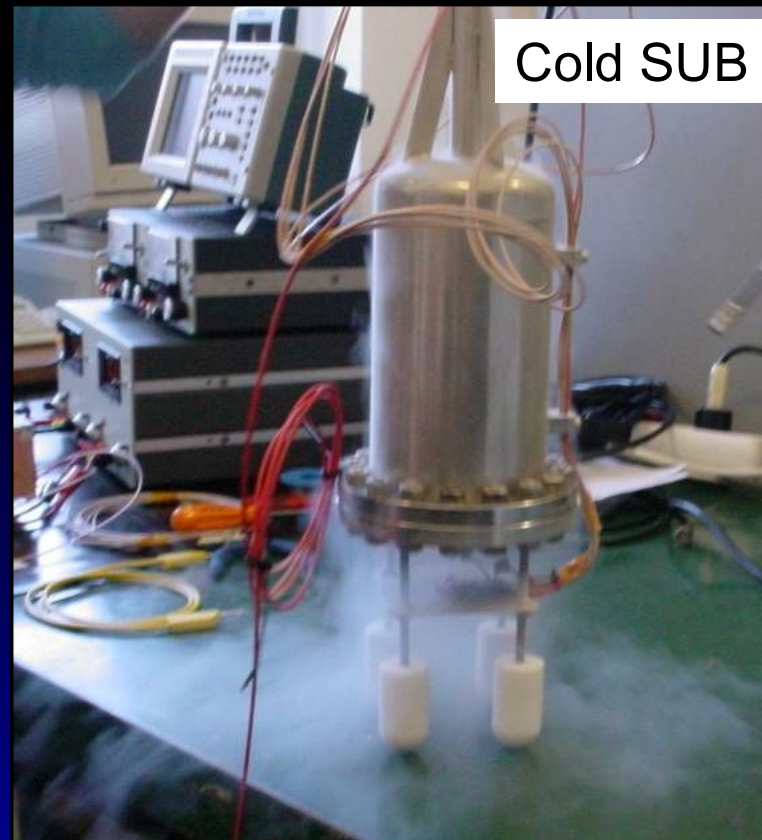
HV filter to reduce high-frequency noise

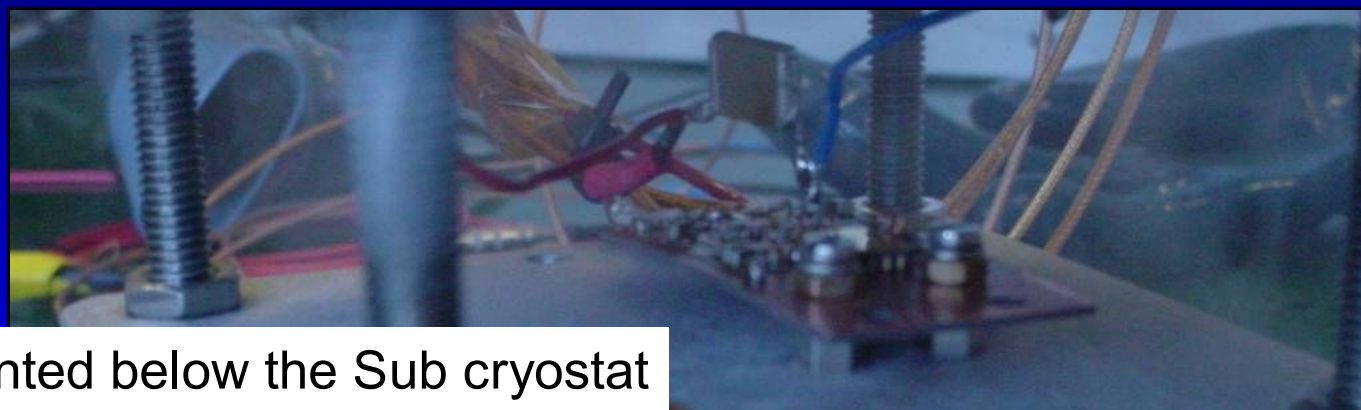Circuit under test:
DC coupled

to the shaper

+HV

detector
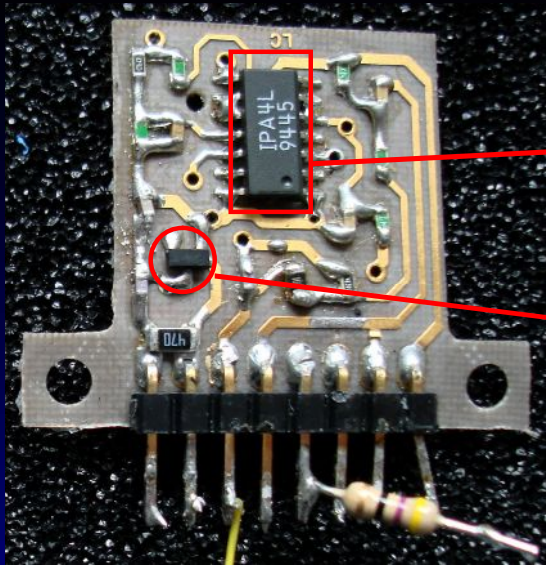
HV

OUT

The Sub at Mi University

Bench test

Cold SUB

PZ0 mounted below the Sub cryostat

Phase I Candidate preamplifiers
IPA4+BF862 (cold) + II stage (warm)

IPA4+BF862

Technology: n-channel monolithic jFET
Components
- IC: IPA4
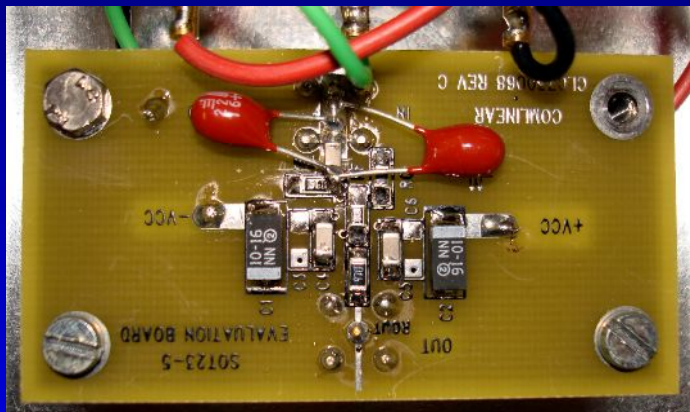
- External:
    - BF862 FET
    - Feed-back network
    - low voltage power supply filters (RC)
    - Test Capacitor
    - Resistors & Capacitors for biasing
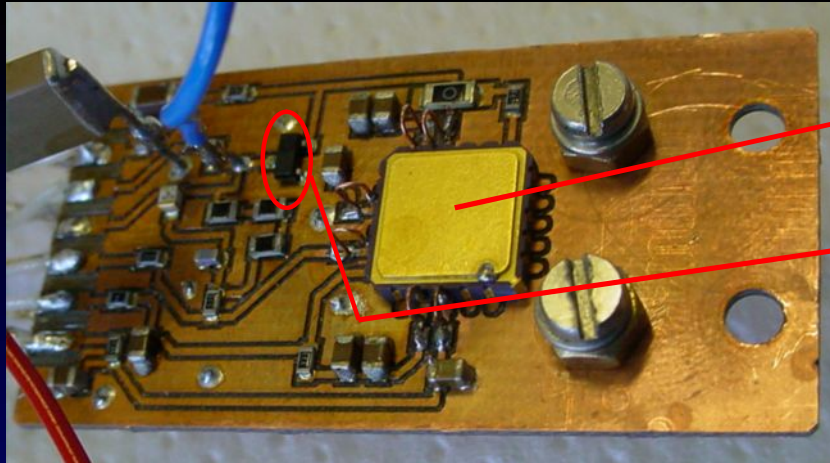
II Stage

Circuit used to reduce IPA4 offset output voltage, give an additional gain and drive 50 Ohm devices

Phase I Candidate preamplifiers

PZ0 (CSA with external input transistor)
Technology: AMS HV CMOS 0.8μm CZX chip on PCB

Components:
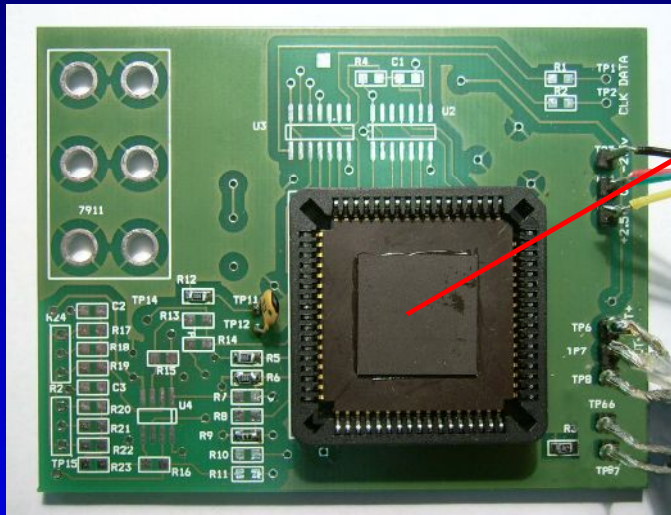- IC
- External:
  - BF862 FET
  - feed-back network
  - low voltage filter capacitors
  - Test Capacitor
  - 2 Resistors for chip biasing
  - 1 Resistor for FET biasing

SR1 (CSA with integrated input transistors)
Technology: AMS HV CMOS 0.8μm CZX chip on PCB

Components:
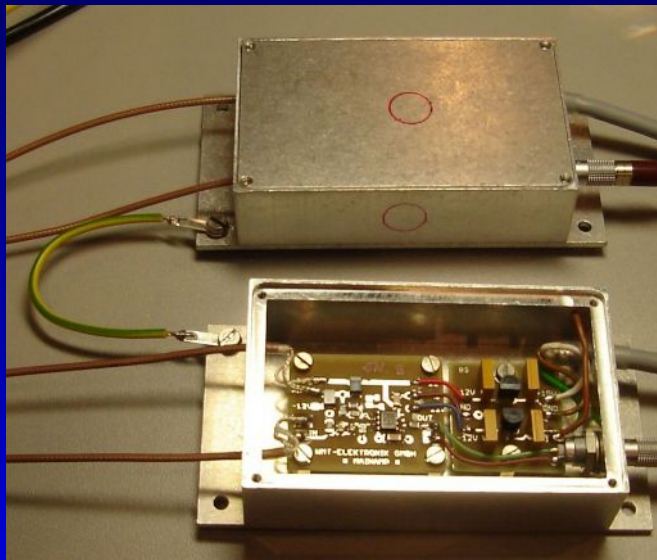- IC
- External:
  - feed-back network
  - low voltage filter capacitors
  - Test Capacitor
  - Resistors for biasing

Phase I Candidate preamplifiers
CSA77 (cold) + Main amplifier (warm)
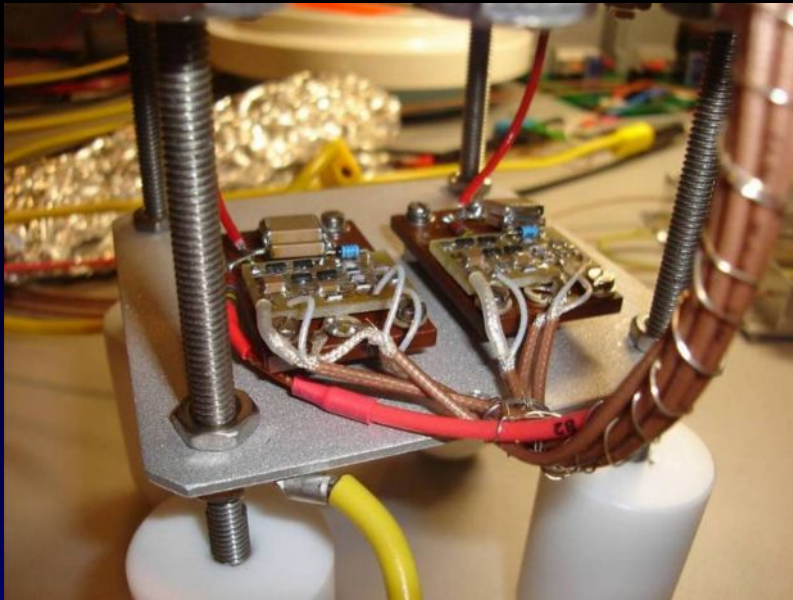
CSA77
Components: 4 BF862 + resistors and capacitors for biasing and filters

Main Amplifiers
Circuit used to make pole-zero compensation, give an additional gain and drive 50 Ohm devices

GERDA FE electronics testing in Milano
Results of tests with Ge-diode, preamplifiers immersed in LN.

Preamplifier (shaping time)	FWHM [keV] (1.33 MeV γ-line of ^{60}Co)	FWHM [keV] (electronics contribution)	Rise time * [ns]	Decay time [μs]	Comments
PZ-0 (6 μs)	2.24 [+]	1.62 [+]	~16	~ 250	oscillation problems with 50 Ω termination on output, 150 Ω is ok
SR-1 (8 μs)	3.07	2.55	~30	~250	preamplifier bias voltage reduced to reduce bias current
CSA-77 (10 μs)	2.64	2.02	not measured nominal at room T: 11ns	~210	gain drift: oscillation of ~5 channels/hour, stabilised after few hr
IPA-4 (6 μs)	2.38	1.80	~100	~320	results with 2nd stage amplifier

* rise time was measured with ~10m long coaxial cable on the signal output
[+] values are averages of more low-statistic measurements (no long time measurement was performed with ^{60}Co or pulser)

GERDA FE electronics testing in Milano
Electronic characteristics

Preamplifier	LV bias [V]	Power [mW]	Driving load [Ω]	Cable between 1st and 2nd stage [m]	Energy sensitivity [mV/MeV]
PZ-0	+4.7 (FET) +3.6 (CC) -2.7 (EE)	23.4	150	-	~217
SR-1	+2.2 -2.2	?	50	-	~82 [+]
CSA-77	+12 -12	?	50	1.4	~54
IPA-4	+12 -3.4	~100 ?	50	1.8	~46 *

[+] measured at room T, with the first version of the cirquit

* without second stage

Ge-diode characteristics: readout with DC-coupling
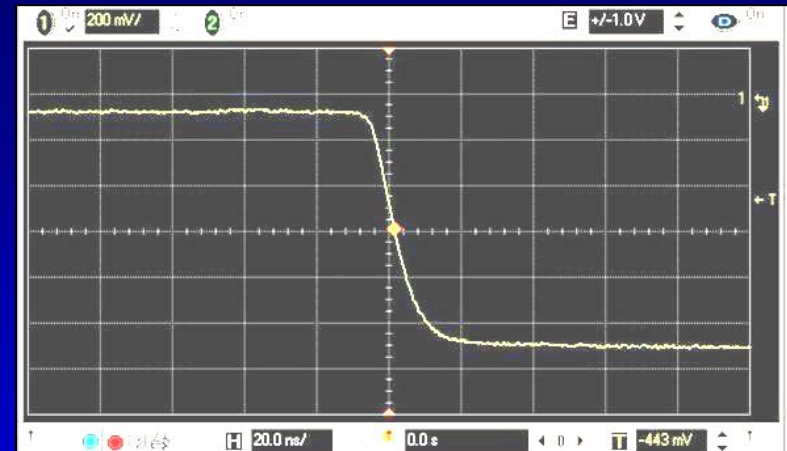nominal HV (full depletion) = 2.5 kV
capacitance when depleted = ~70 pF

Performances with COLD FE: PZ0

Comparison between **noise measured** at room temperature (T=300°K) and in LN (T=77°K)

Best resolution obtained with (encapsulated) prototype crystal and cold PZ0 CSA
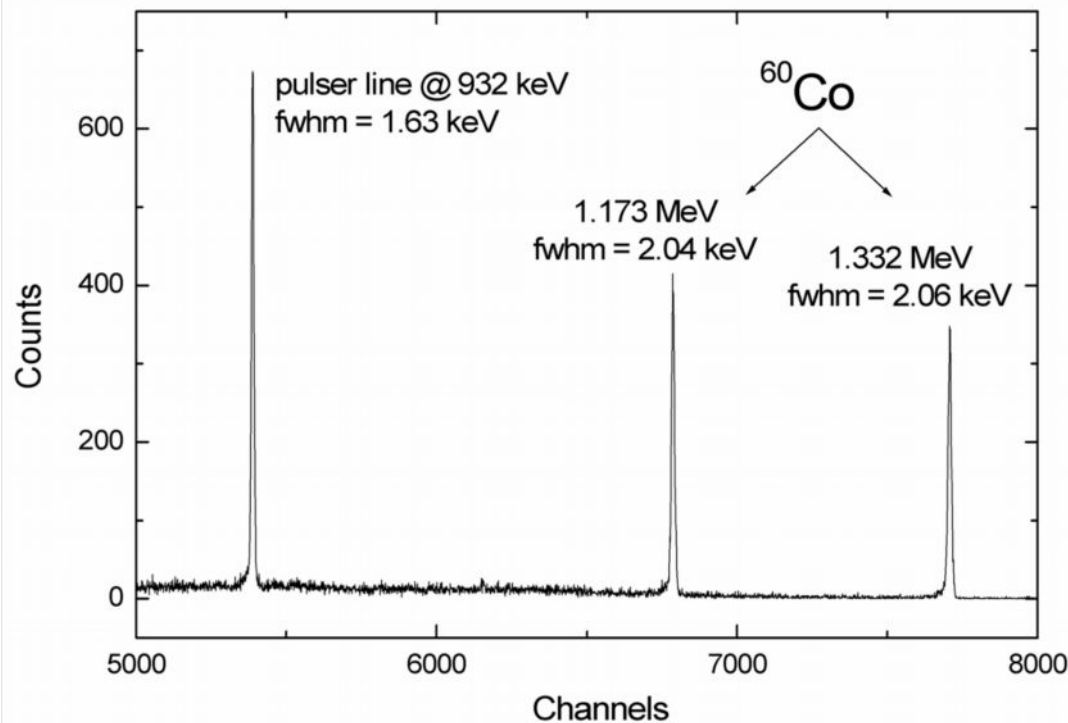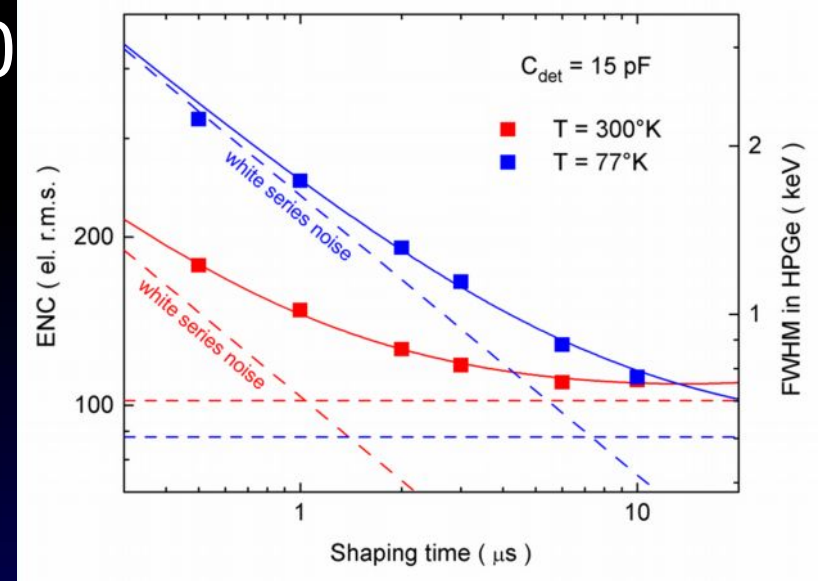
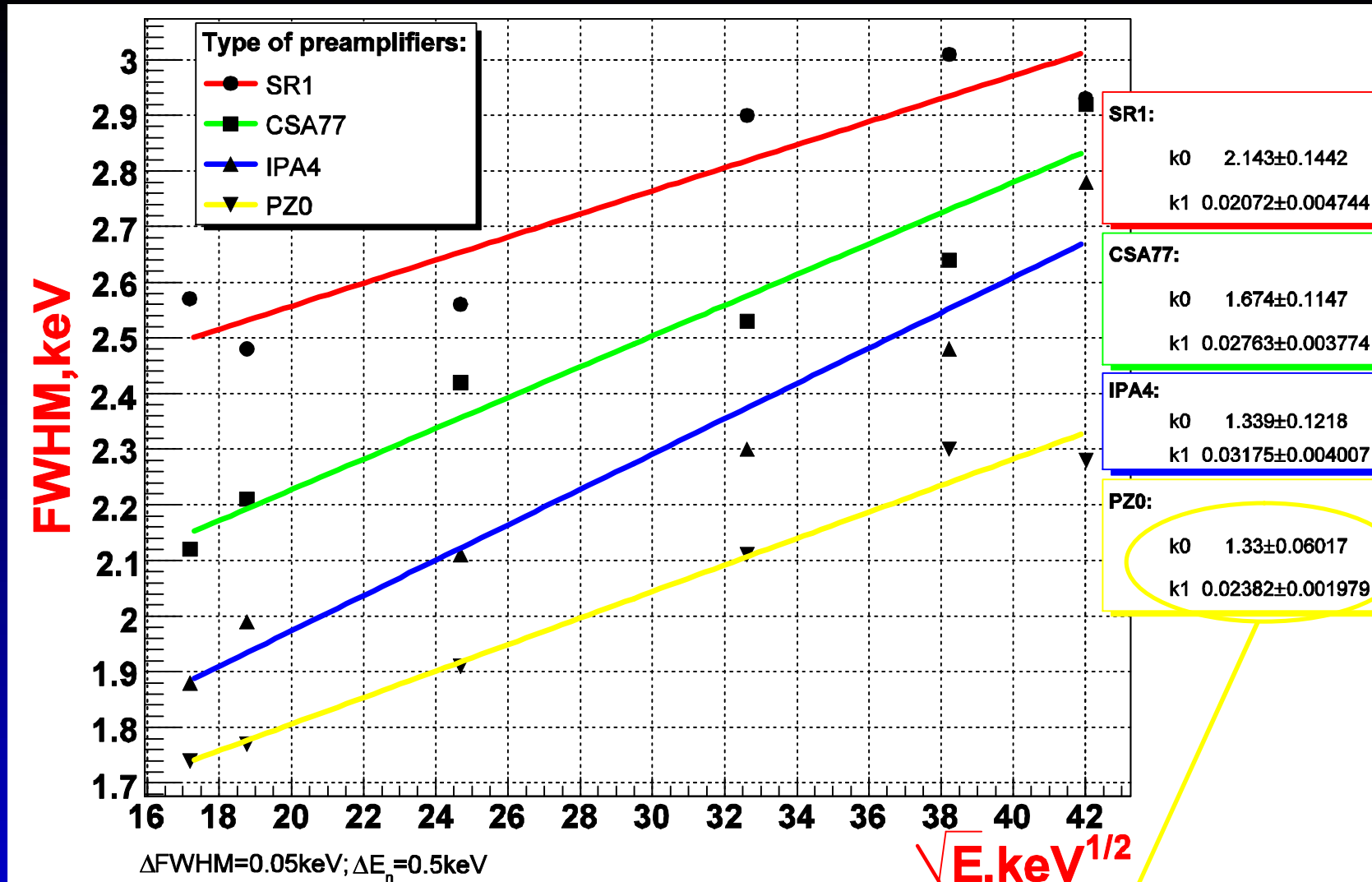**Acquired output signal** driving a 50 Ω coaxial cable of ~ 10 m : rise time of ~ 15 ns

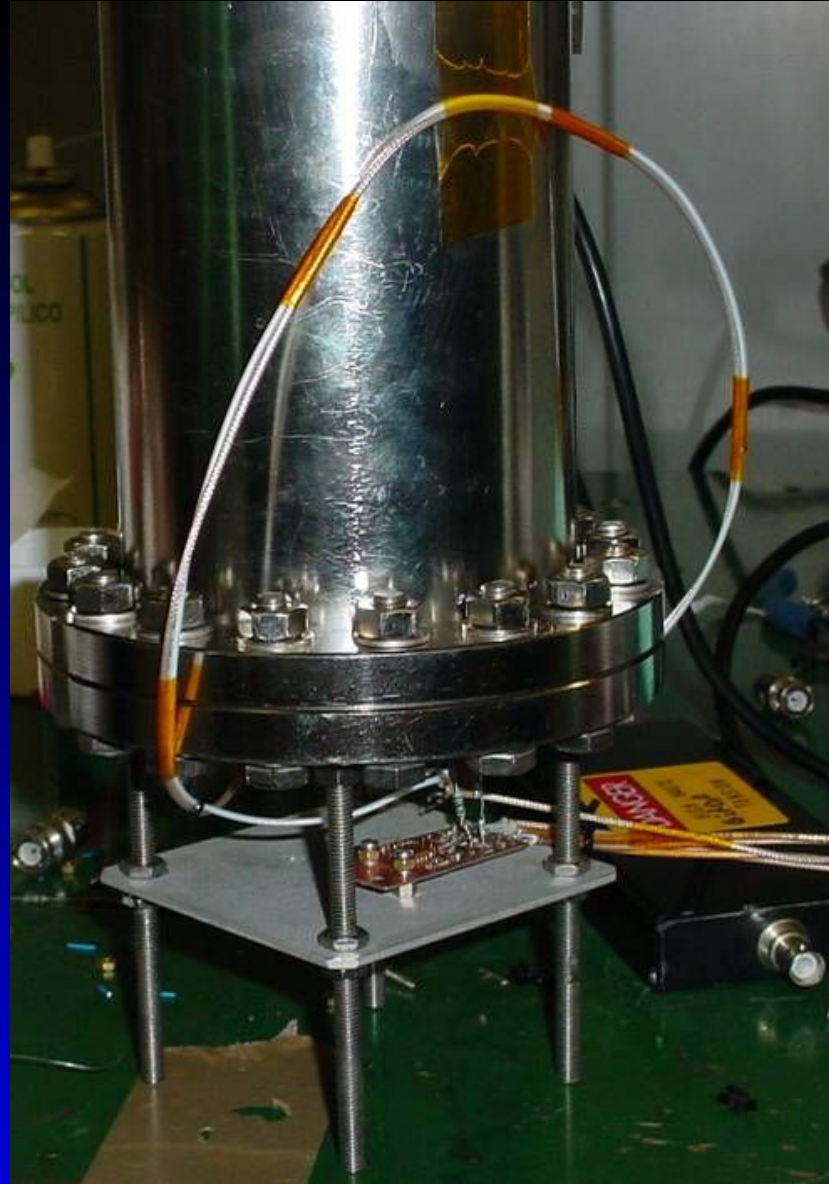Estimate of intrinsic noise of FE circuits starting from a background analyis

$$FWHM = k1 \cdot \sqrt{E} + k0$$

PZ0 is the circuit with less intrinsic noise

PZ0: Test with 50cm cable on preamp-input.
Purpose: simulate effect of cable length from bottom crystal in string to CSA location (top of string)

- increase of sensitivity to microphonics, RF pick-up and resonant disturbances in cirquit
- rise time worsening -> 25 ns
- resolution worsening:

  ^{60}Co: 2.24 keV -> 2.5 keV

  pulser: 1.62 keV -> 1.9 keV

Euroball capsule new test bench
(Ge capsule of former Euroball experiment)

Definitive Location: LNGS Autorimessa 2

- Setup renewed (dewar, filling lines etc.)
- New dewar (80 l) low LN/LAr loss (less than 1 l/h compared to 1.6 l/h old dewar)
- Cooling down speed regulated by a winch used to slowly lower the detector (8-10 h to cool down safely) and a cold finger
- Cooling down procedure (with a new dewar) repetible, reproducible and working
- 1 cooling cycle performed (detector is cold in these days).
- Resolution at pulser 1.6 keV

Conclusions

- From the comparison of the circuits tested, PZ0 is the best one, from the viewpoint of energy resolution and of timing.
- Possibility to make PSA with discrimination of multi-site events and single-site events.

Purposes of the bench test

- Test of fully integrated FE circuit (SR1).
- Integration of SiPM (Silicon Photomultiplier) readout with Ge detector readout.
- PSA (development of algorithms) with a fast FE circuit SR1 coupled to a Ge detector.