TG3 Status Report

On behalf of TG3 working group

Outline

- AGATA preamps. No change since last report.
- IPA4. News: equipped with external FET and 100 Ohm output stage. Solution ready for prototypes read-out (N of board need TBD). Availability of integrated chip as die and mounted in SOIC14 ~ 80 pcs (or more).
- Update of CMOS preamplifier:

  News: F. Zocca

  B. Schwingenheur

- Cabling from FE to Digital electronics

The front-end solutions for GERDA

Existing devices suited for GERDA PHASE I:

- BF862 FET (inside LN bath) + Milano-Agata Hybrid preamplifiers (outside LN bath)
- Integrated monolithic JFET preamplifier IPA4 with internal or with external JFET. (both inside LN bath)
- BF862 + Amptek 250 preamplifier (both inside LN bath)

CMOS Front-end:

- ASIC CMOS Circuits. Probably available for Phase I, necessary for PHASE II
  - Two development: Milano (A. Pullia) and MPI Heidelberg.

Comparison of the three preamps features

	T [K]	Energy Sensitivity [mV/MeV (Ge)]	RT [ns]	ENC_{rms} [n.electrons]	Power [mW]
(AGATA+BF682)[A] short cable	300	150	6.5	145 (τ = 2 µs)	220
(AGATA+BF682)[C] long cable	300 77	150	80	156 (τ = 2 µs) 180 (τ =10 µs)	
(AGATA+BF682)[D] long cable	77	150	33		
IPA4[E]	300	150 (C_f= 0.5 pF)	400 (V_+=12V)	110 (τ =10 µs)	130
	300	75	200 (V_+=12V) 150 (V_+=18V)	114 (τ =10 µs)	
	~77	75	140 (V_+=12V) 60 (V_+=18V)	130 (τ =10 µs)	
	~120	75	80 (V_+=12V) 40 (V_+=18V)	75 (τ =10 µs)	20
AMPTEK 250 + BF862[F]	300	55	27	144 (τ =2 µs)	
	77	55	55	168 (τ =2 µs)	
	120	55	27	100	

[A] C_D = 27 pF, C_f = 1.5 pF

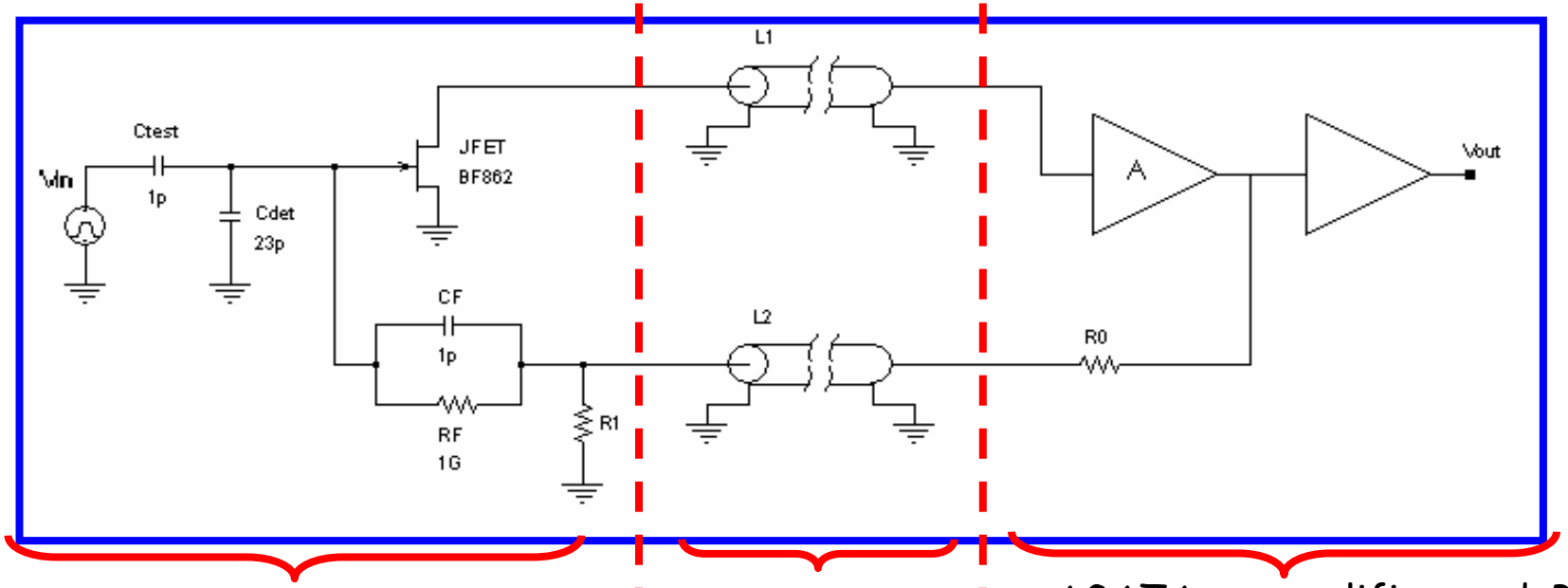
[B] C_D = 23 pF, C_f = 1.0 pF, 2x3 m cable between JFET and preamp, Ccomp=33 pF

[D] C_D = 23 pF, C_f = 1.0 pF, 2x3 m cable between JFET and preamp, no compensating capacitance.

[E,F] C_D = 27 pF, C_f = 1.0 pF

Test of the AGATA preamps tested in the GERDA setup (long cables and FET in LN)

measurements performed { at the test bench
at room temperature (300°K)



- Philips BF862 JFET
- C_F = 1pF , R_F = 1GΩ
- C_{det} = 23pF , C_{test} = 1pF
- R1 (& R0) = termination resistances

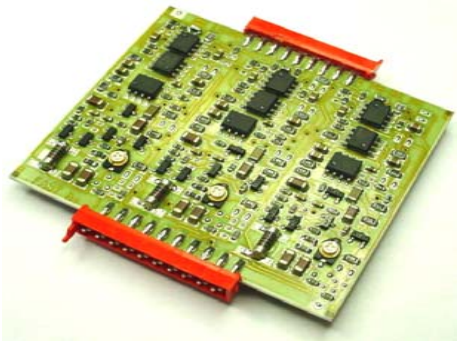
Coaxial cables :

RG62 (93 Ω)

or

RG58 (50Ω)

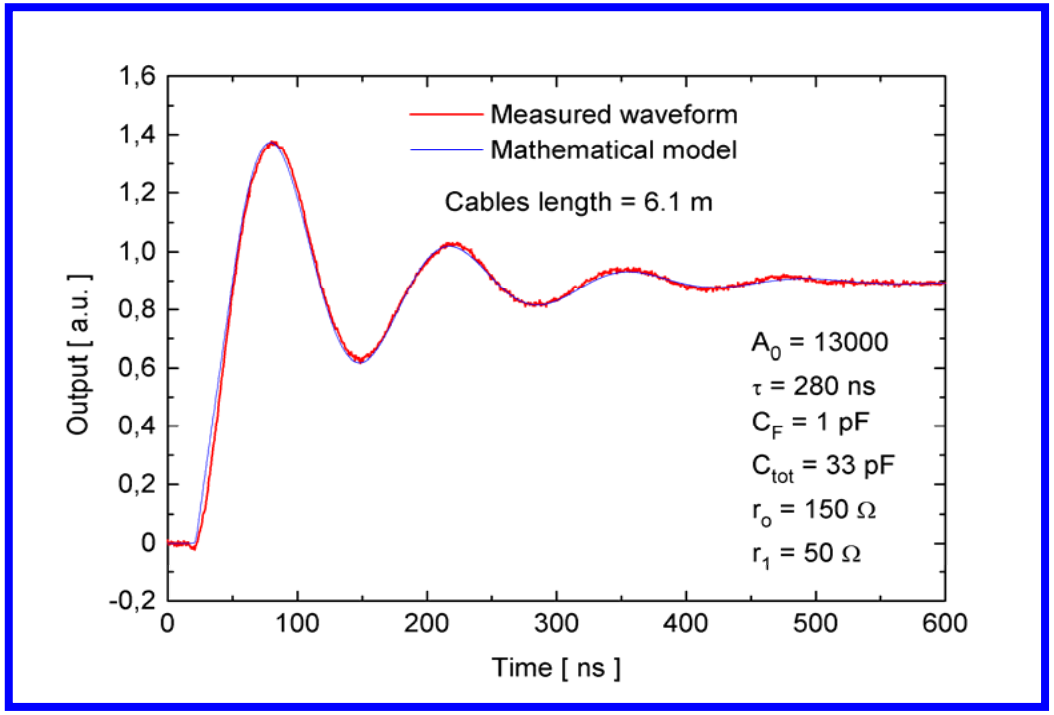
AGATA preamplifier mod. PB-B1



Oscillating response

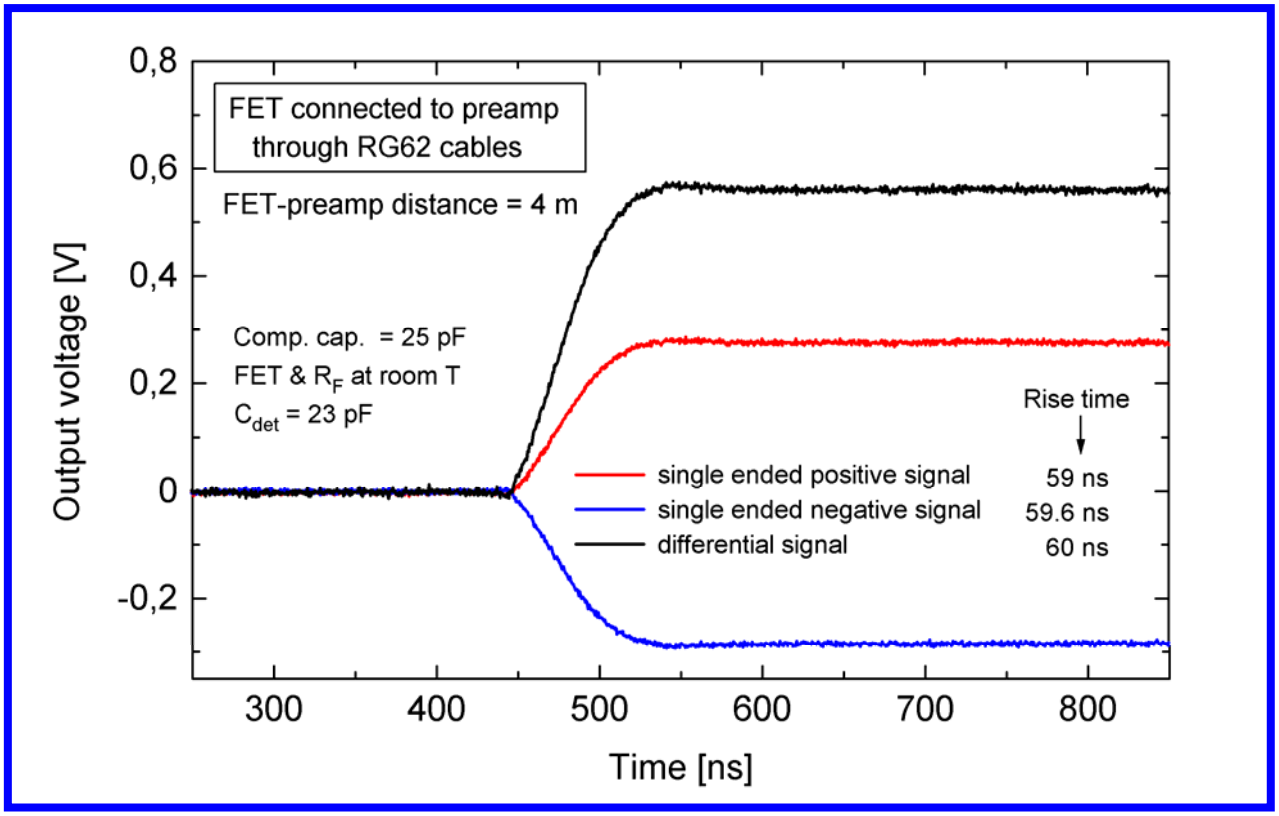
NO compensation capacitance

JFET-preamp distance: ~ 3m ➡ total length of the delay lines: ~ 6m



Comparison between the waveform observed at the circuit output and the mathematical model based only on the time delay introduced in the feedback loop

Stabilizing the output response by means of a compensating capacitance



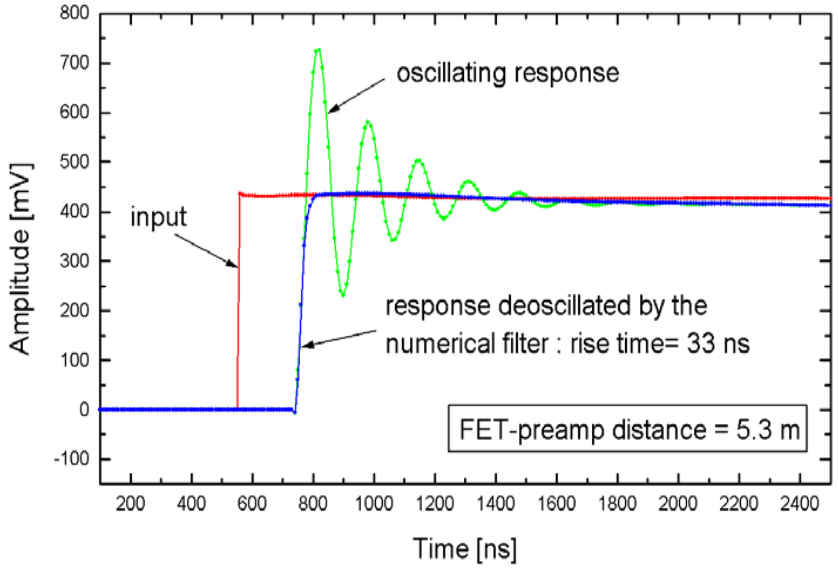
Single cable length (FET-preamp distance): ~ 4m

A compensation capacitance of 25pF allows to stabilize the output signals, but we have to accept a little overshoot (~1%).

The rise-time obtained is of ~ 60ns

If we want to COMPLETELY eliminate any overshoot, we have to reduce the bandwidth and accept a LONGER rise time.

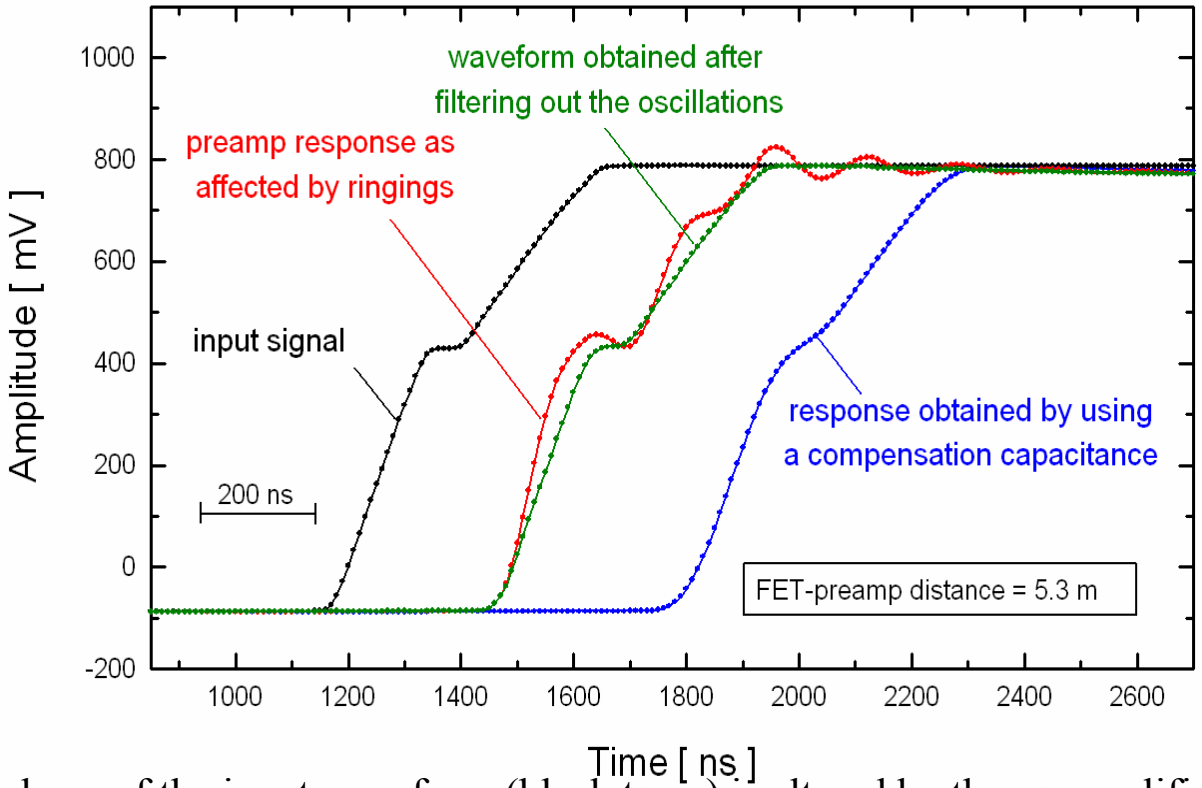
The technique of deoscillating filter



The response of the preamp at a step function, before and after applying the de-oscillator filter

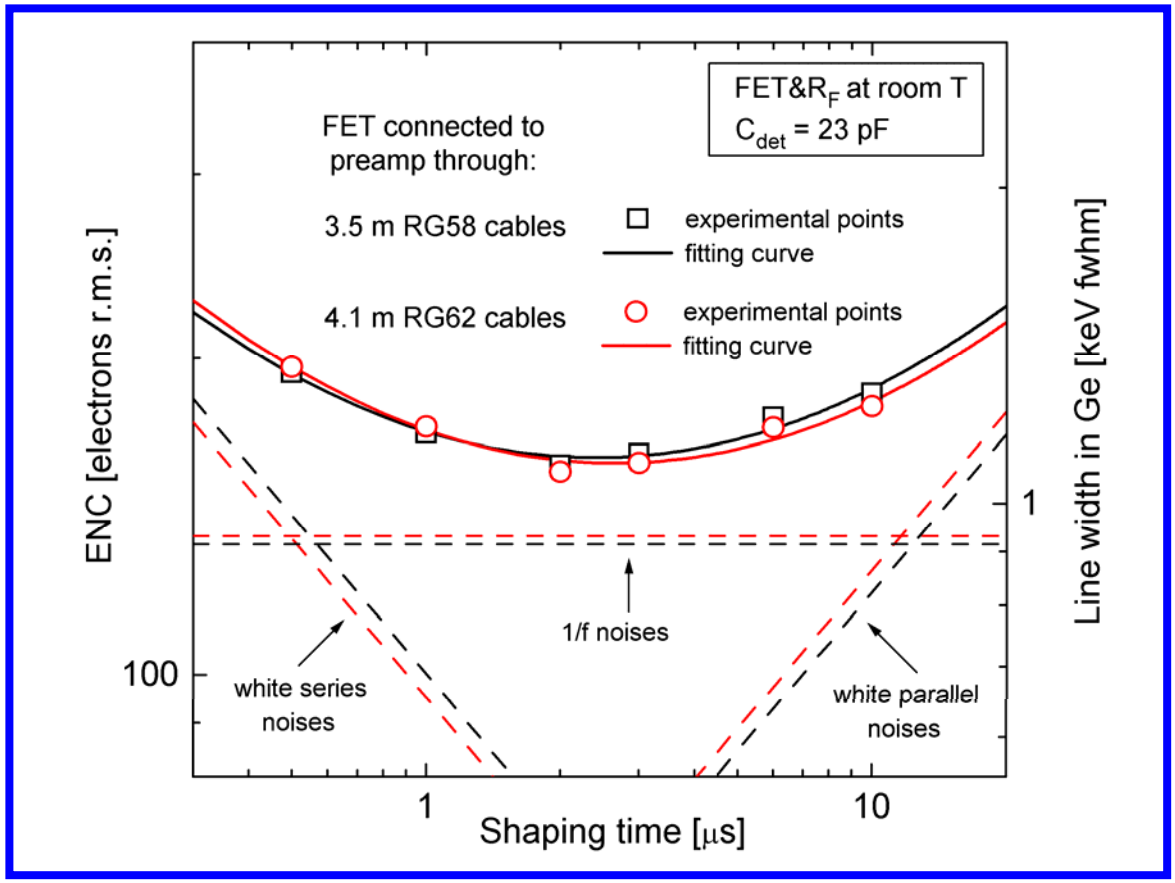
The de-oscillator function

The result of applying the de-oscillator filter when the input charge pulse is composed by two "structures" (double-hit event)



The shape of the input waveform (black trace) is altered by the preamplifier oscillations (red trace). The original waveform is reconstructed using the de-oscillator filter (green trace). As a comparison the response obtained with a highly compensated preamplifier is also shown (blue line), as delayed by 300 ns for the sake of clarity.

Noise measurements
(at the test bench, JFET at room temperature)



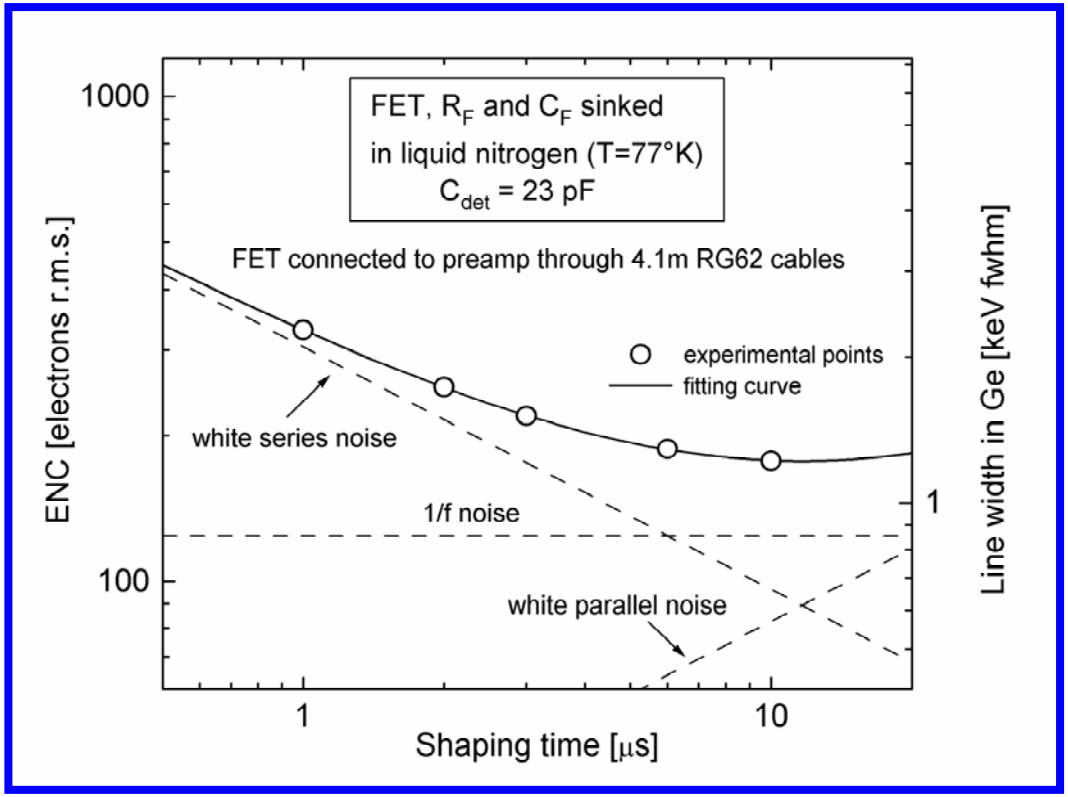
- FET at room temperature
- C_{det} = 23 pF
- semi-Gaussian shaper amplifier (Ortec mod.572)

Minimum at 2 μs shaping time:

156 electrons r.m.s. = 1.07 keV fwhm in HPGe

Noise turns out to be almost independent from the cable length or type

Noise measurements (at the test bench, JFET in LN)



- C_{det} = 23 pF
- semi-Gaussian shaper amplifier (Ortec mod.572)

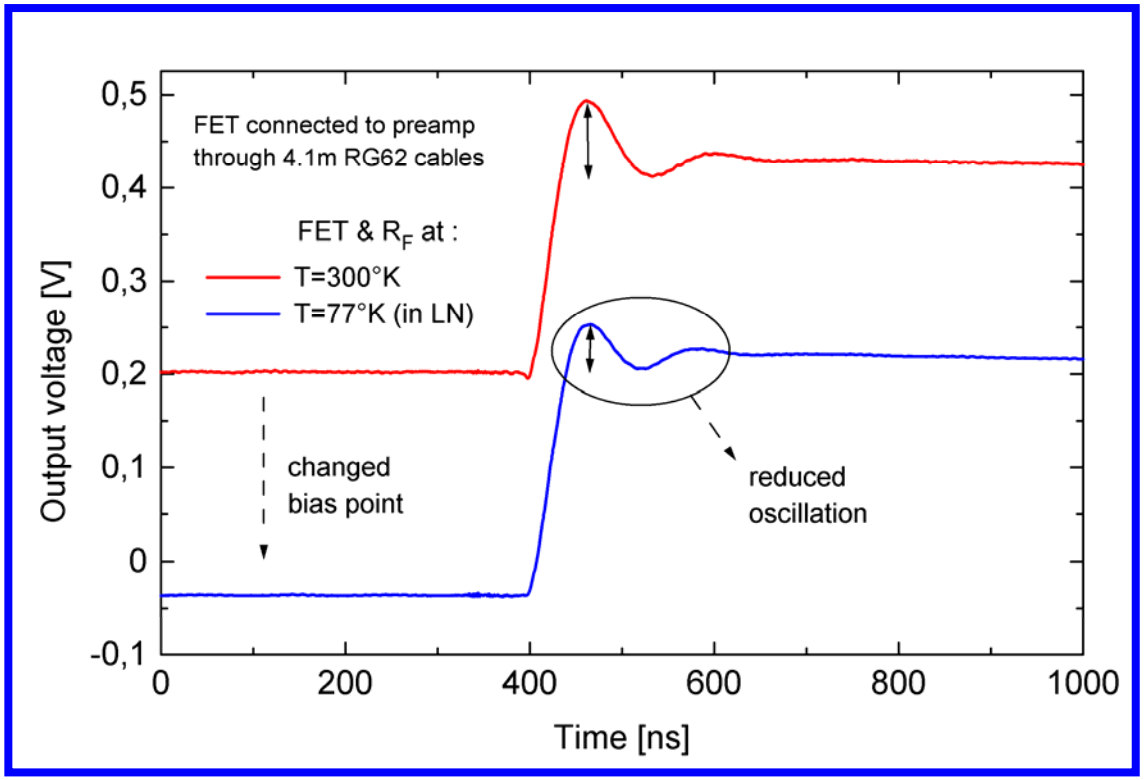
JFET in LN (T=77°K):
minimum at 10 μs shaping time
178 electrons r.m.s. = 1.2 keV fwhm in HPGe

Remember :

JFET at room T (300°K):
minimum at 2 μs shaping time
156 electrons r.m.s. = 1.07 keV fwhm in HPGe

The reduced transconductance g_m causes a worse electronic noise !

Bandwidth measurements



The reduced g_m causes a decrease in the charge loop gain and so a reduced bandwidth of the circuit

This decrease is not sufficient to eliminate oscillations but it only helps to partially stabilize the circuit, so that the needed compensation capacitance will have a lower value

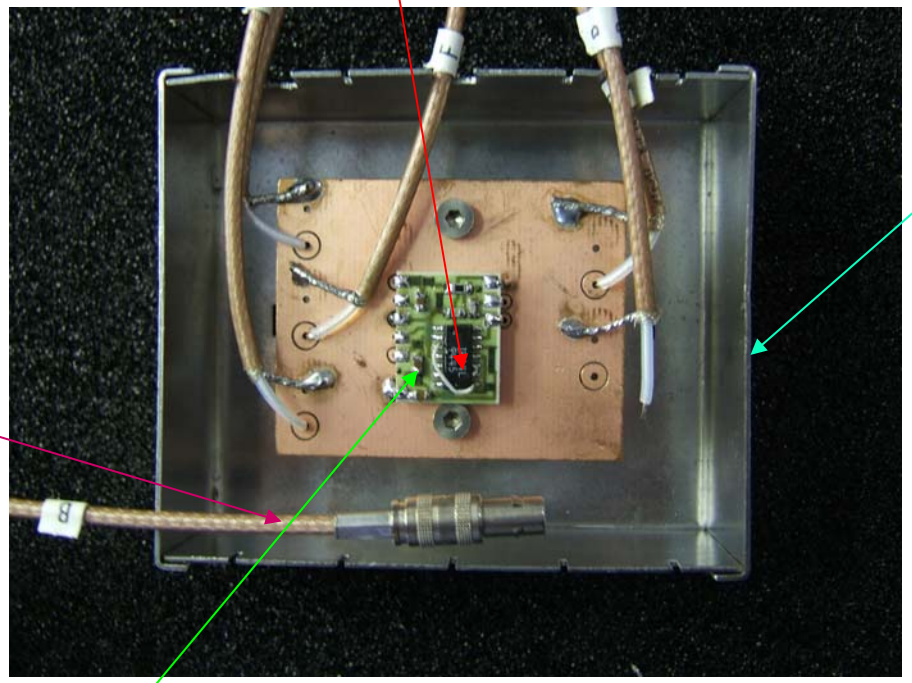
Rise time values obtained after complete compensation (with no oscillation or overshoot) are of the same order of those measured at room temperature

Conclusions on the use of AGATA preamps applied for GERDA

✓ The AGATA hybrids preamps have adequate performances for GERDA but can be placed only outside the LN bath or in a vacuum insulated box inside the LN bath. In the first case they have to be connected to the front-end JFET by 2 x 6 m long cables (93 Ohms or 50 Ohms have been tested) to close the feedback loop. The delays introduced in the feedback loop by the long cables induce oscillations in the output pulse. These oscillations can be managed either compensating the capacitance in the amplifier or applying a newly developped de-oscillating technique. With the latter a rise time of the order of 33 ns has been reached with a Cdet=23 pF.

The monolithic N-JFET preamplifier

Developed in the ’90s in a joint reasearch project between BNL, Italian MURST and INFN, for LAr, LKr calorimetry.



RG316 50 Ω cable

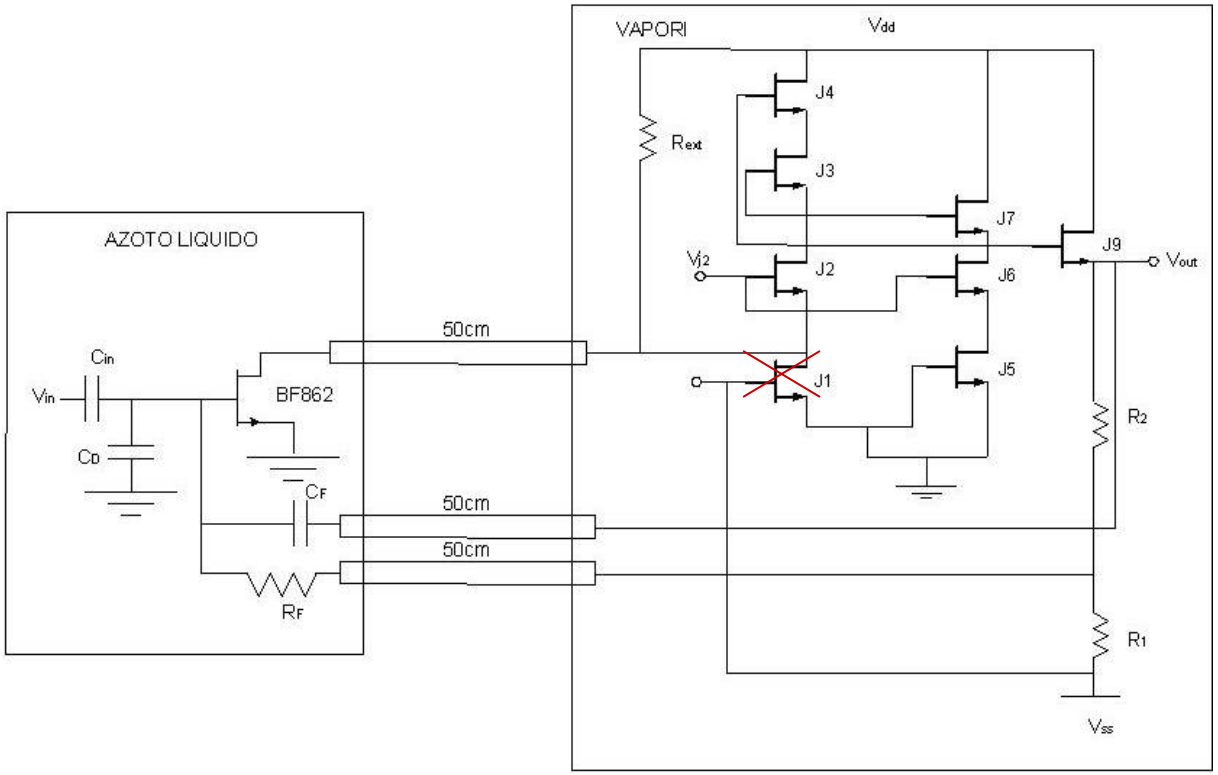
Shielding box

The IPA4 polarization circuit.
V. Re, co-author of the IPA4 circuit, provided us several IPA4 chip in SOIC plastic case + 1 polarization board, and several useful discussions.

The IPA4 N-JFET monolithic preamplifier

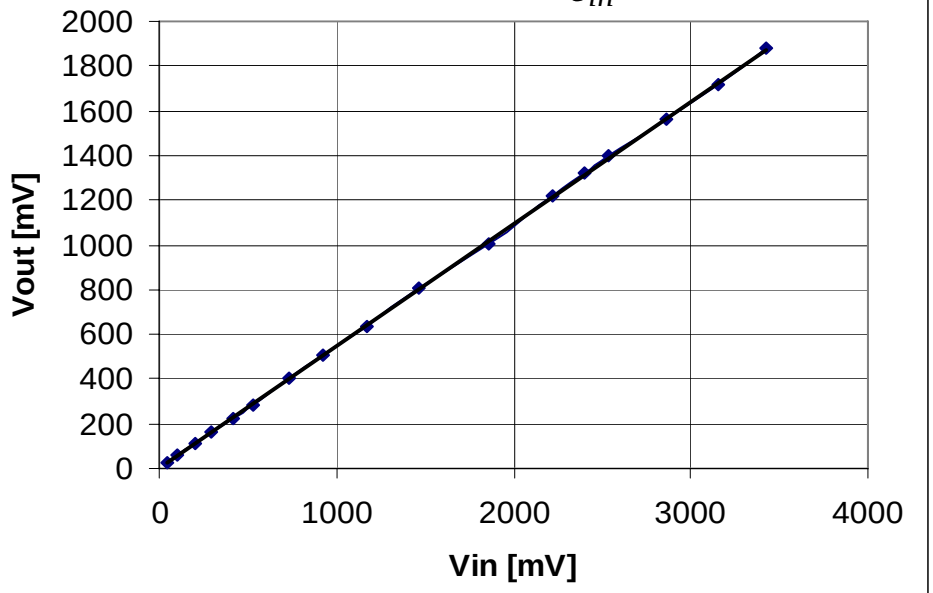
Sensitivity	~ 2 -2.5 V/pC with C_f= 0.5 pF → 120 mV/1 MeV in Ge
A(f)	75 dB – 60 dB (depending on the adopted configuration)
g_m J1	9.7 mA/V
W,L of J1	1820 μm, 15 μm
S_f of J1	1.52 nV/Hz$^{1/2}$
C_i	9 pF
τ_r	400 ns with C_f= 0.5 pF
Output	Single ended. Do not drive 50 Ω load.
Power consumption	~ 100 mW
Polarity	positive and Negative
V+,V-	+12 V, -6 V

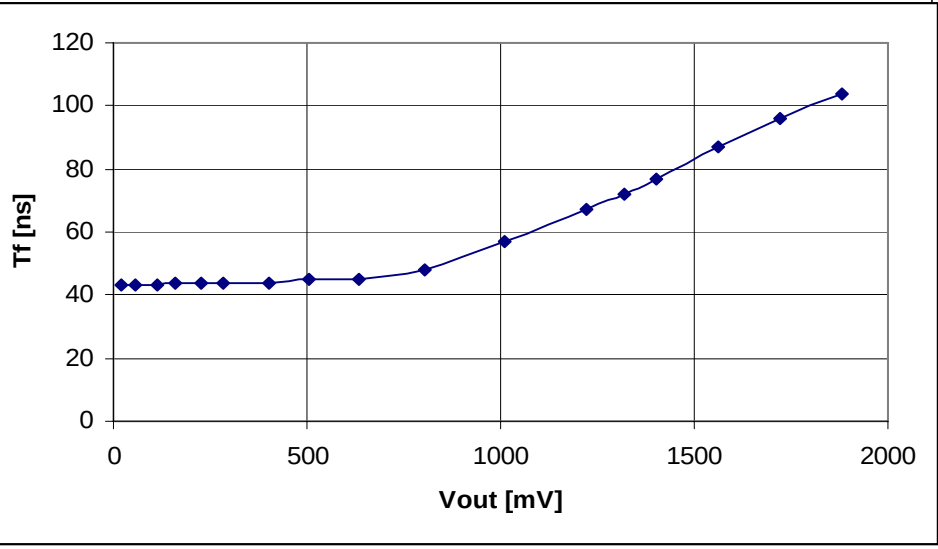
IPA4+external FET BF862

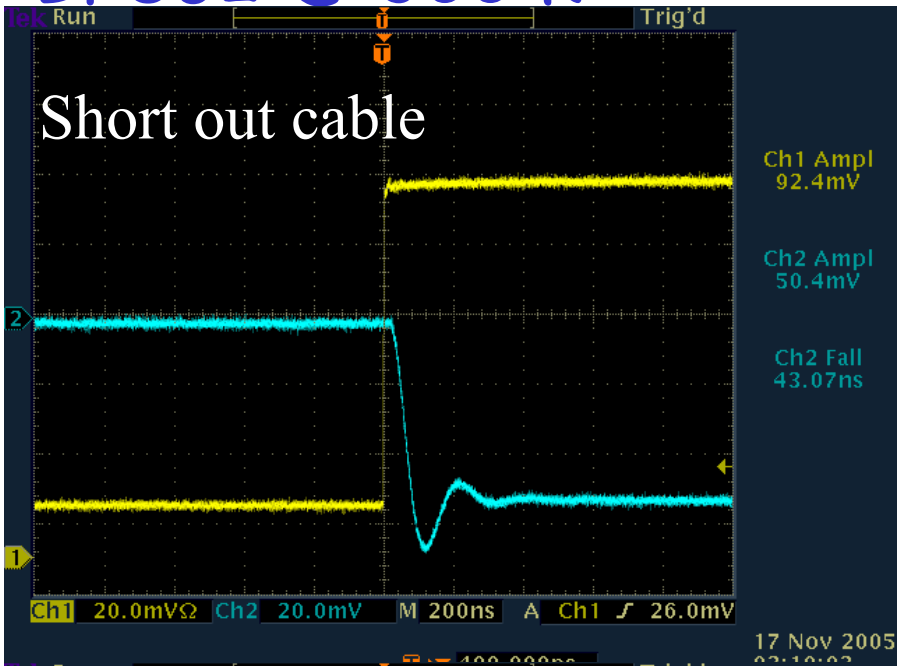


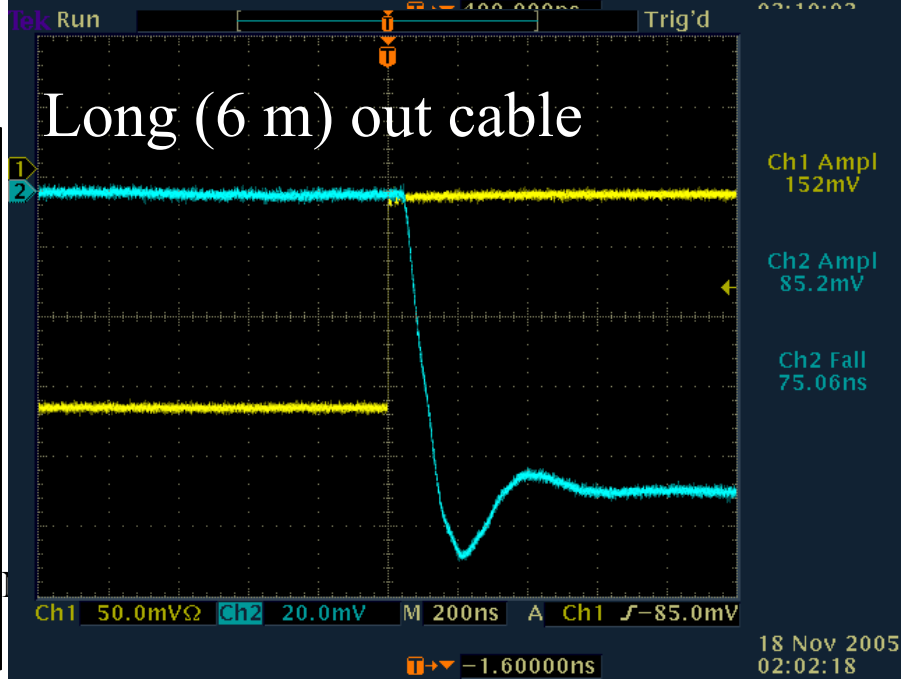
IPA4+external FET BF862 @ 300 K

Linearità $\frac{V_{out}}{Q_{in}} = 1{,}15V / pC$

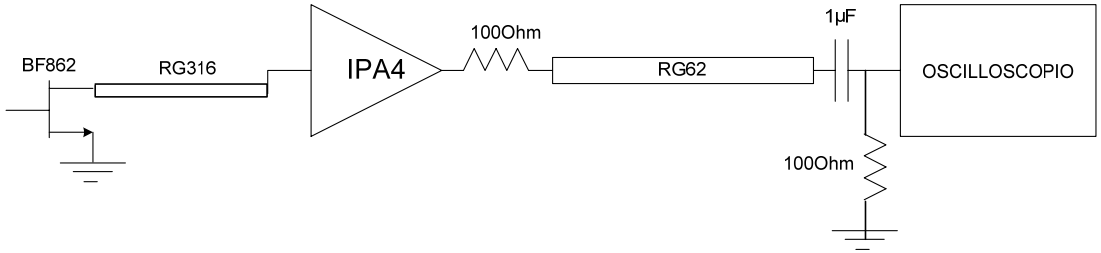


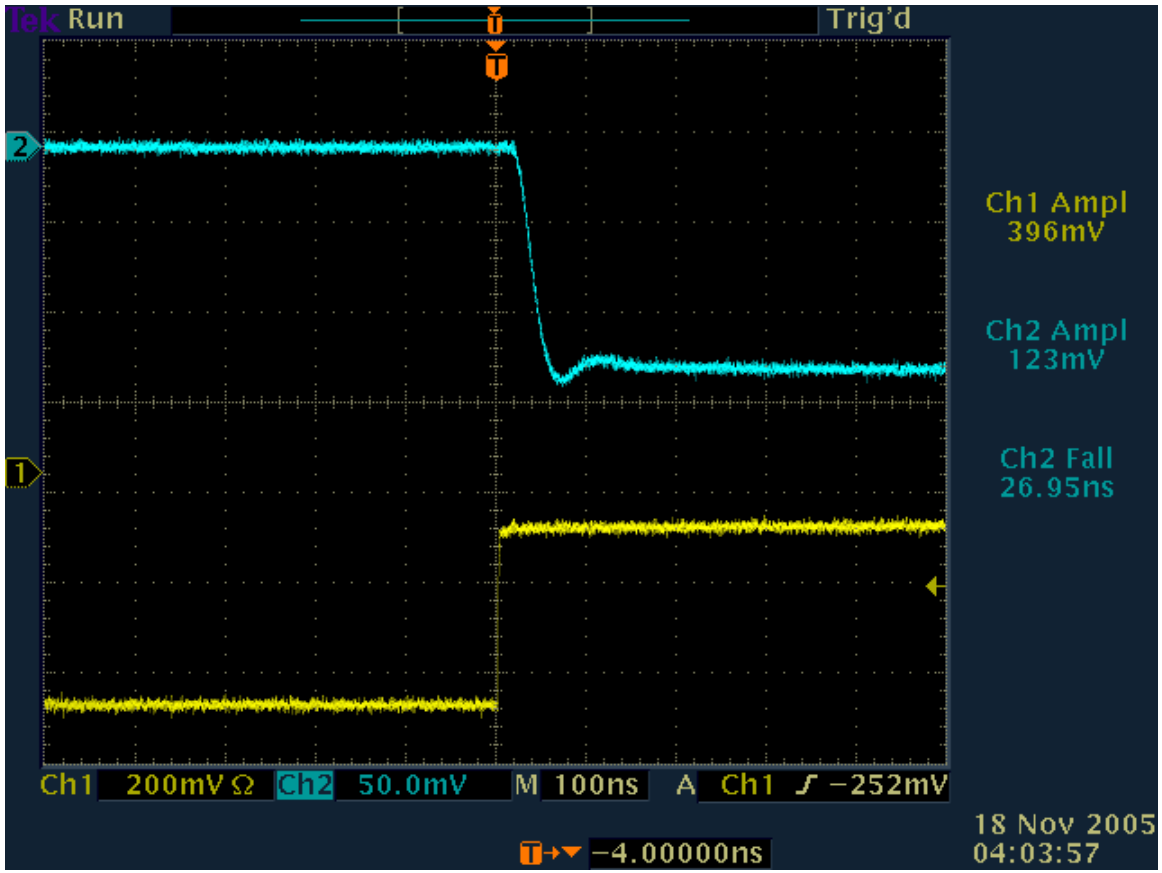






IPA4+external FET BF862 @ 300 K





Comparison of pulse fall time for IPA4 with internal and external FET.

CD [pF]	τf [ns] (BF862)	τf [ns] (J1)
0	27	110
15	36	140
27	44	155

$$\tau_f = C_T \frac{C}{C_F \times g_m}$$

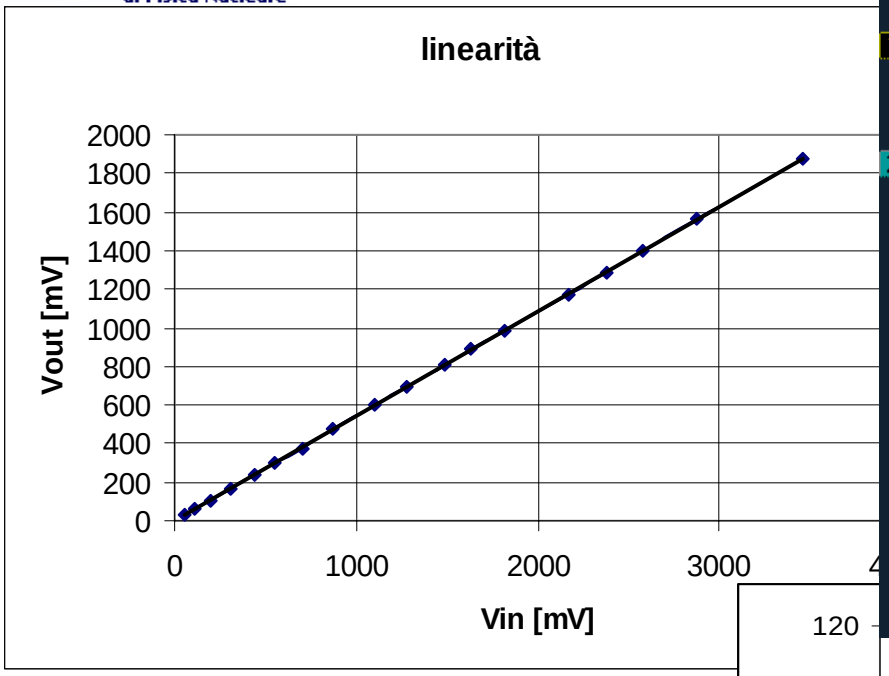
g_m J1 (I_{ds}~ 2.6 mA)= 9.7 mS

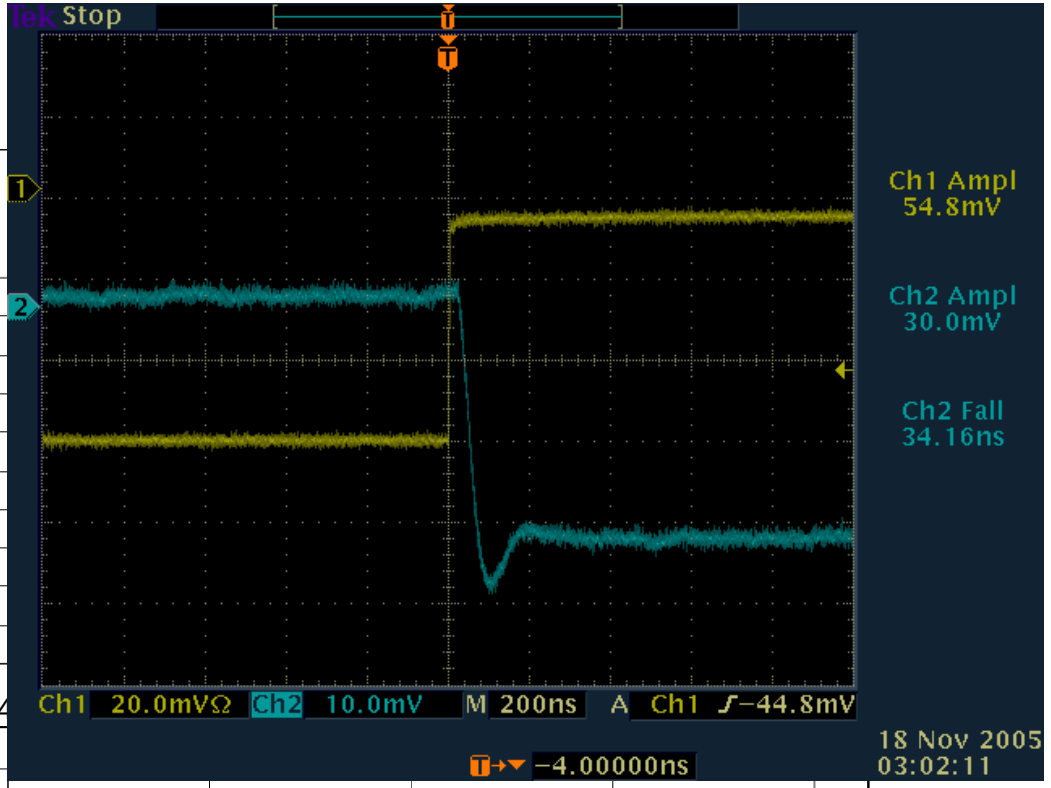
g_m BF862 (I_{ds}~ 3 mA)= 30 mS

$\frac{V_{out}}{Q_{in}} = 1{,}155V / pC$

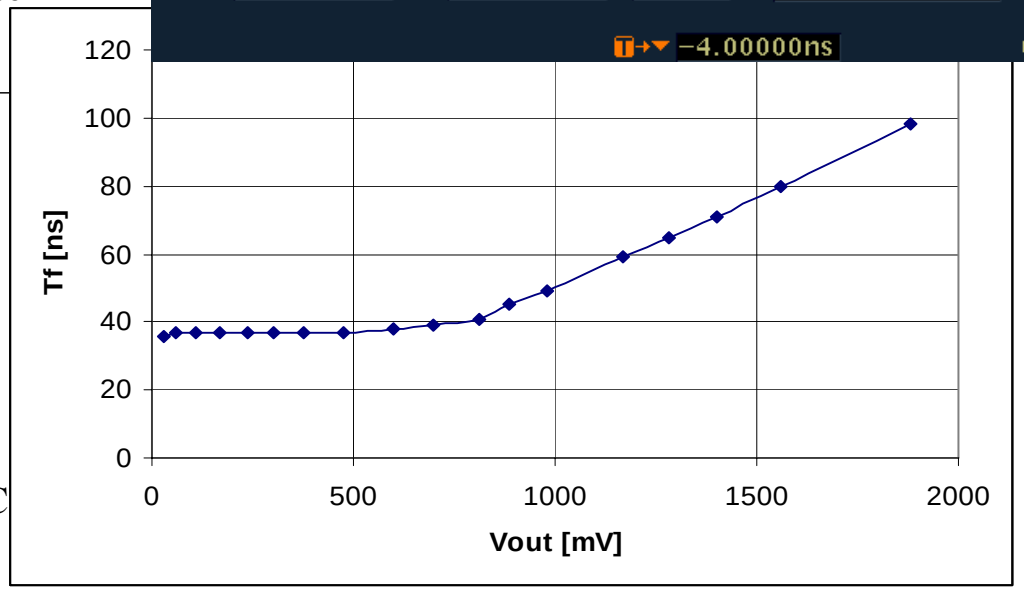
Istituto Nazionale di Fisica Nucleare

IPA4+BF862 @ LN

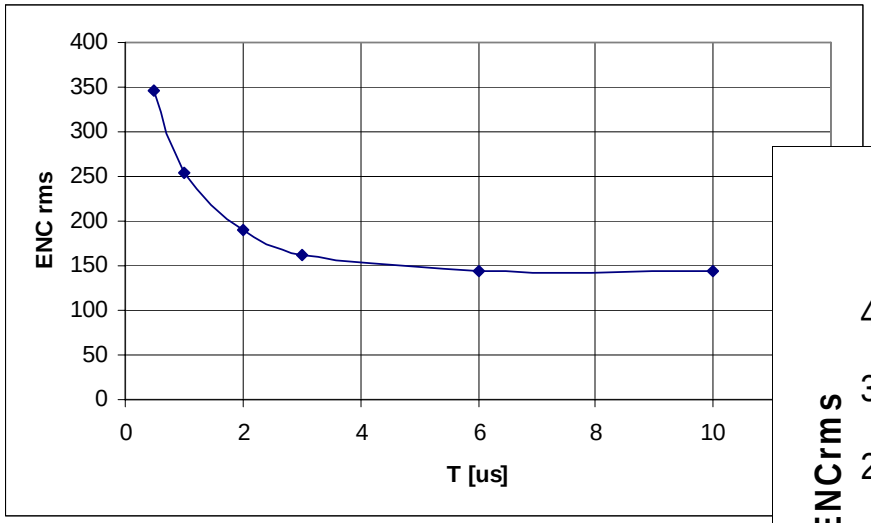




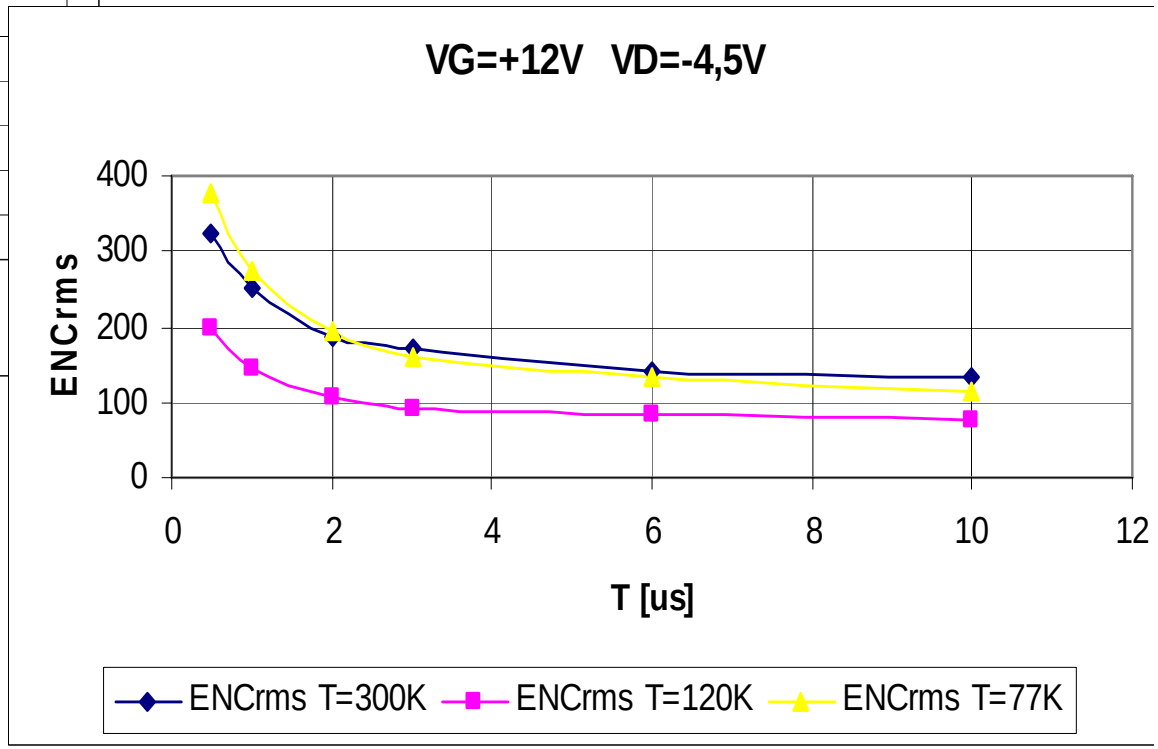
$\frac{V_{out}}{Q_{in}} = 1{,}155V / pC$



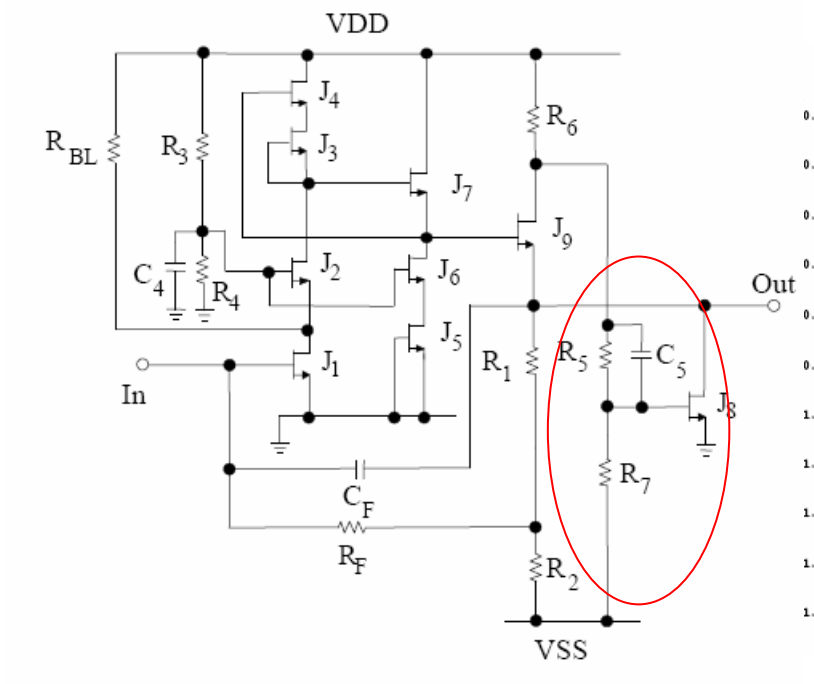
IPA4+BF862$_{ext}$ @ LN

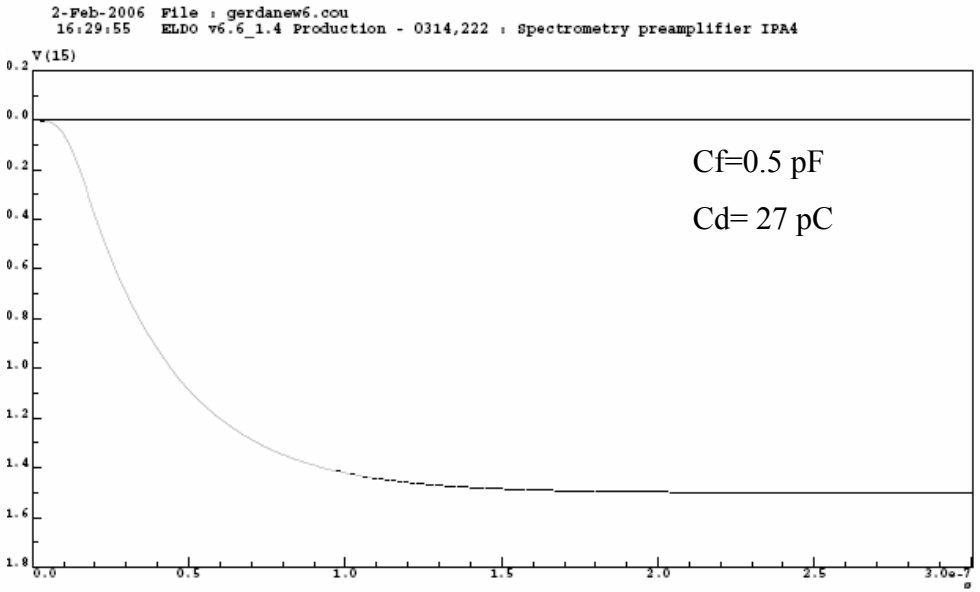


IPA4+J1$_{int}$



IPA4 + $J1_{ext}$ + 100 Out stage: simulated pulse 50 ns fall time (@ 300 K).

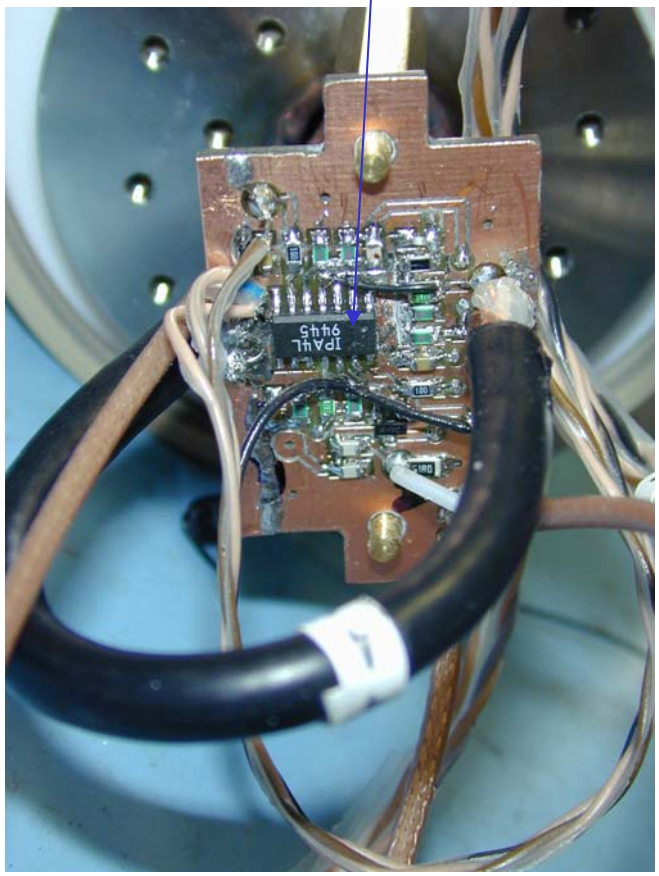




Swing to -1.5 V

IPA4 + $J1_{ext}$ + 100 Ω Out stage: the new test board

New setup for LN measurements



Production of IPA4 based FE for crystal prototipes (Phase I & II) read-out. Issues related to radiopurety

- CMOS preamps (Milano R&D) will be ready as front-end after summer 2006. CMOS from HD?
- Availability of enough IPA4 chips (2 wafer to be cutted + 20 chips in SOIC packages); use them to read-out crystal prototipes
- Ordered board production. Layout done. Need to define total number(~ 30)
- Components and radiopurety
  - Board substrate : Diclad 570 (PTFE/glass) 0.2 mm or Cuflon© (pure PTFE with copper evaporated under vacuum) 0.25 x 10^{-3} ", golded.
  - Resistors and Capacitors: 0804 and 0603 SMD components.
  - IPA4 in SOIC 14 pins packages. Also possible to mount as die (chip dim 44 x 33 x 8 mils).
  - Soldering compound: selected for CRESST

Total mass ~ 5 g. → Assuming a specific activity of the ensamble of 10 mBq/kg for ^{232}Th (obtainable without terrible effort) → Activity of each FE board (1 ch) ~ 5 μBq of ^{232}Th.

Pure PTFE Ultra Low Loss Microwave Substrates

Polyflon's CuFlon® Substrates

Polyflon has taken advantage of the qualities of PTFE and coupled them with a proprietary plating process to produce a microwave substrate whose performance cannot be equaled by any other substrate available at this time.

The pure PTFE material with a dielectric constant of 2.1, and a maximum peak dissipation factor of .00045 (at 1 to 3 GHz), is available in standard and custom dielectric thicknesses, (.00025" to .005" and .010" to .125"), with double sided copper, in a standard range of copper plated claddings which includes 1/3 oz.(0.5 mil), 1/2 oz.(0.7 mil), 1 oz.(1.4 mil), and 2 oz.(2.8 mil). More or less copper can be applied in the plating process to meet the specific requirements.

Comparison of CuFlon and PTFE Glass Laminates

Parameter	PTFE	PTFE/GLASS
Dielectric Constant	2.10	2.17
Dissipation Factor (10 GHz)	.00045	.0013
Peel Strength	8 lbs/in.	8 lbs/in.
Water Absorption	0.01%	.035%

Unique Characteristics of PTFE

Electrical and Physical Properties

PTFE has unique electrical and physical properties: low loss tangent and dissipation factor, low dielectric constant, very high volume and surface resistivity, high temperature resistance, chemical inertness, and almost zero water absorption. PTFE has been used as insulation in many RF(low to microwave frequencies) applications, including commercial, government, and military. It is the only material currently available where all these desired and diversified characteristics come together.

Mechanical Properties

PTFE is a semi-rigid material, and due to this characteristic it has two minor drawbacks, namely; cold flow extrusion and a higher coefficient of thermal expansion ratio than rigid materials. Some substrate manufacturers have added various elements to the PTFE to make it more rigid. This has reduced these problems slightly, but has, in turn, created more serious problems, such as raising the loss tangent and creating non-uniformity of the dielectric constant in the substrate. Additionally, the dielectric constant is not consistent over temperature and frequency variations.

Cuflon good candidate for CMOS ASIC FE

Cabling (for HV and FE)

Available measurements performed on coax cables and components

	^{228}Ra mBq/kg	^{228}Th mBq/kg	^{226}Ra mBq/kg	^{40}K mBq/kg	^{60}Co mBq/kg	^{137}Cs mBq/kg
Kapton coax 3.5 g/m (HV candidate)	< 15	< 11	< 12	< 100	< 5	< 4
Kapton flat (Cuore)						
Teflon coax (RG316 16 g /m or RG178 8 g/m)						
SMD resistors (COBRA)	270 810	180 580	270 620	1300 <500		

Cabling from FE to FADC depends on FE

- Single-ended / twisted
- Controlled impedance at LN
- Radiopurity
- Teflon and kapton coax worth to be investigated deeper

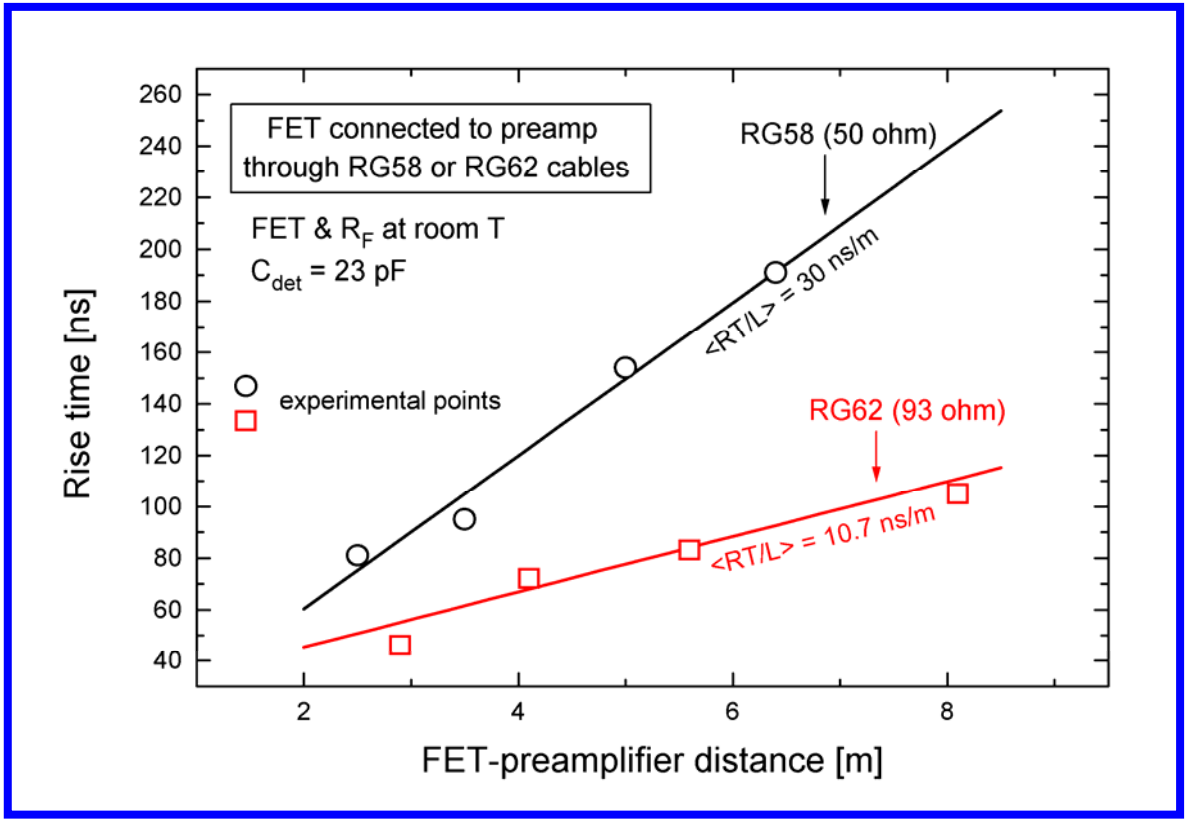
Question

- Where and when perform a full program of γ spectrometry and/or ICPMS measurements dedicated to FE and cabling?

ASIC CMOS fully integrated circuit at Hd

Comparison of RG62 with RG58 cables to connect JFEt to the amplifier

Rise time values vs. different FET-preamp distances in complete absence of any overshoot



Better performance of RG62 (93 ohm) cables !

The main cause is the difference in the time delay they introduced in the signal transmission:

RG62: ≈ 4 ns/m

RG58: ≈ 5 ns/m

Conclusions on the use of AGATA preamps applied for GERDA

- ✓ The noise of the preamplifier is 156 e- (rms) when the FET is at room temperature and 178 e- (rms) at LN temperature. This correspond respectively to 1.05 keV and 1.2 kEV FWHM in Germanium
- ✓ In liquid nitrogen the JFET transconductance decreases: this fact helps to stabilize the circuit against the oscillations due to the delay lines in the charge loop BUT causes an increase in the electronic noise. The performance would improve by warming the JFET a little bit.

The circuital layout of the I(ntegrated)P(re)A(mplifier)4 N-JFETmonolithic preamplifier: input device J1 is dimensioned to match detectors of 10 <Cd<100 pF

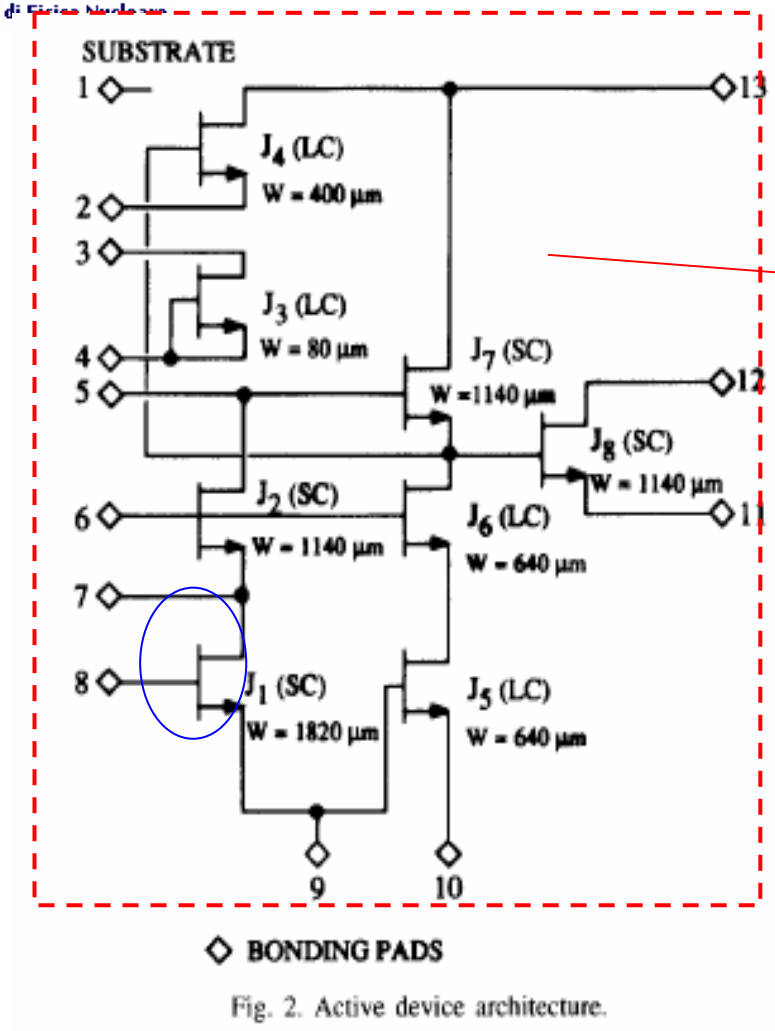
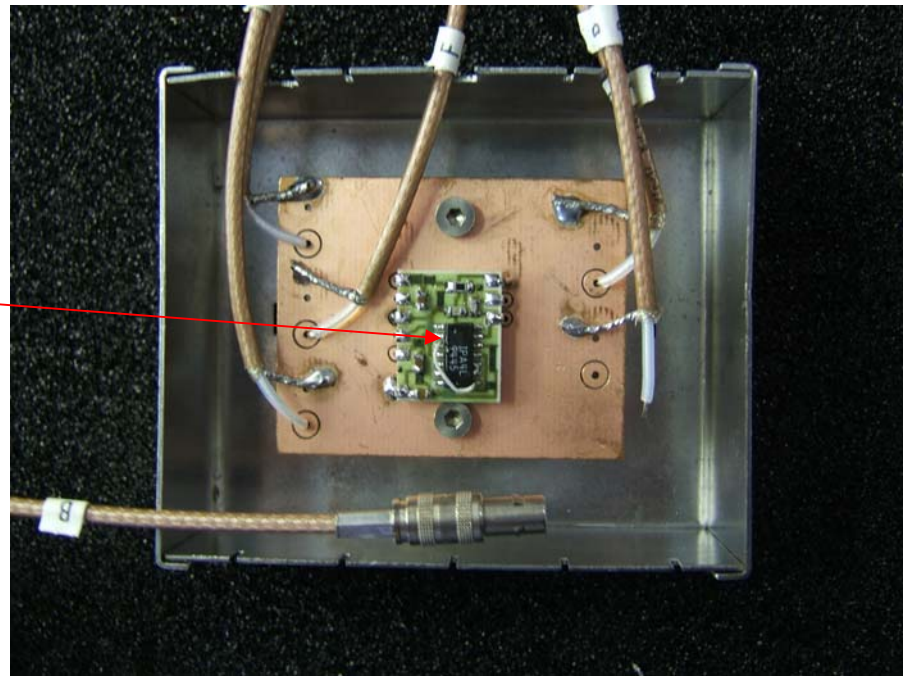


Fig. 2. Active device architecture.



The preamps is integrated, all JFET realized with the buried-layer technology (very good noise performances in principle better than than CMOS but slow devices technology. Developped for LAr and LKr applications).

The IPA4 hybrid ciurcuit with C_fR_f and polarization components

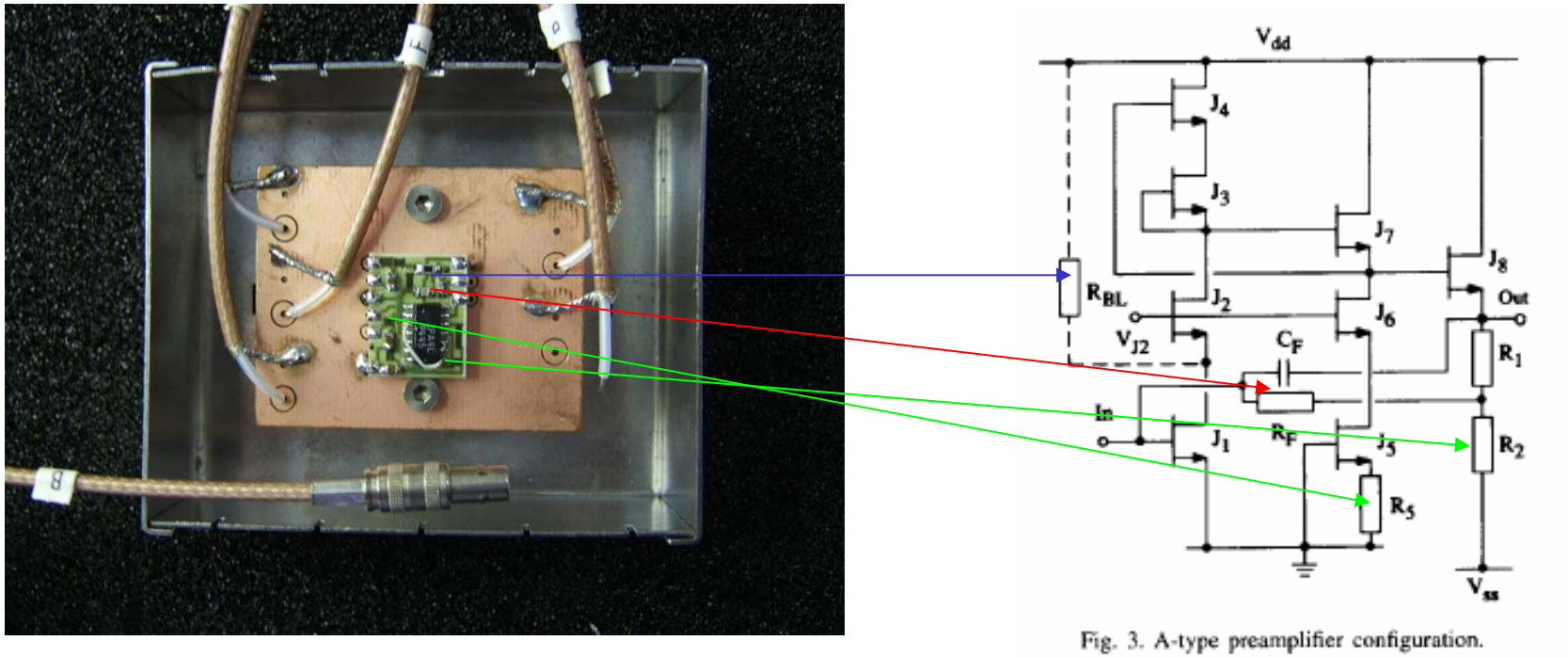


Fig. 3. A-type preamplifier configuration.

All polarization components are out of the preamp, to allow several preamp configurations, to fit the application.

Published noise figure of IPA4 preamp.
Never measured at LN or LAr.

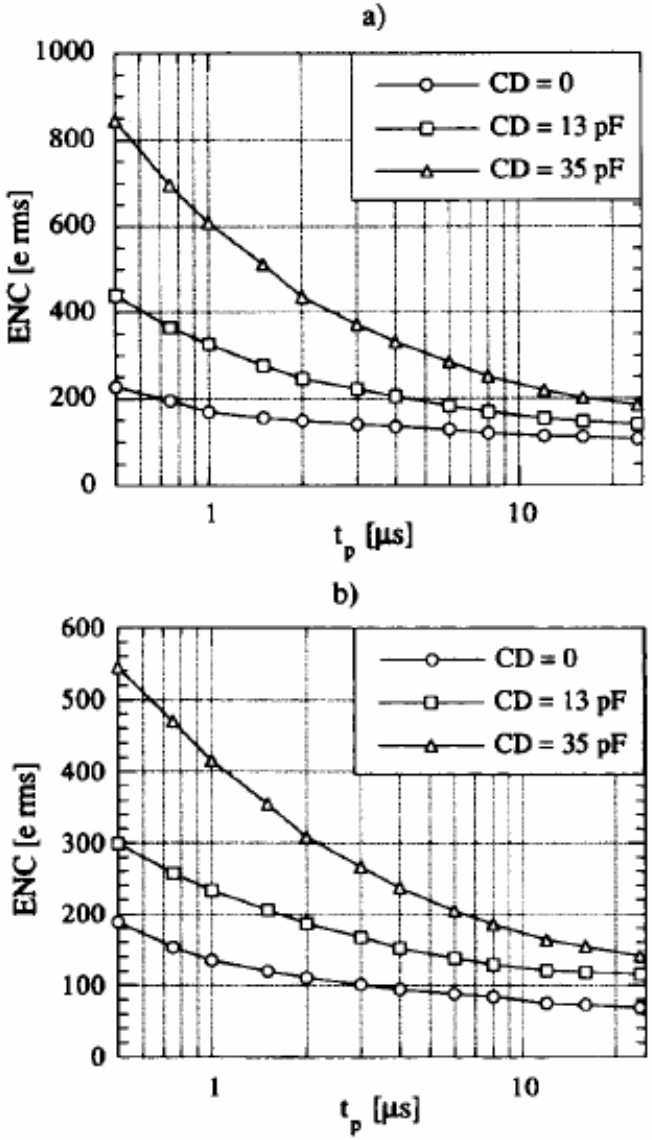


Fig. 7. ENC as a function of the peaking time t_p for the A-type preamplifier followed by a semigaussian unipolar shaper: (a) The standing current in J_1 is 0.6 mA; (b) The standing current in J_1 is 5 mA.

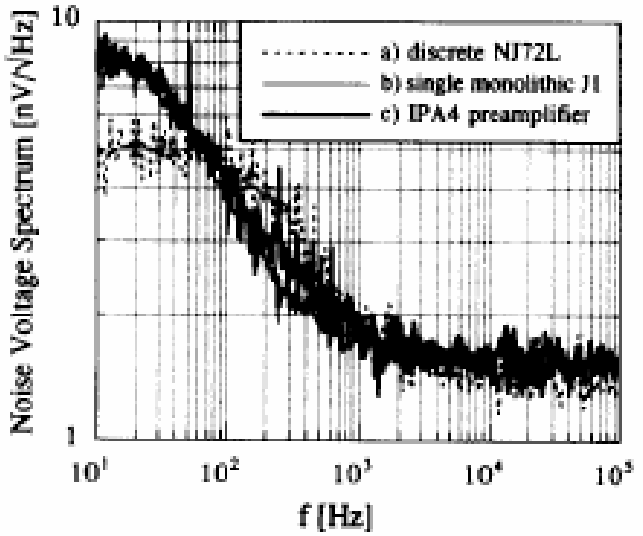


Fig. 6. Input-referred spectral densities of voltage noise as a function of frequency: (a) Discrete device with the same geometry as J_1; (b) J_1; (c) Complete preamplifier.

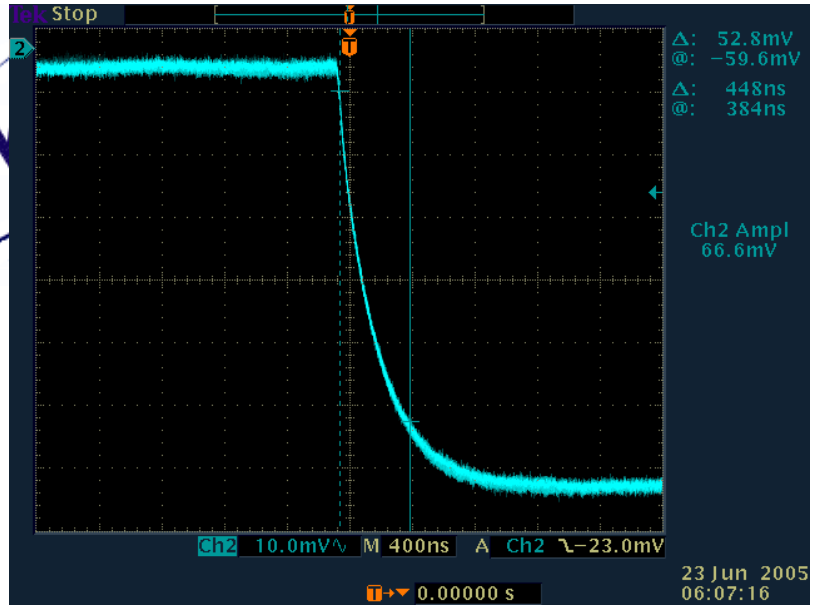
Purpose of our tests on IPA4:

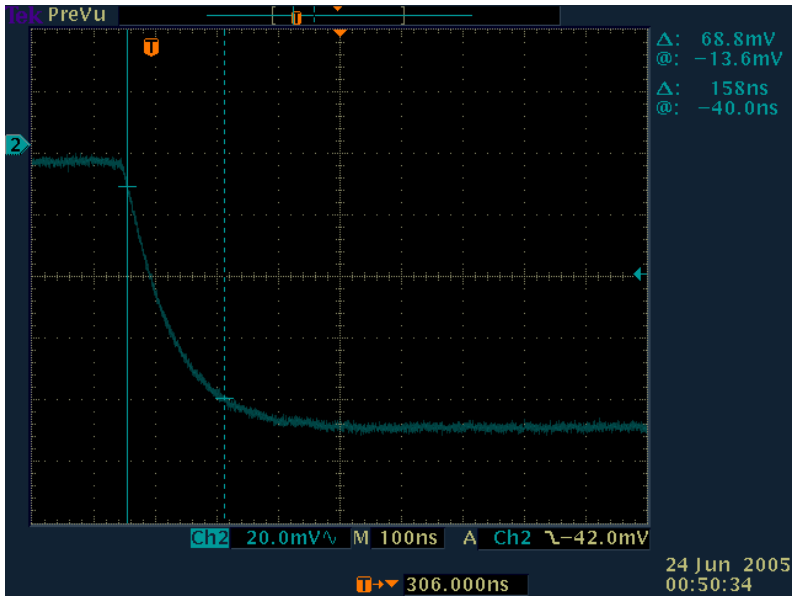
- reproduce the nominal behavior

- measure the pulse rise time, poorly described in the reference paper and in the thesis.

- test several possible operational configuration, varying the relevant operational parameters (I_{DS} in J1, the active load of the high impedance node, the polarization V_{DC}, etc.) to improve the pulse RT.

- Characterize the device at LN temperature (noise, and RT).
- Test the possibility to drive a long cable.





Test of IPA4 on the its ibrid board

(thick film circuits + SMD capacitors and resistors)

	C_f = 0.5 pF C_D = 27 pf R_{BL} = 4.7 kW	
T / V_{DC}	300 K	> 77 K
+12, -6	450 ns	320 ns
+18, -6		160 ns

Increasing V_+ and cooling the RT significantly improves.

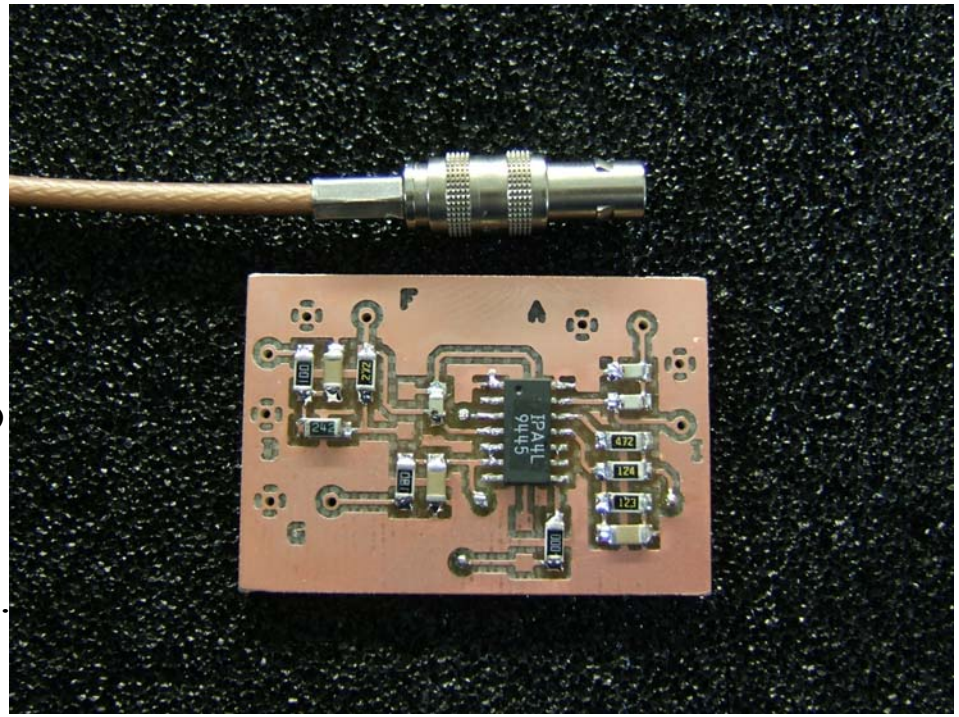
$T_r = C_t\ (C/g_m\ C_f)$

Measured sensitivitv: 2.6 V/pC

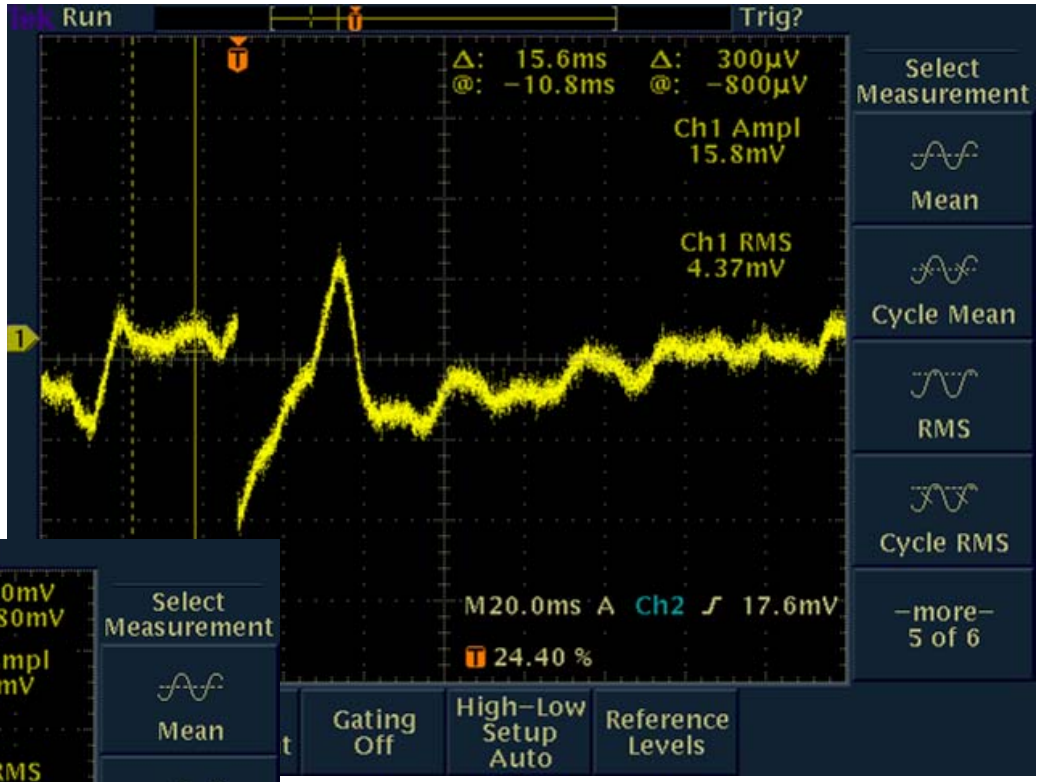
The integrated circuits permanently damages after few cycles at LN

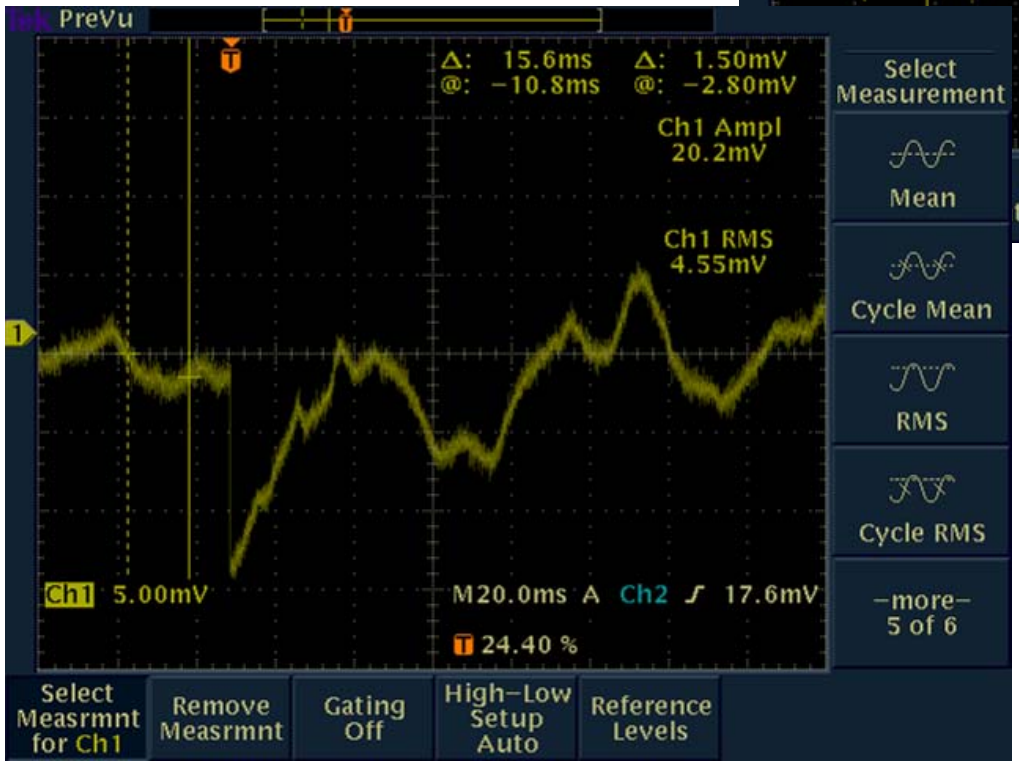
Test of IPA4 mounted on a newly build PCB board

- To vary safely the relevant components to vary IDSS, Cf, Cd etc, and because the thermal cycles damaged the ibrid board, we built in our lab a printed board. Performed the following tests:
- Vary R_{BL} 4,7 kΩ, 2,7 kΩ, 1,8 kΩ to increase the IDS→ No significant variation of RT.
- Substitute J3 with resistor (2.5 kΩ, 1.6 kΩ) to reduce the active load. → No significant variation of RT.
- Change C_F→as expected significant variation.



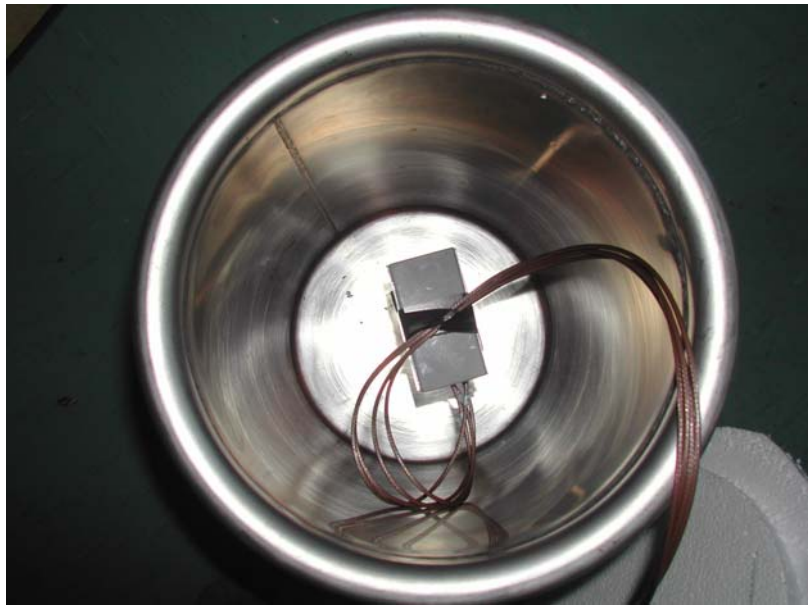
REMARK: All our measurements preformed with Teflon RG316 cables



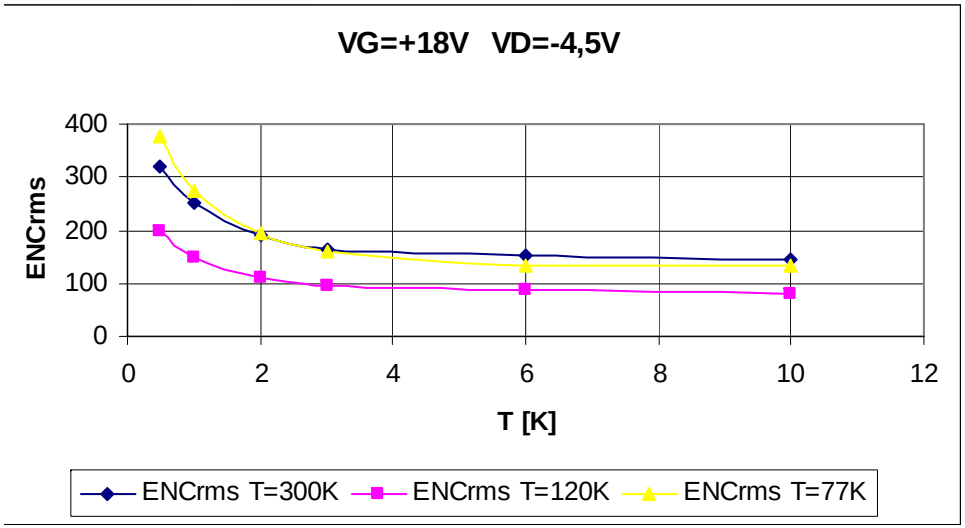


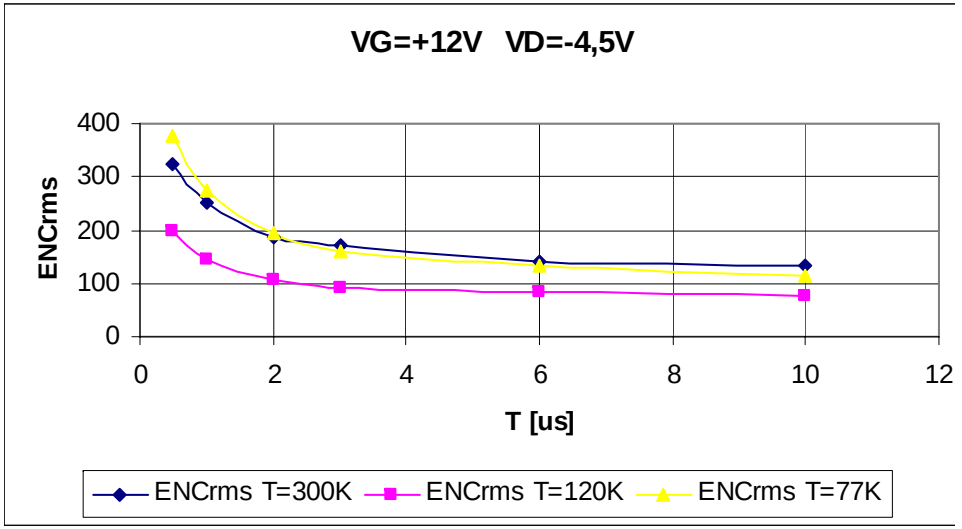
Effect of boil off bubbles when the preamp is directly immersed in the LN. It has to be put in a cage and cooled down through a cold finger.

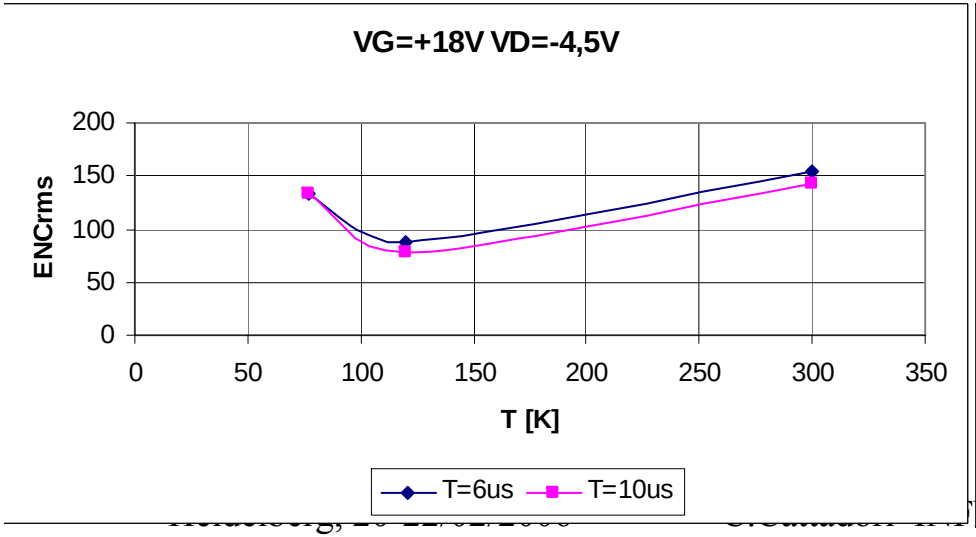
The IPA4 LN test setup: preamp in a box in close contact with a cold- finger.

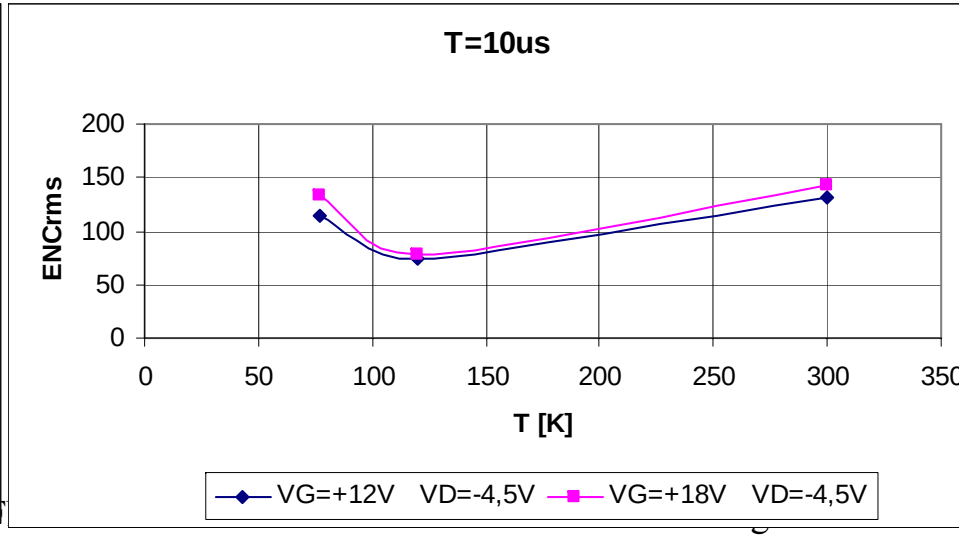


IPA4 measured noise figures in the GERDA setup at relevant temperatures









Comparison of tests at T=77 K and T=300 K
Cf = 1.0 pF, Cd= 27 pF

	IPA4 on printed circuit. T=77 K	IPA4 on printed circuit. T=300 K	removed back Cu layer
V_+= 12 V	175 ns	150 ns	125 ns
V_+= 15 V	155 ns	110 ns	105 ns
V_+= 18 V	120 ns	100 ns	93 ns

Conclusion: our double Cu layer printed board presumably introduce a parasitic Cf, as it is faster but gain is reduced. Again, increasing V+, significantly improve the RT.

Noise measurements at T=300 K

V+= 12 V,Cf=1.0 pF, Rf=10 GΩ,Cd=27 pF

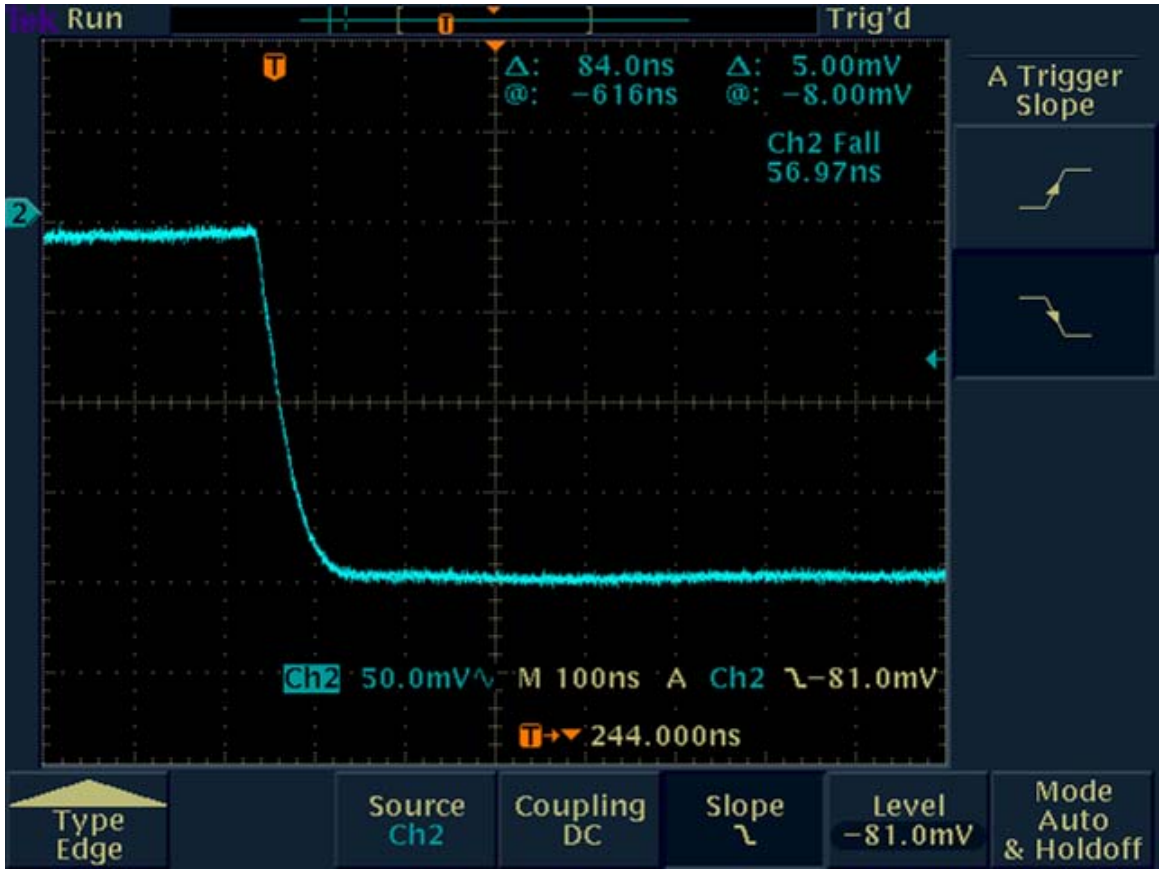
T=300 K

τ [μs]	ENC_{rms} [e^-]
0.5	300
1.0	225
2.0	185
3.0	138
6.0	115
10.0	107

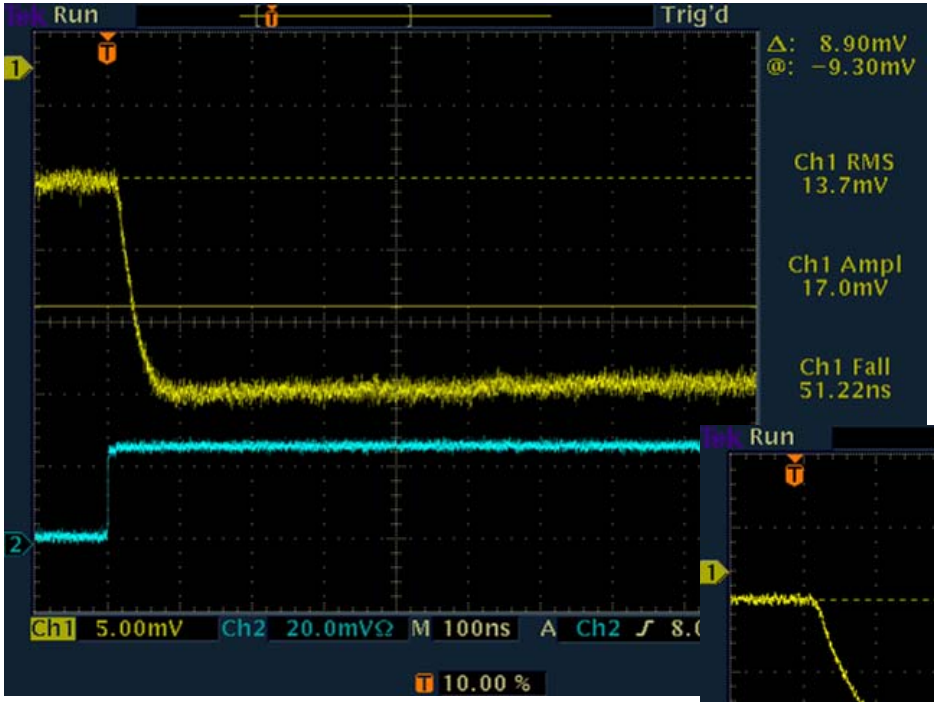
T=77 K preliminar

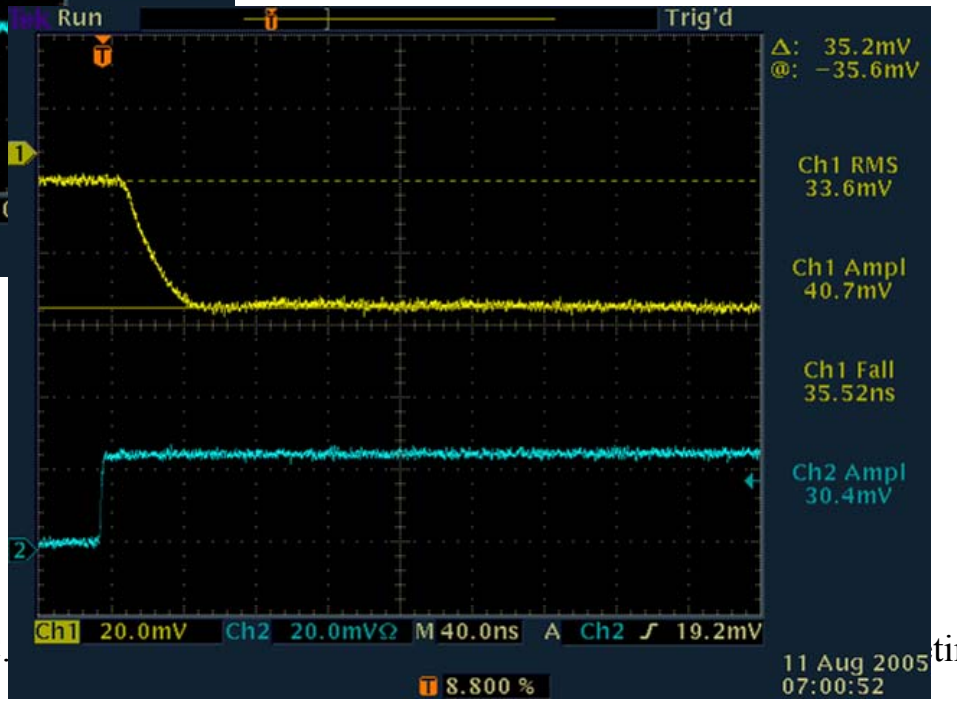
τ [μs]	ENC_{rms} [e^-]
0.5	293
1.0	230
2.0	211
3.0	206
6.0	196
10.0	135

At LN difficult to perform measurements due to microfony caused by bubbles on chip and board. Then built a rudimental cold finger, but

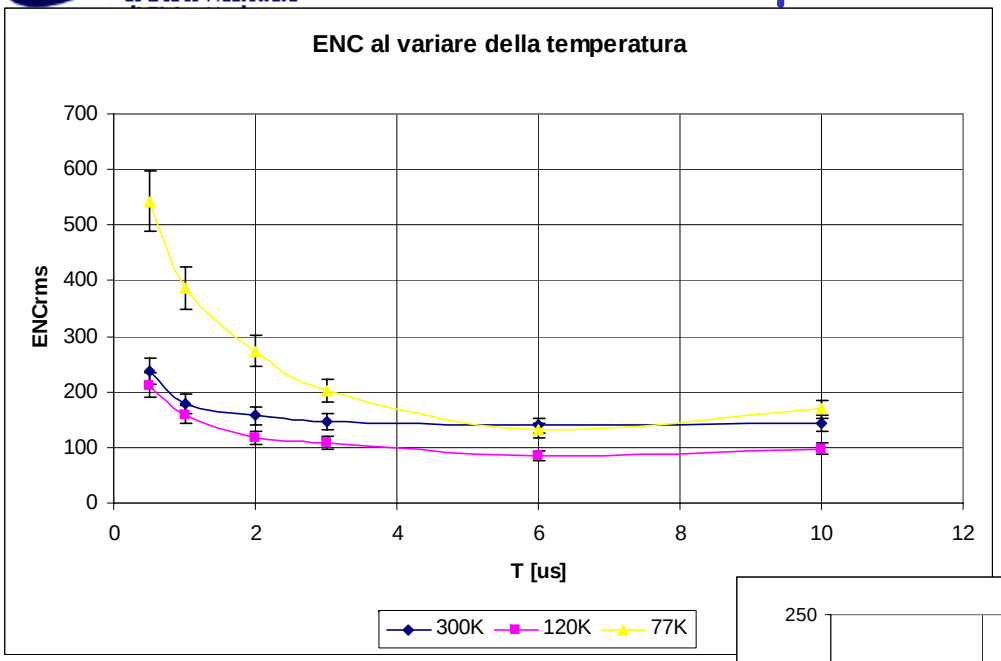

Run
Trig'd
Δ: 84.0ns Δ: 5.00mV
@: −616ns @: −8.00mV
Ch2 Fall
56.97ns
A Trigger
Slope
Ch2 50.0mV
M 100ns A Ch2 −81.0mV
244.000ns
Type
Edge
Source
Ch2
Coupling
DC
Slope
Level
−81.0mV
Mode
Auto
& Holdoff

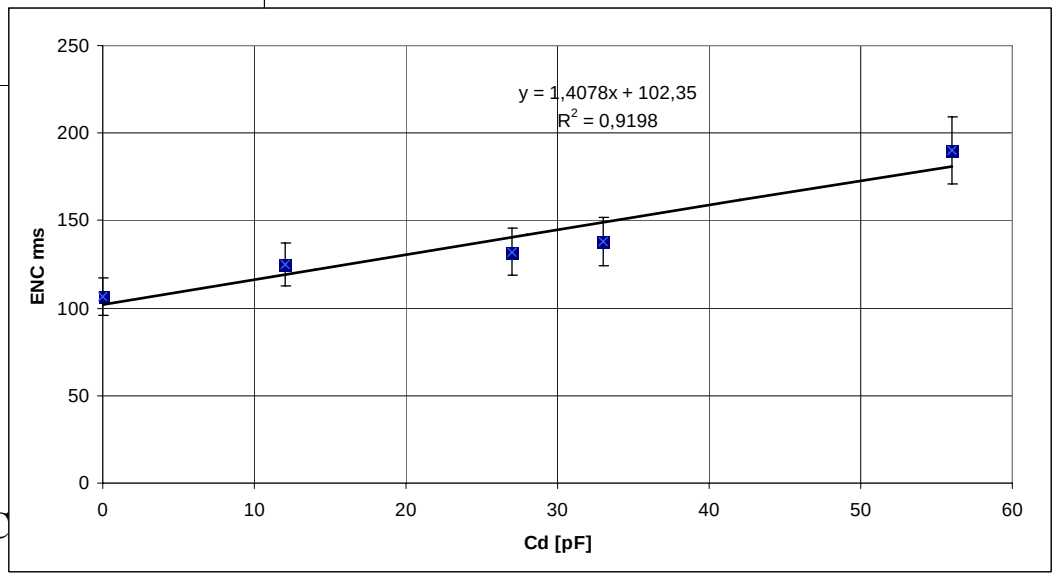
Test of Amptek 250 preamplifier





Test of Amptek 250 preamplifier





Conclusions

• Work is ongoing to look for the preamps suitable to work in our experimental conditions and a couple of solution are pursued.

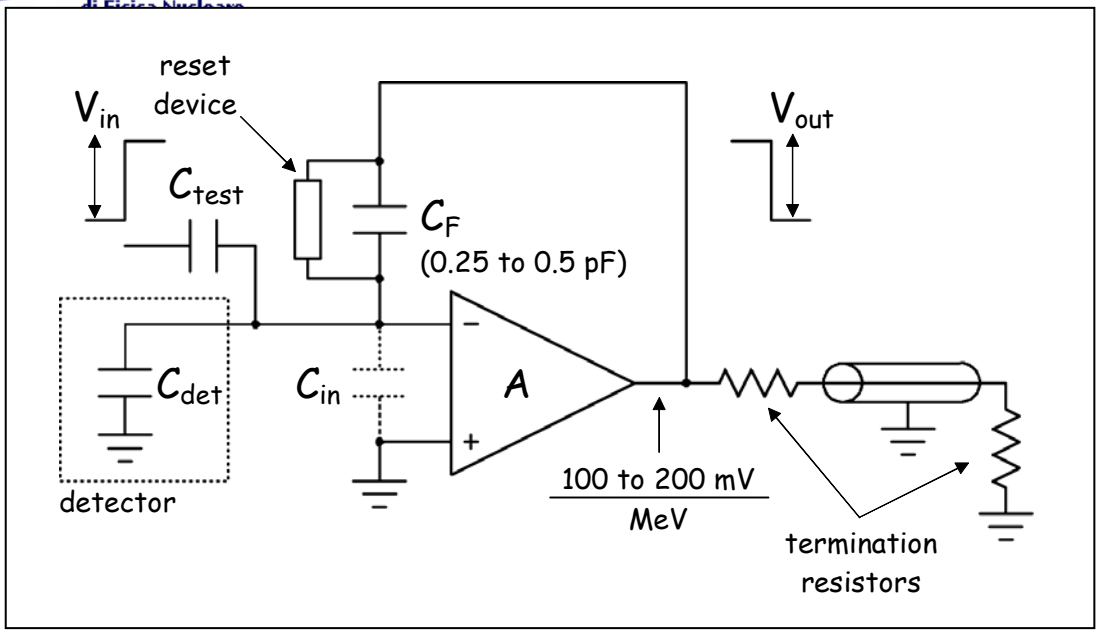
• Open issue:

choice of mounting (preamp nearby cristal or in junction box), cables, gamma ray -measurements of feedback components, and of IPA4 preamplifiers in the die configuration, long term stability measurements, etc….

CMOS ASIC circuit R&D program

- Milano: AMS 0.8 μm, 5 V technology
- Hd: AMS 0.6 μm technology

Loop gain



stable part of the gain

"static error"

$$\frac{V_{out}}{V_{in}} = \frac{C_{test}}{C_F} - \varepsilon \qquad \varepsilon = \frac{1}{G_{loop}}$$

G_{loop} > 1000 for gamma-spectroscopy performance

$$G_{loop} = A \times \frac{C_F}{C_{in} + C_{det} + C_{test} + C_F}$$

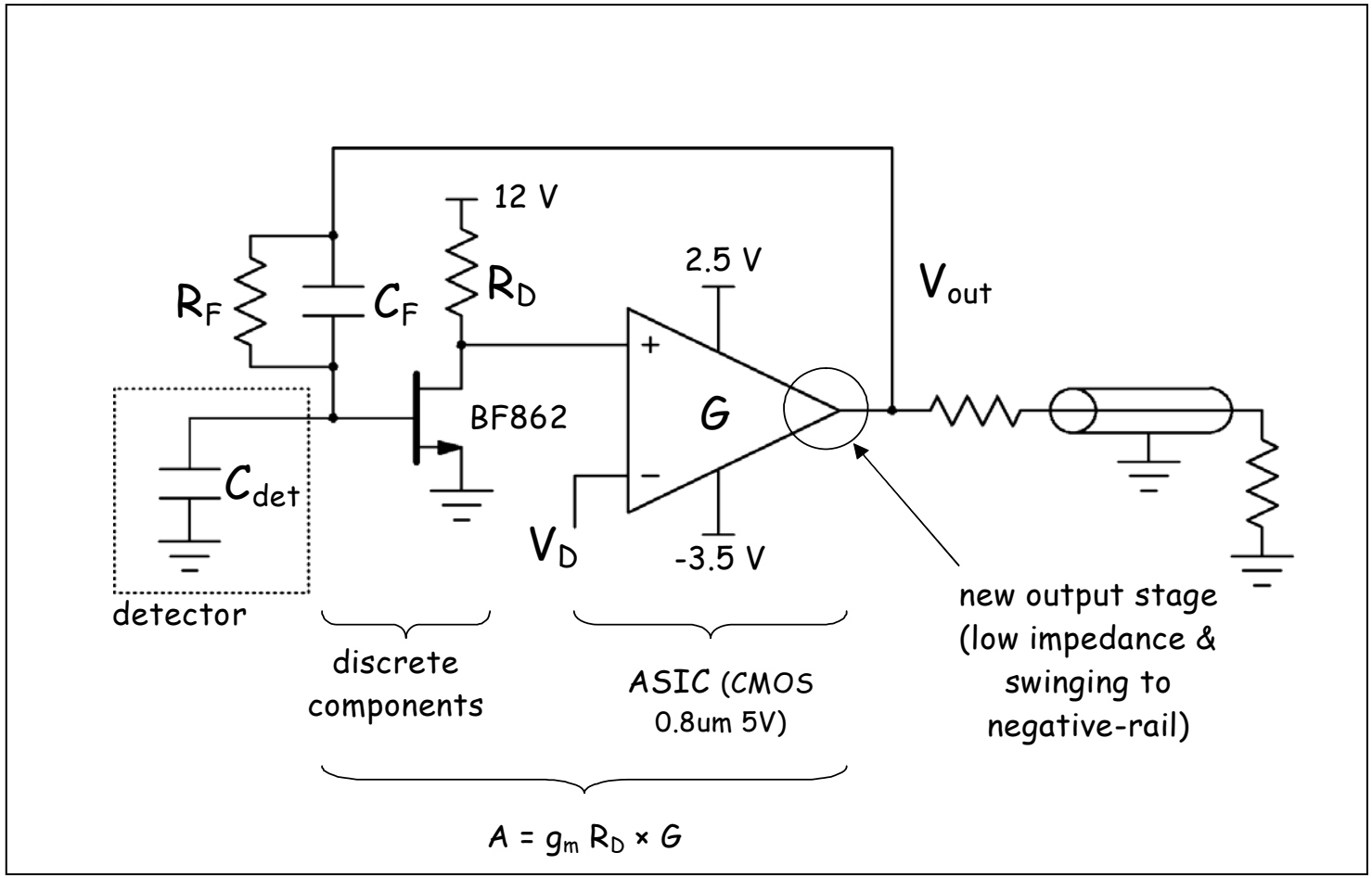
~ 0.5 pF

~ 50 pF

Capacitive divider

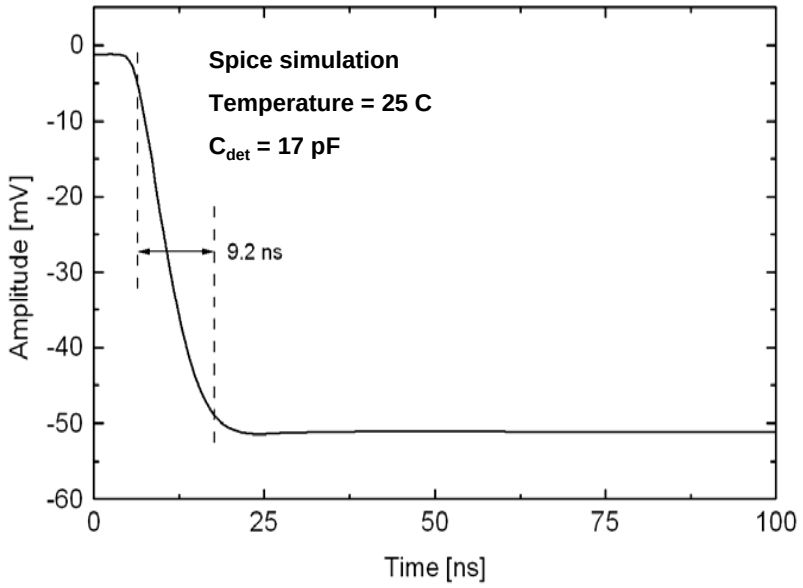
$$A > 10^5$$

Proposed circuit structure (from J. Gal*)

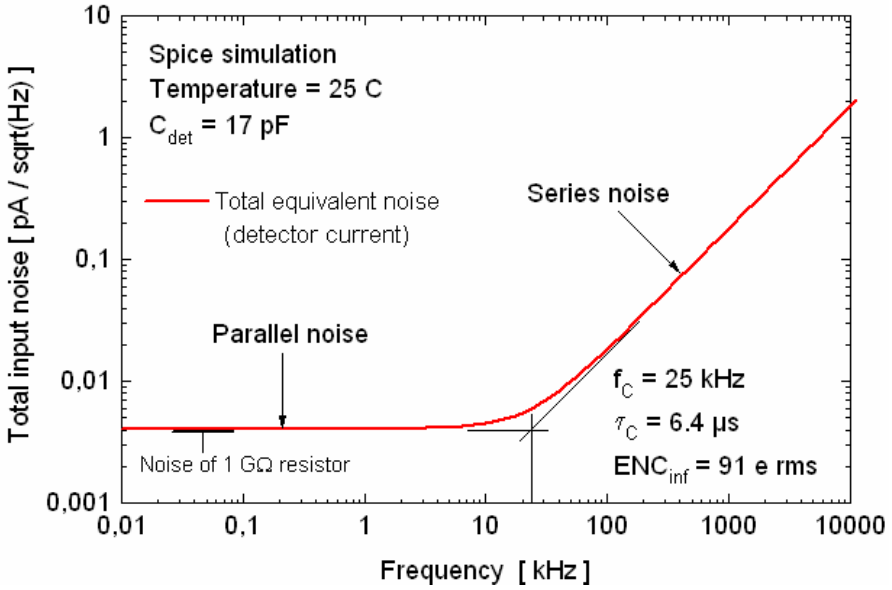


*J. Gal et al. "Realization of charge sensitive preamplifiers using current feedback operational amplifier", Nucl. Instrum. And Meth., Vol. A366, pp. 145-147, 1995

Spice simulation of proposed circuit



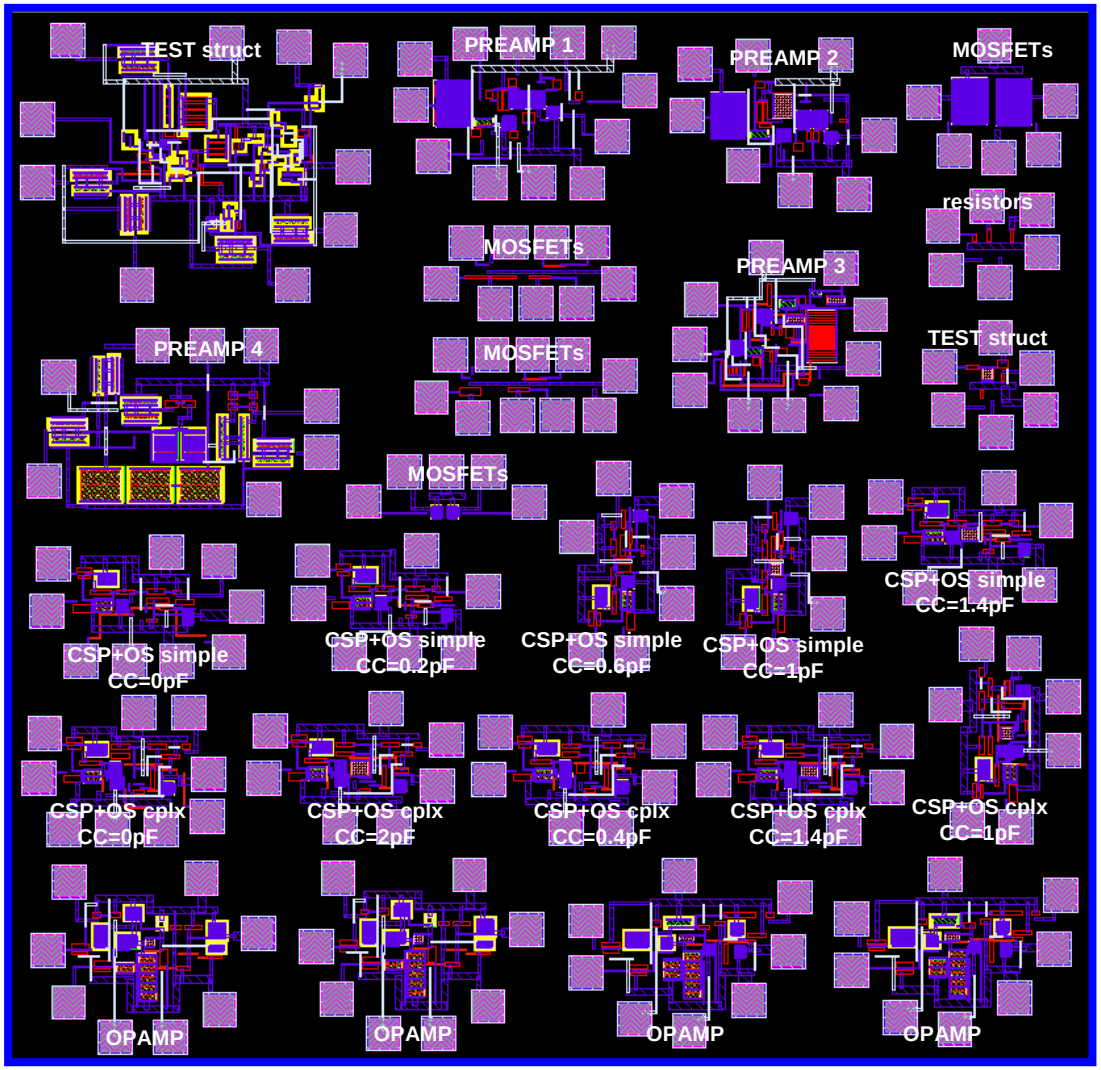
Rise time < 10 ns with
50 Ohm cable
Negative swing = -3.3V



Input referred total noise is low enough:

ENC_{inf} = 91 el. r.m.s.

Test chip



3.3 mm

3.3 mm

PREAMP 1
pMOS + ext R_F + ext bias
Vmax = 550mV (50 Ohm)

PREAMP 2
pMOS + ext R_F + int bias
Vmax = 550mV (50 Ohm)

PREAMP 3
pMOS + reset pMOS + shaper

PREAMP 4
pMOS + ext R_F + ext bias
Vmax = 2V (1 kOhm)
HIGH VOLTAGE comp's

CSP + OS simple
CSP with new rail-to-rail output stage. Various comp cap's

CSP + OS cplx
CSP with new rail-to-rail output stage. Various comp cap's

Conclusion

- A few issues must be addressed before a complete design of an integrated preamplifier for GERDA can be made
- The output stage must be able to drive a 6m long cable maintaining its bandwidth and a large negative voltage swing
- A test chip has been designed to address the most critical issues of this design, which will be delivered in the next months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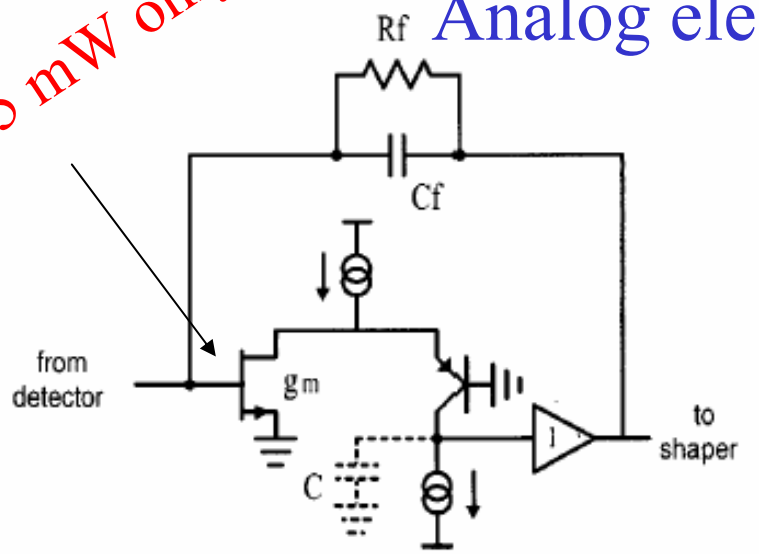

Fig. 2. Simplified schematic of a standard charge preamplifier. The detector adds a capacitance (not shown) at the input of the order of tens of pF for segmented HPGe detectors.

the detector capacitance is increased. In fact the risetime T_r of the preamplifier is given by [4]

$$T_r = C_t \left(\frac{C}{C_f \times g_m} \right) \qquad (1)$$

where

C_t sum of detector, preamplifier-input, and feedback capacitances;

C_f feedback capacitance;

C internal capacitance of the amplifying node of the preamplifier;

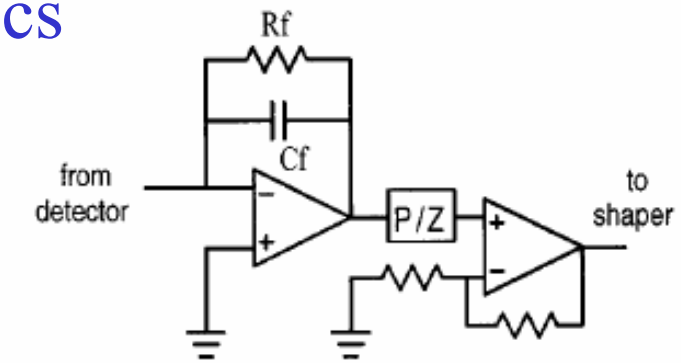

Fig. 3. A standard approach to increase charge sensitivity while reducing the decay time. Note that a P-Z network is required.

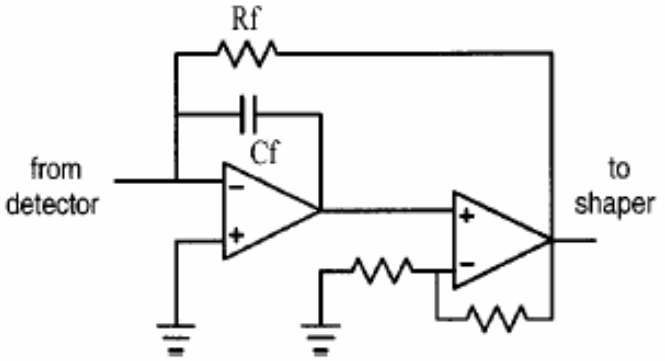

Fig. 4. Proposed approach. The discharge current is increased due to the increased voltage drop across R_f. The decay time constant is thus reduced with no need of a P/Z network.