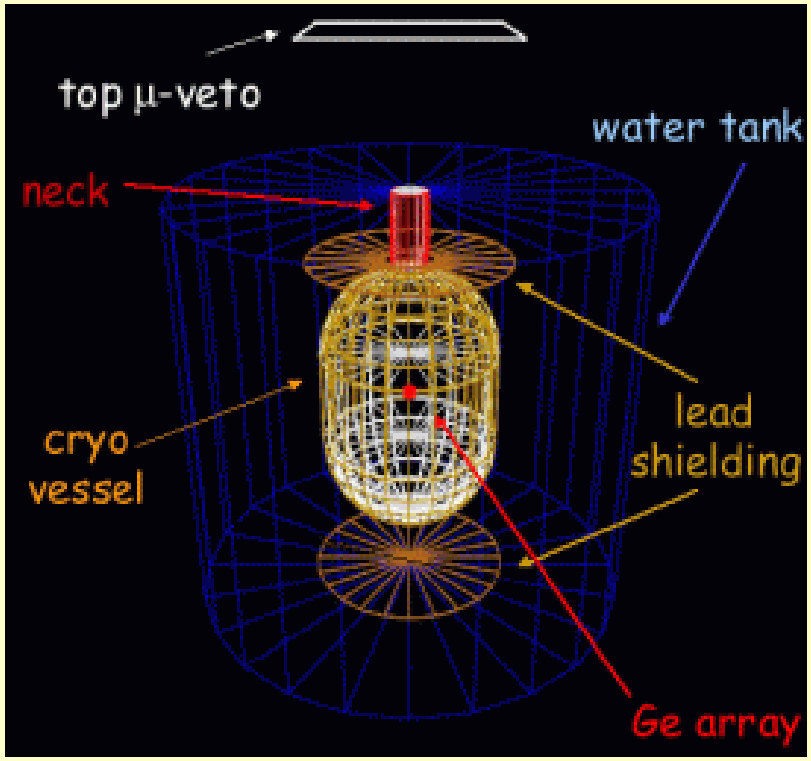
CSA104

, alias **Gullinbursti** (meaning "Golden Mane") a boar in Norse mythology, is a charge sensitive ASIC for the Gerda project.

Schematics and design by ‘FBE ASIC Design & Consulting‘, chip layout by the ‘ASIC labor Kirchhoff-Institut für Physik Heidelberg‘, chip fabrication by ‘X-FAB semiconductor foundries‘.

The Gerda experiment [Ger 04] searches for neutrinoless double beta decay of ^{76}Ge. Germanium diodes made out of isotopically enriched material are suspended in a superinsulated copper cryostat filled with liquid nitrogen (LN) or liquid argon (LAr). Because of ist radiopurity the liquid does not contribute to the background and serves as a shield against external radioactivity. The shielding is completed by an outer layer of water, i.e. the cryostat is mounted in a water vessel. Experimental location is *Laboratori Nazionali del Gran Sasso (LNGS), Italy* .

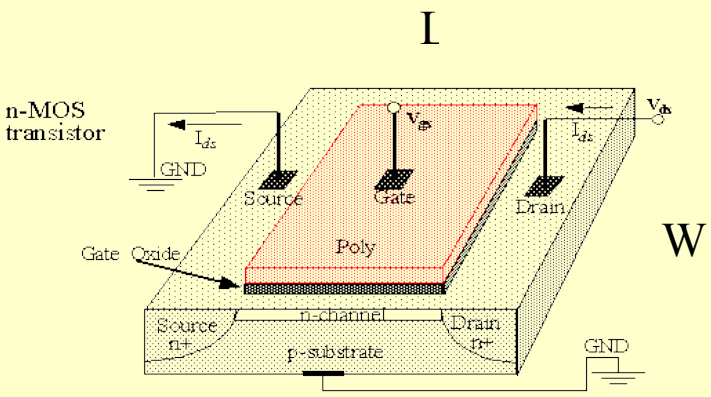


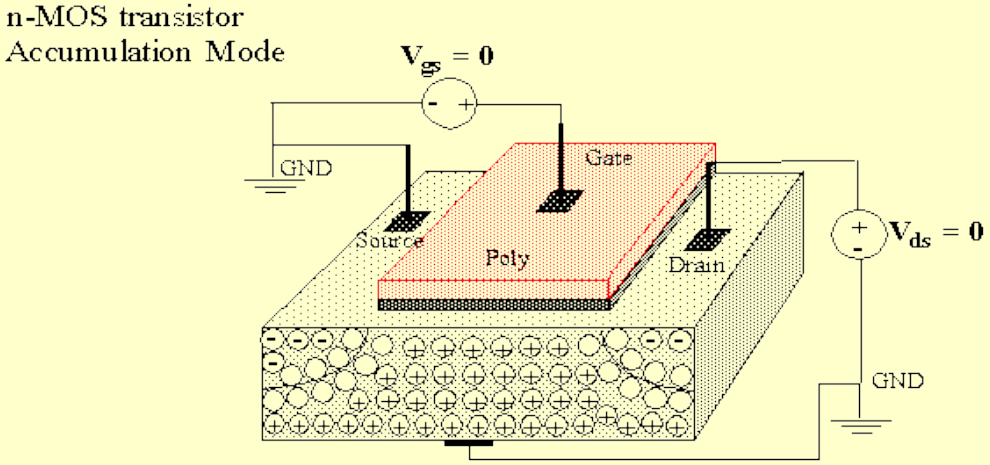
The LN tank is 45m^3, approx 9.1m in height.

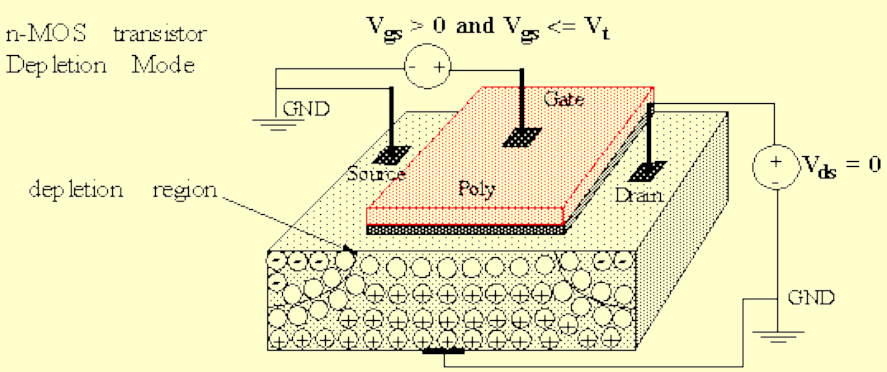
Guestimated number of neutrinoless events is <10 per year, back ground is sub Hz.

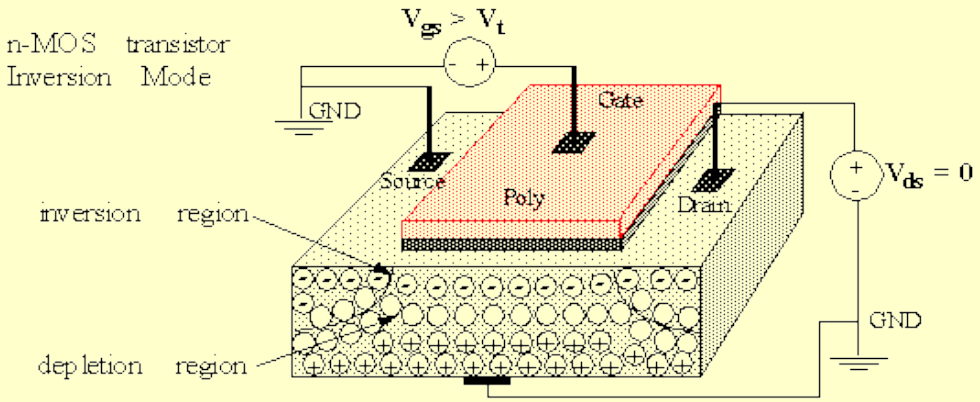
Around 300 electronic readout channels.

A MOSFET reminder.









Demands on the electronics

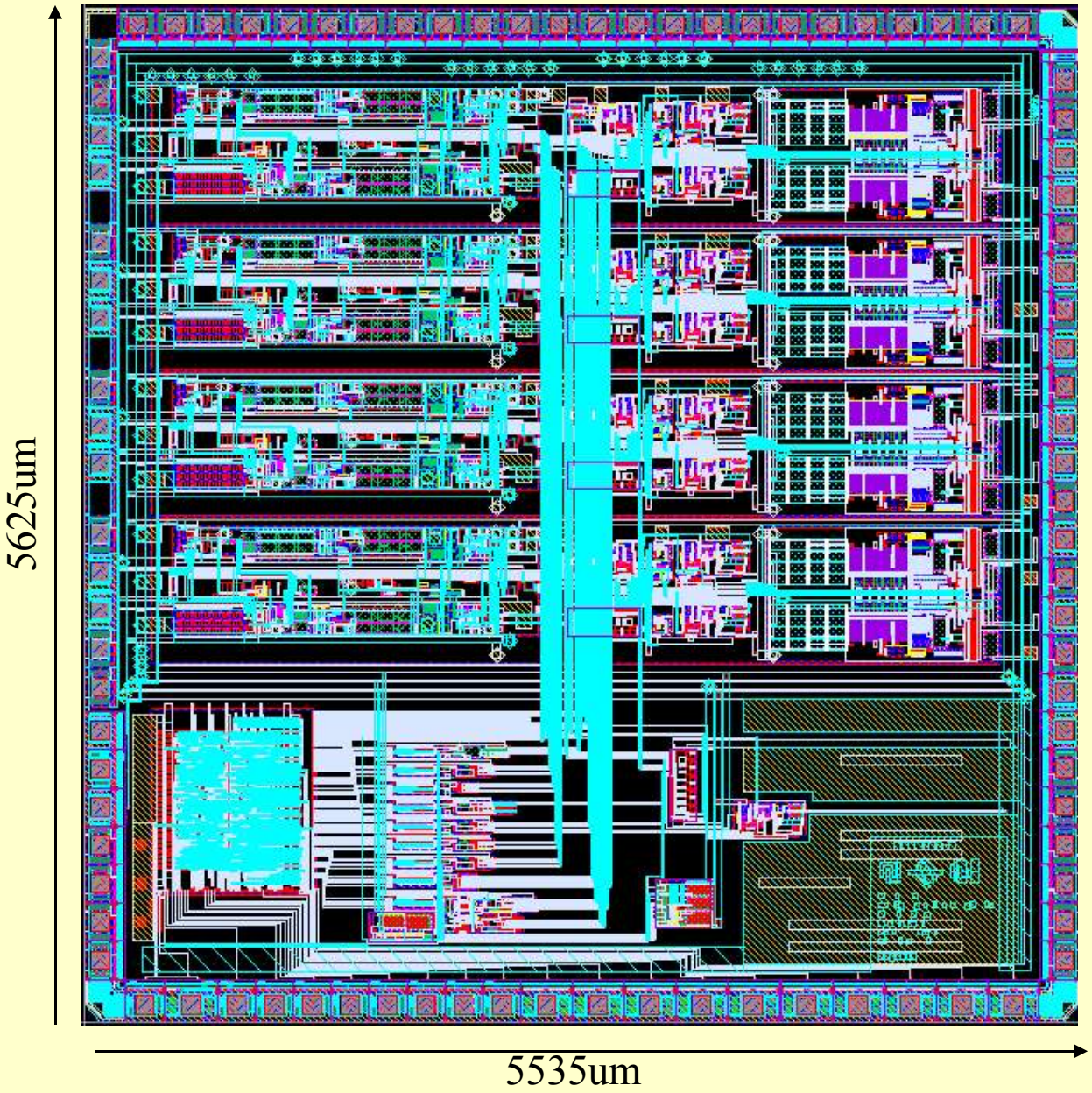
Fully integrated system.
Low power, no bubbling of the nitrogen. 50mW/channel.
Differential voltage output to drive 10m of twisted pair cable.
Total gain 277 mV/MeV (5.9 mV/fC)
Measuring sensitivity 2 keV (625e-)
Dynamic range 5 keV - 10 MeV
Rise time 10 - 30 ns
Linearity DNL will be < 1% to fit a 14-bit ADC. Sensitive to 300e-.
ENC 100 e- at 30 pF load, this is ~20 times less than the Beetle.
Operating temperature 77 K (- 200 ^{o}C), this helps.

CSA104 floor plan

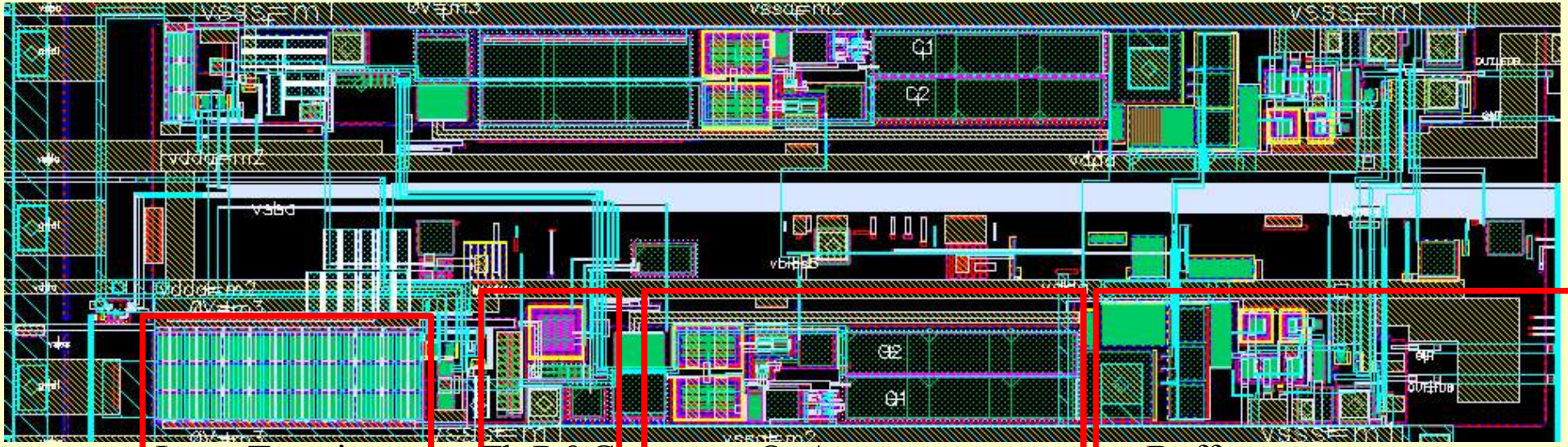
Reference channel #1
Input channel #1
Reference channel #2
Input channel #2
Reference channel #3
Input channel #3
Reference channel #4
Input channel #4

I^2C	Bias Gen

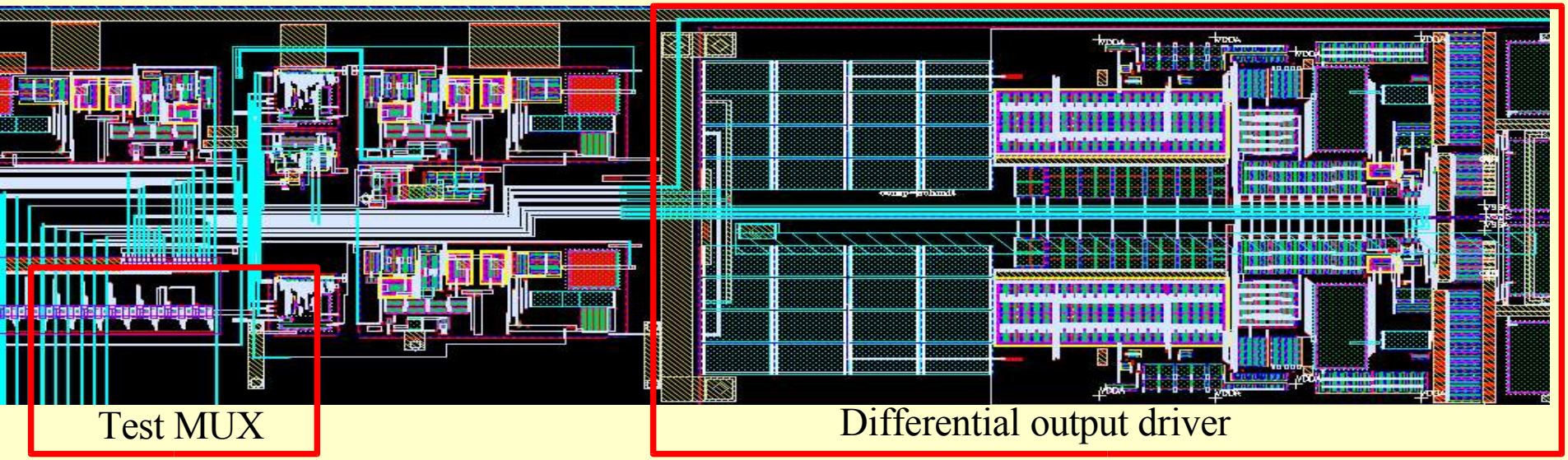
CSA104 layout. XFAB 0.6um 5V process.

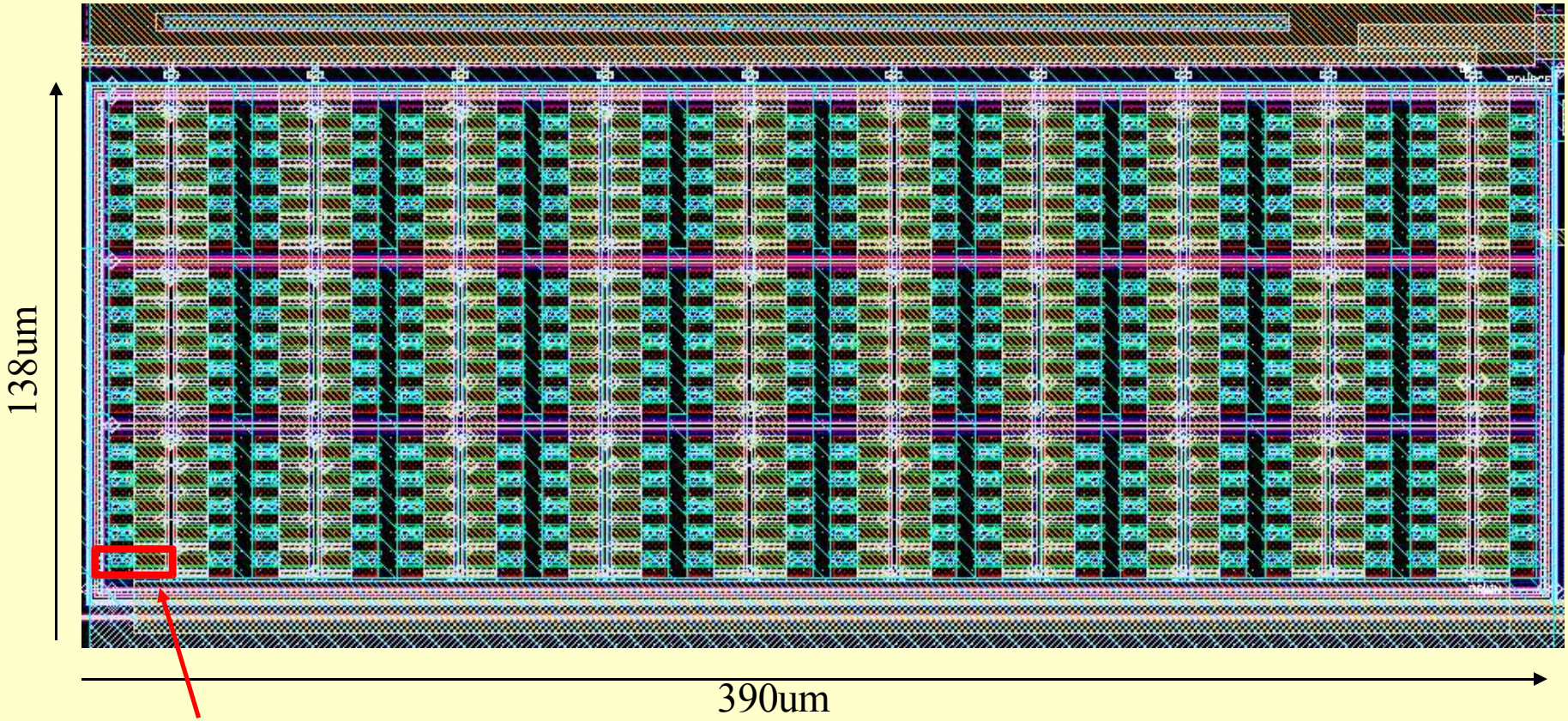


First half of channel



Second half of channel



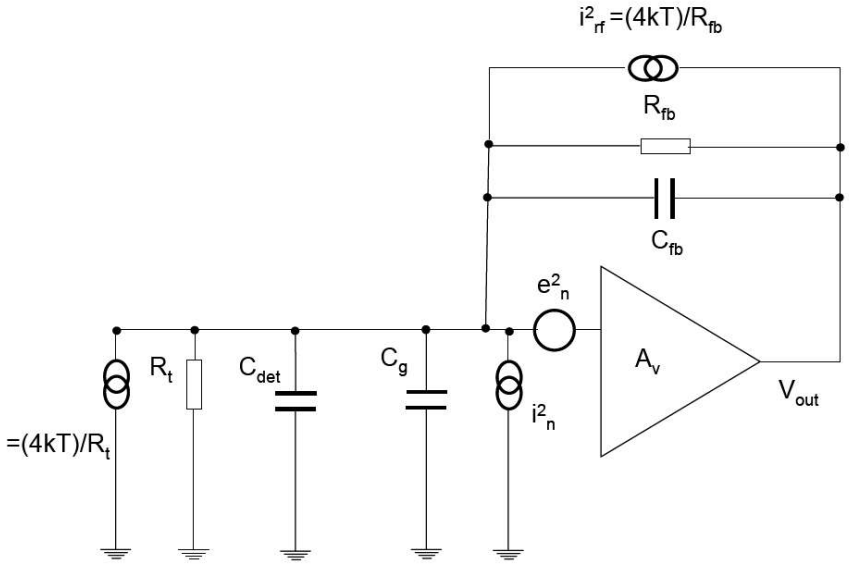


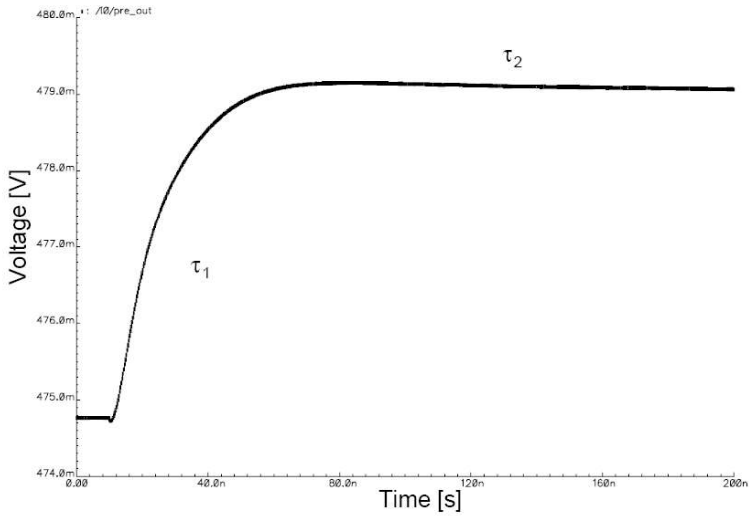
The input transitor is made-up of 600 transitors with a W/L of 15/06 um. This gives a total W/L of 9000/06 um. The total size is ~54000 um^2 (6 times the size of the Beetle Tran).

Why so big? Why PMOS?

$$i_{sn}^2 = 2qI_{DC} \qquad v_f^2 = \frac{K_f}{C_{ox}^2 WLf}, \qquad \frac{8}{3}kT\frac{1}{g_m} \qquad g_m = \sqrt{2k'(W/L)}\sqrt{I_D}$$

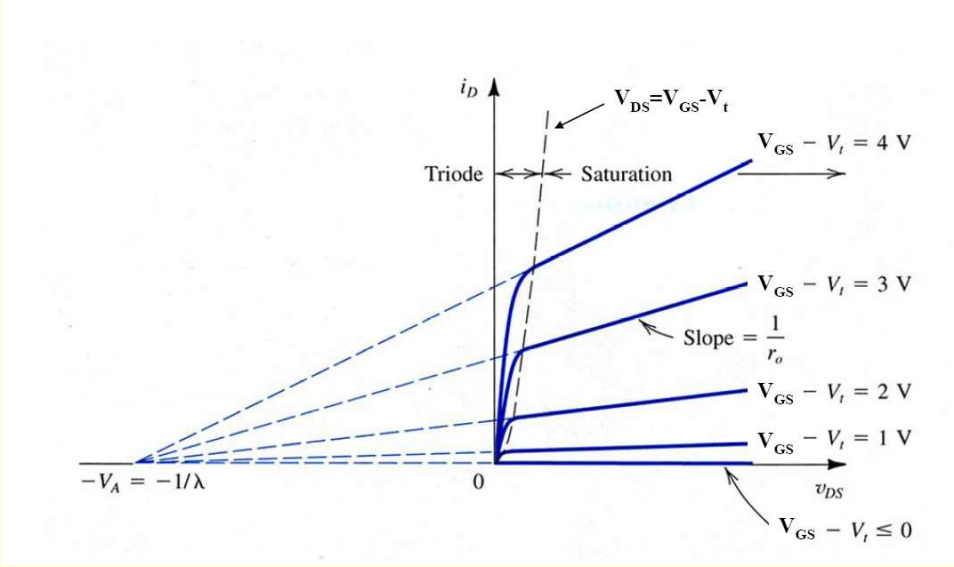
The other source of noise is Rfb. This should be big to reduce thermal noise and the 'ballistic decifit' i.e 99.9% of the signal should be captured.





How to make this big Rfb resistor.

Standard integrated resistor. This would need to be 833mm long. The resistor alone would cost 308k Euros.



With a MOSFET but in what operating mode:

2) In saturation, this would charge the cap.

2) In the triode region where the MOS behaves like a resistor.

for the triode region where $V_{GS} \geq V_t$, $V_{DS} \leq V_{GS}-V_t$

$$I_D = k_n' \left(\frac{W}{L}\right)\left[(V_{GS}-V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right],$$

V_{DS} is the preamp signal output and needs to always be smaller than V_{GS} This makes for a very long transisor.

So it has to be in the subthreshold region where $V_{GS} < Vth$. Here the transistor is turned off, and there is only a leakage current between drain and source. Very hard to control.

Project Status

The schematic and layout is complete and has passed the LVS.

The layout was sent to XFAB on the 08/02/06 for DRC checks.

The layout passed the DRC checks on the 09/02/06.

The chip fabrication process started on the 10/02/06

The 25 chips are expected back mid May.