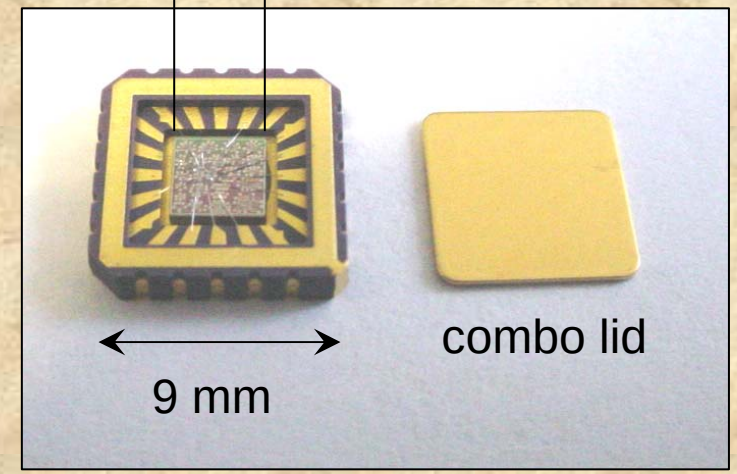
STATUS report on FE and related components.

C.M. Cattadori on behalf of TG3 WG

OUTLINE

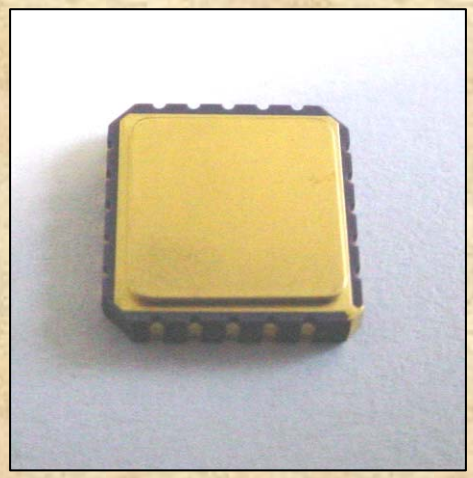
- Overview of ASIC Front- End circuits in advanced phase of development
- Choice of PCB material (Support for FE circuit). Cuflon is now preferred material
- Cables (HV and Signal). No new since Rindberg
- Feedthroughs (HV and Signal).
- LV Power supply

Chip PZ-0 (v1 & v2) for GERDA



Case 20LCC - open

Case 20LCC - closed



Lid can be soldered with Au-Sn alloy or other solder paste

Version v1: C_{comp}= 1pF (T_{rise}= 17ns)

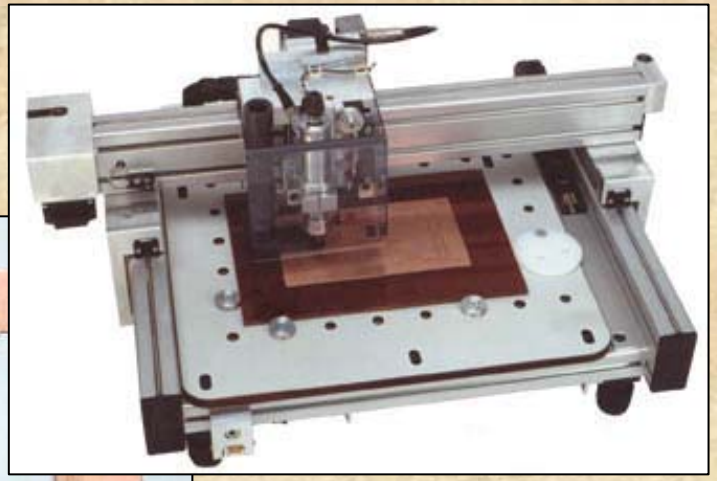
Version v2: C_{comp}= 0.6pF (T_{rise}= 13ns)

ENC = 150 e^- rm.s.

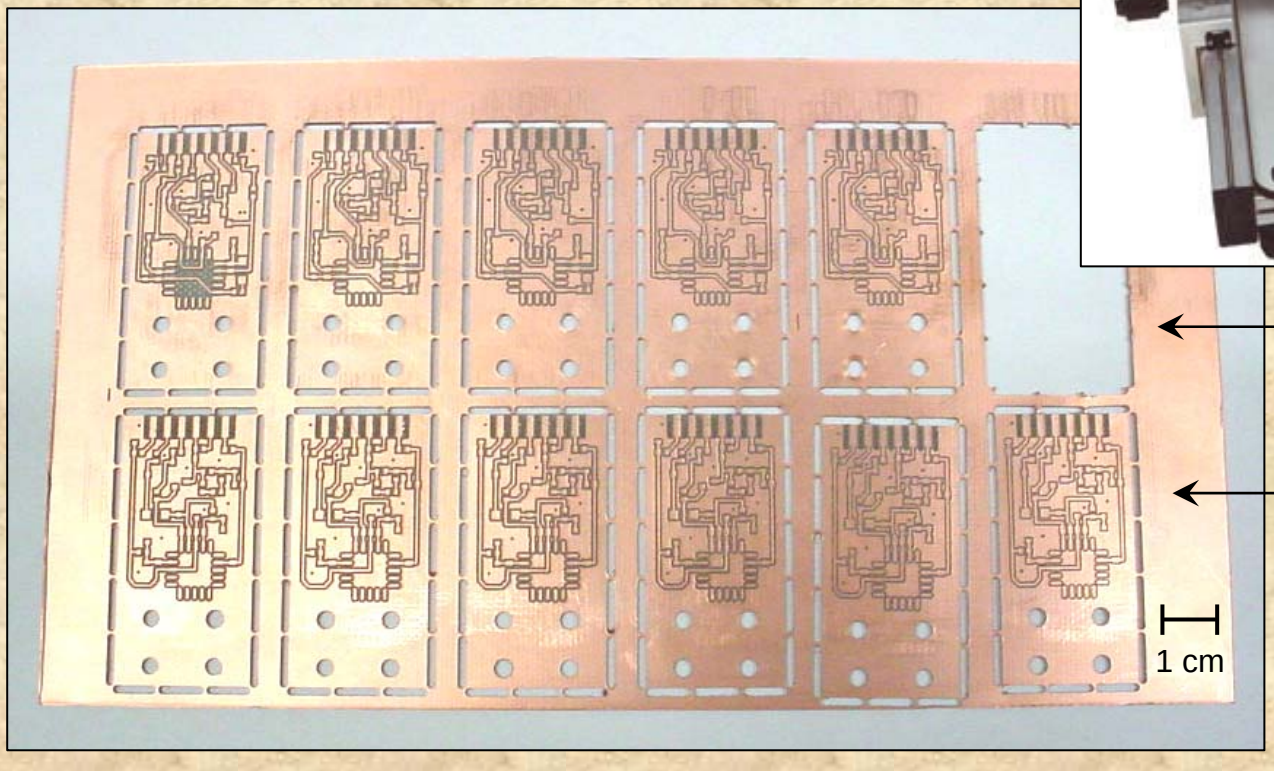
C.M. Cattadori- INFN MiB & LNGS

Preparation of Printed Circuit Board

Bungard CCD/2 milling machine



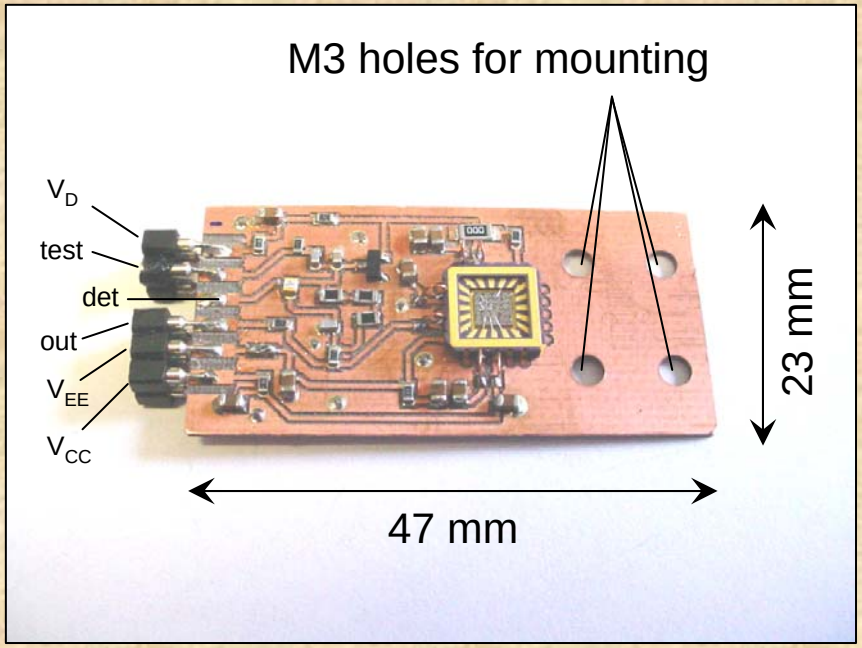
0.8 mm PTFE laminate



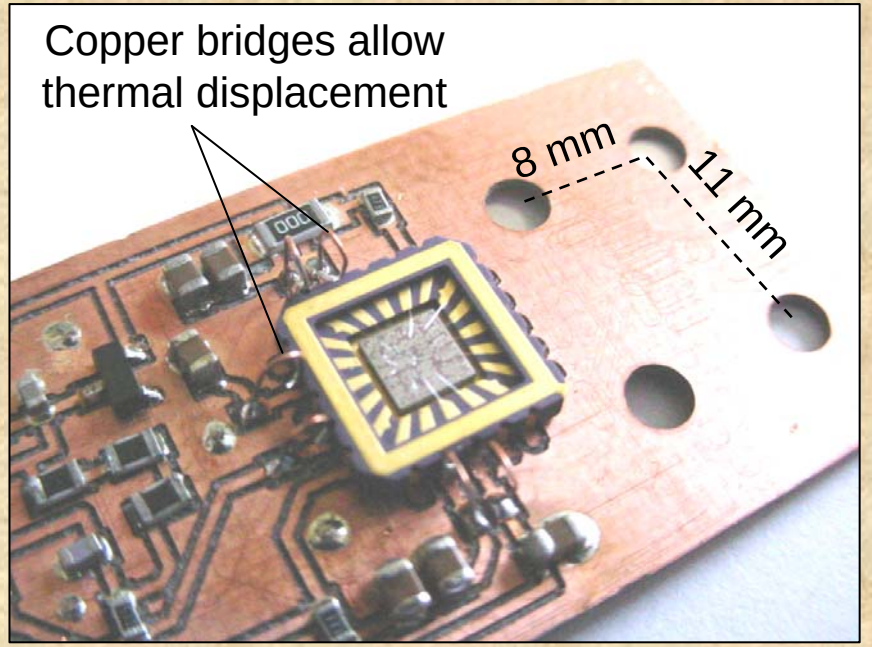
6 PCB's for PZ-0 (v1)

6 PCB's for PZ-0 (v2)

PCB + chip PZ-0 (v1)



PCB as shown with chip and bias components installed



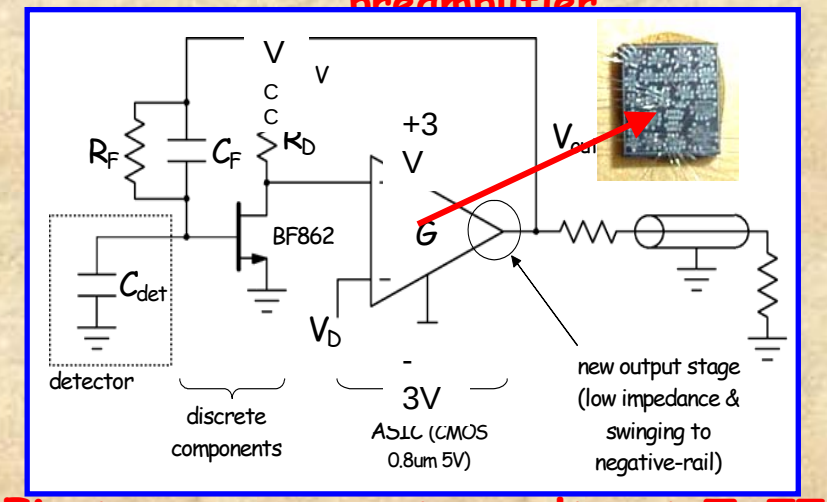
Detail of the board. The 20LCC case is not yet closed

Mass of PCB + components (no chip) is 2.55g
Mass of chip (including case) is 0.35g
Total mass = 2.90g

Performance:
as already shown

(F. Zocca 'Status of CMOS FE Electronics, GERDA meeting, Heidelberg Feb 2006)

Tested circuit structure: external BF862 JFET + 0.8μm 5V CMOS single-ended preamplifier



First measurement results at T=77°K

(C_F = 0.15pF, R_F= 1GΩ, C_{det} = 15pF)

Negative output voltage swing: ~ 2.4 V

Energy sensitivity (C_F = 0.15 pF) : ~ 185 mV/MeV after 50 Ω termination

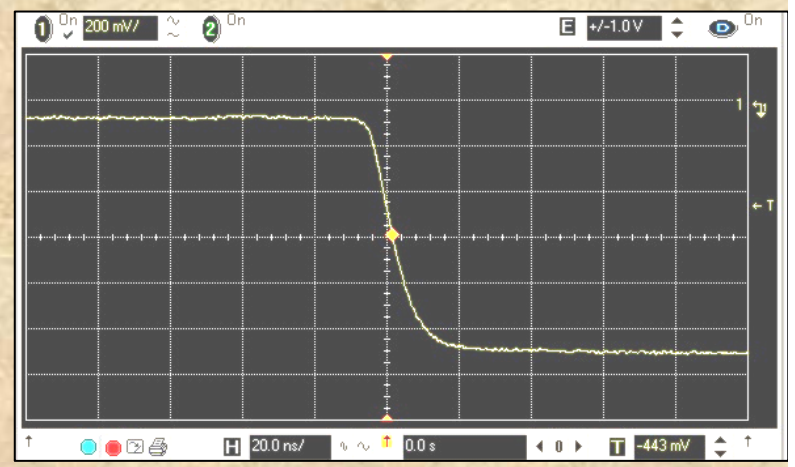
Input dynamic range: ~ 6.5 MeV

Rise time: ~ 15 ns driving 10m cable

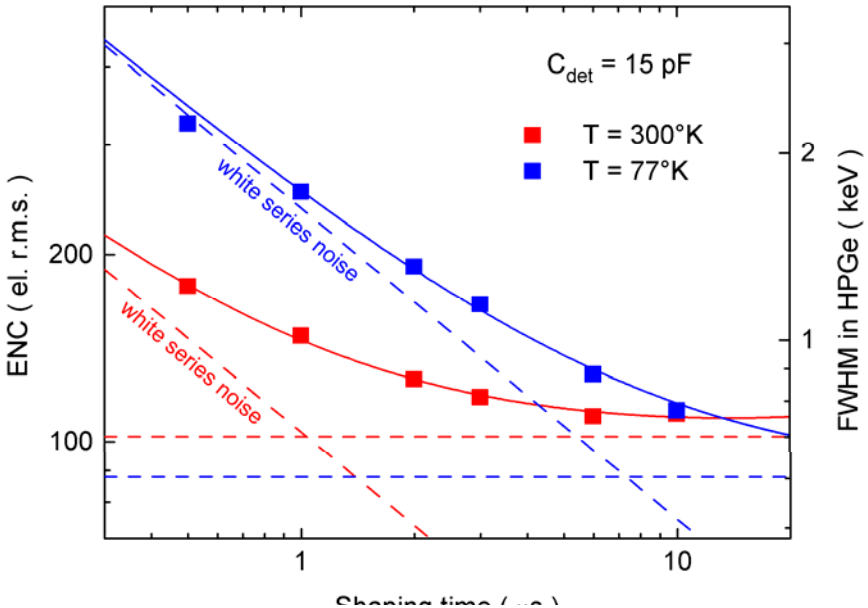
Minimum ENC (C_{det}= 15pF) : 112 e^- at τ_{shap}=10μs

Total power consumption: ~ 25 mW

Acquired output signal driving a 50 Ω coaxial cable of ~ 10 m : rise time of ~ 15 ns



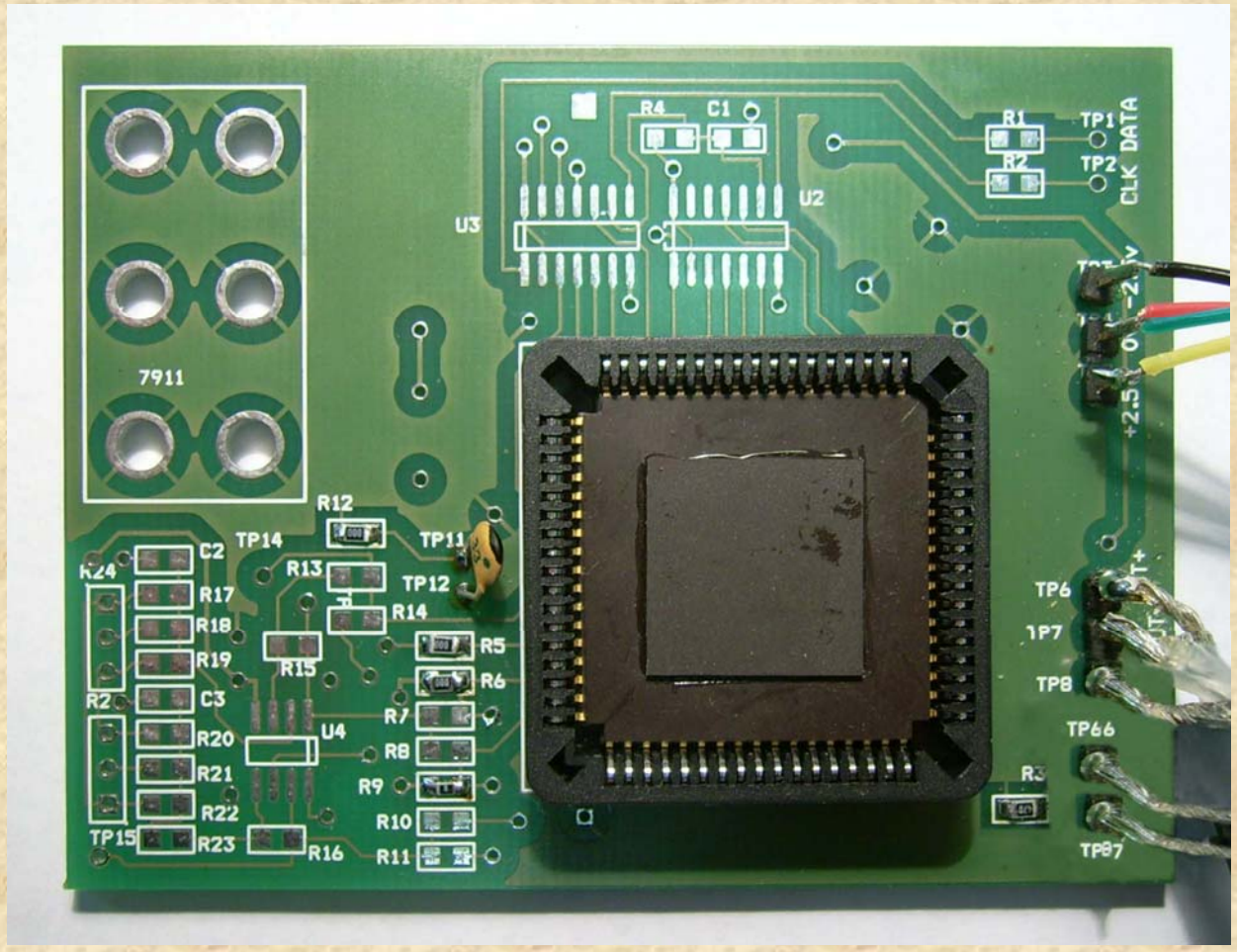
Comparison between noise measured at room temperature (T=300°K) and in LN (T=77°K)



Status of PZ-0 (v1)

- 2 chips wire bonded (each with both v1 and v2 versions)
- 6 PCB's for PZ (v1) and 6 PCB's for PZ (v2) milled
- 1 PCB for PZ-0 (v1) fully mounted and tested @ room T
- 1 PCB for PZ-0 (v2) fully mounted
- Sealing of lid succesfully tested in LN
- Chip availability: 16
- Time needed to fully mount & test 10 boards: two months (but test with detector is needed before "production")

PCB for GERDA PZ-1
Fully Integrated Preamplifier



Performances: as already shown by S. Riboldi ”Charge Preamplifier with Fully Differential Line Driver Integrated in AMS CMOS 0.8um CZX Tech. for the GERDA Experiment” GERDA Milano meeting – November 2006

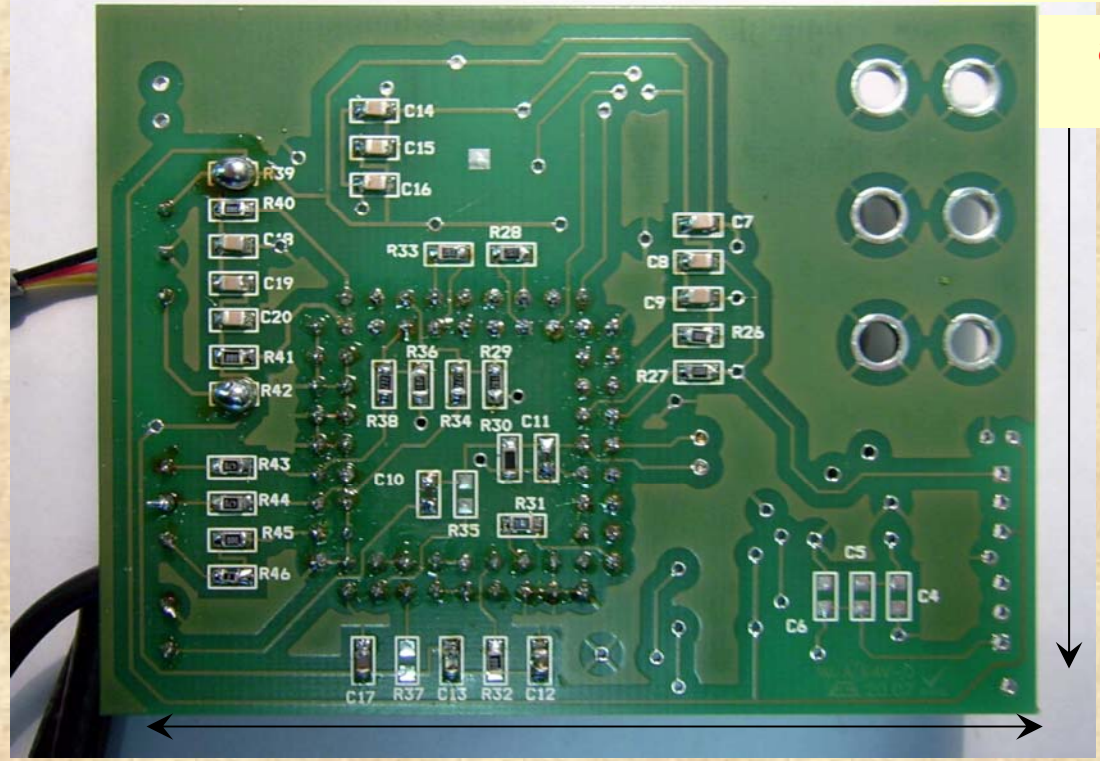
PCB for GERDA PZ-1
Fully Integrated Preamplifier

All discrete passive elements are to be integrated in the next IC revision…(as shown in GERDA 2006 Milano Meeting)

PCB bottom laye

…except for 2 or 3 capacitors

and for the 1 GOhm feedback resisto
(in case the “fast reset” is not used)



60 mm

PCB dimension far to be Definitive. Once all the Digital Current Generators ar Thresholds will be fixed, board dimension can be redu down to (40 x 20) mm

80 mm

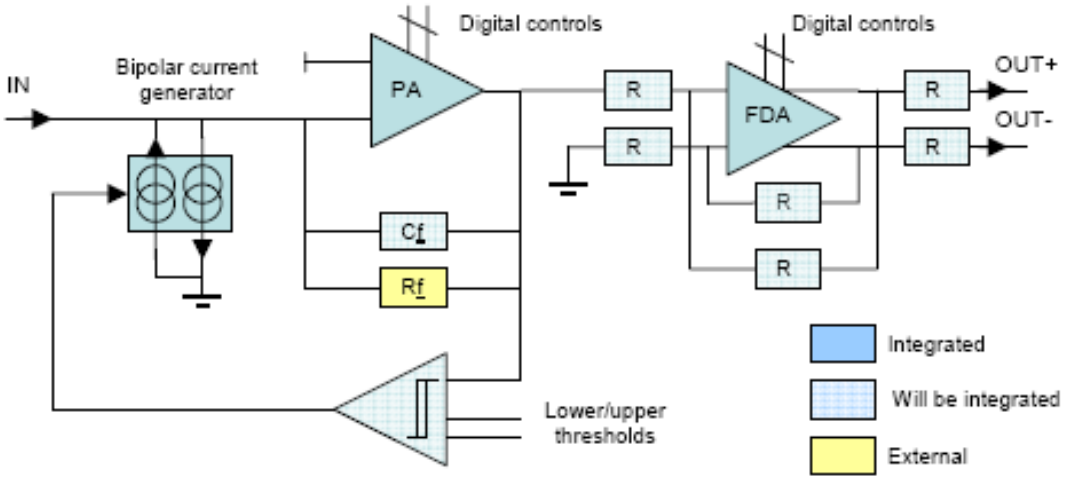


Fig. 1 : Schematic design of the front-end electronics as in Fig. 3, showing the preamplifier (PA), the fully differential amplifier (FDA) line driver, the bipolar current generators (integrated) and a few discrete passive elements on the PCB (resistors and capacitors) that will be also integrated in the next version of the electronics. Bipolar current generators and external comparators will implement a pulsed reset control scheme, also to be tested in the future. The FDA line driver has an additional input (not shown) to set the common mode voltage of the output signals.

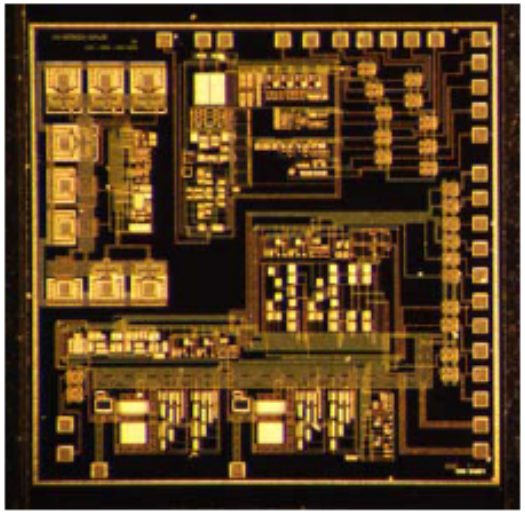
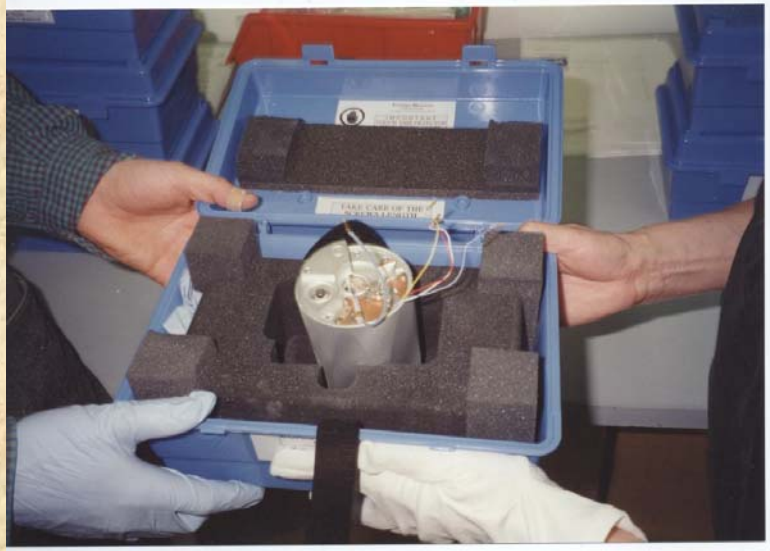


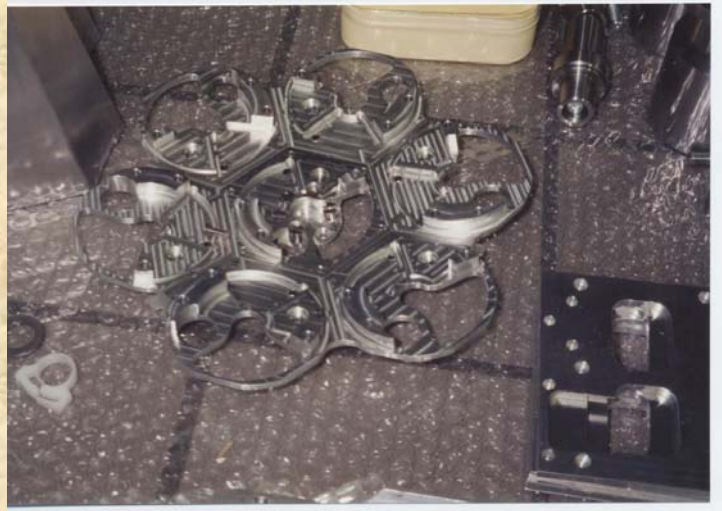
Fig. 2 : Front-end electronics IC
(Area = 9 mm^2, MOS devices number > 200,
AMS HV CMOS 0.8 um CZX tech.)

Cdet = 33 pF , Cf = 1 pF, Rf = 1 GOhm, Rloads = 50 Ohm, Power supplies = ± 2.5 v, FDA gain = 2.4	
BW (PA+FDA)	≈14 MHz
Rise time (PA+FDA)	25 ns
Idle bias current	9 mA
Output voltage swing (before 50 Ohm series res.)	± 2 v
Noise @ 25 C (12 us pk.t. gaussian shaping)	230 e rms
Noise @ 77 K (12 us pk.t. gaussian shaping)	165 e rms
Noise @ 77 K (optimum shaping by DPLMS)	150 e rms

Status of GERDA PZ-1
Fully Integrated Preamplifier

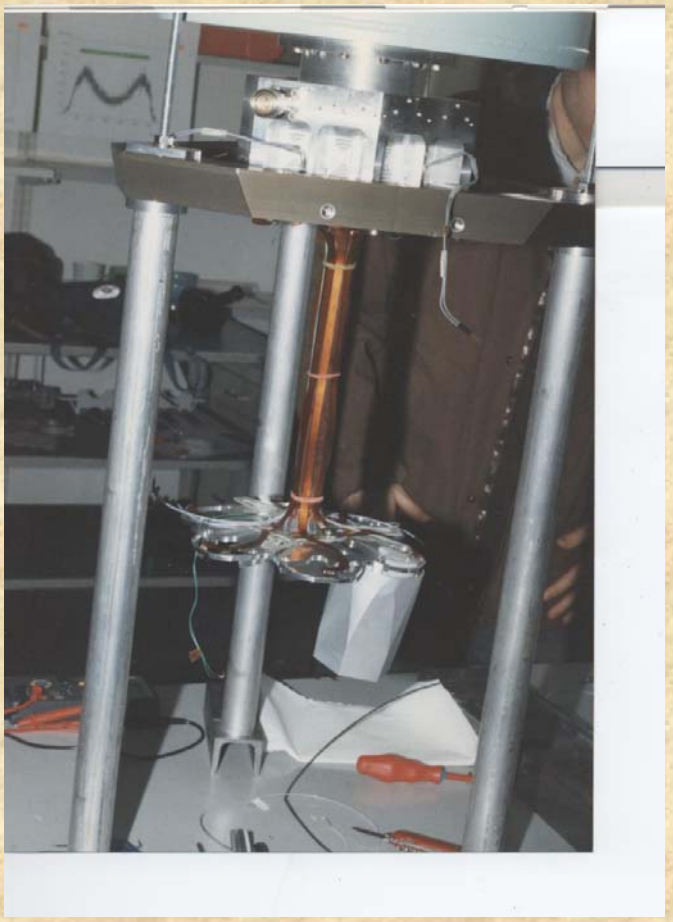
- 2 ICs bonded (lid sealed with epoxy glue)
- Circuit tested at both r.t. and l.n.t
- IC is robust, beware of fragile bonding wires…!!!
- Prototype PCB populated and tested
- Chip availability: 30 pcs
- Time to set-up 10 preamps: two months
  (manufacturing “commercial PCBs”, bonding ICs)
  (1500 euros + bonding costs)
- Weights: IC < 0.1 g ($3 \times 3 \times 0.4$ mm^3)
  actual IC package = 3 g (could be lower)
  actual PCB = 15 g (could be much lower)





Euroball capsule: we plan to use it for FE testing.

Al capsule EB welded (Eurysis type)



Euroball capsule mounted on its cold finger (suited to cool down 6 capsules).

We will receive only the capsule, no cold finger and connecting plate.

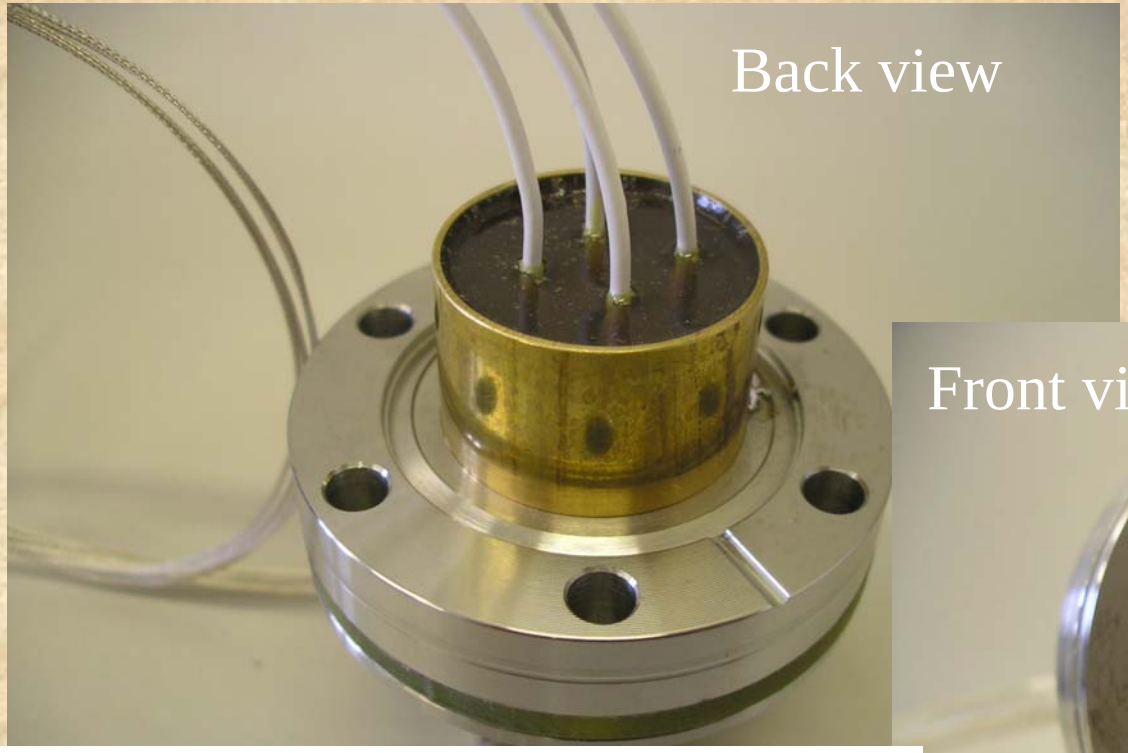
With this capsule we will be able to test only PZ-1, not PZ-0 (external FET), as the latter has been Optimized to read holes and not electrons.

New Dewar + closed chamber ready (since 3 months) at LNGS to be the electronic test facility but crystal is missing. Urgent to start to build the first complete read-out chain, from FE to PSA.

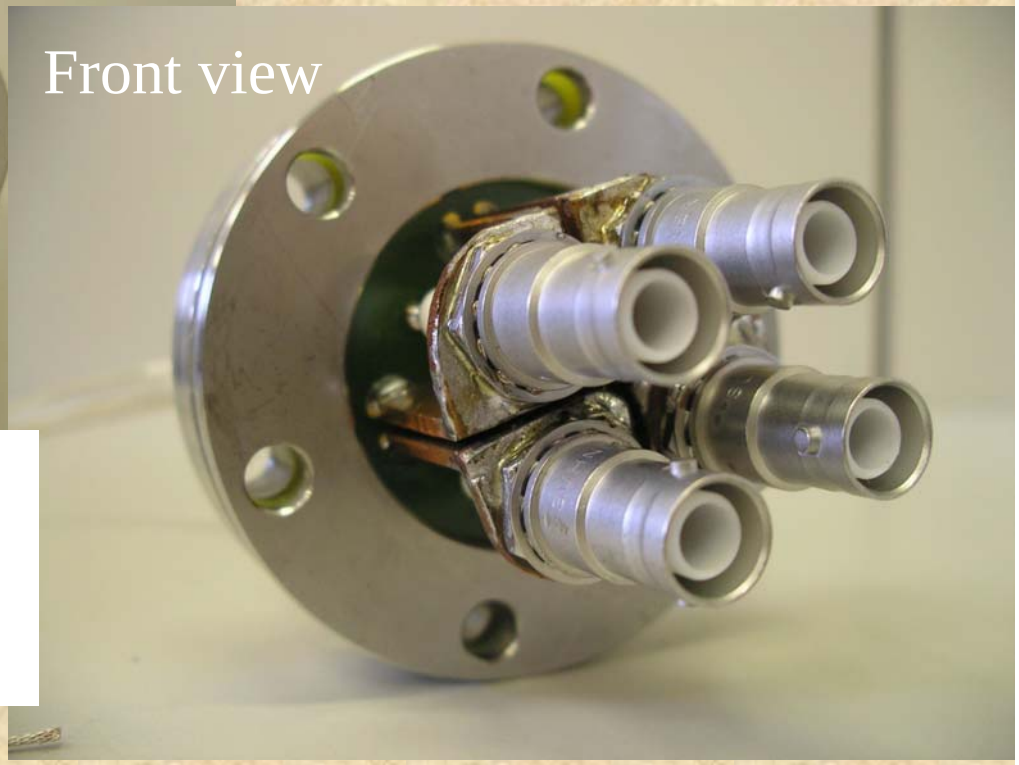
Low Voltage Low Noise PS designed at PD –INFN V=+12 V, V=+5 V, V=-5 V, I = 0.7 A each)

Units in NIM modules delivered to LNGS, by INFN-PD

HV flanges against discharges: Developed and patented by INFN PD. 9 flanges ordered



Signal and LV Connectors: Fisher 102



Other option: SHV Stycast insulated. Demonstrated to work at LNGS 1 month run+ multiple HV cycles in Ar atmosphere

Adopted Cables for present tests

1st choice HV cable: Kapton coaxial cable. Tested up to 4.5 kV. Weight ~ 3 g/m

Alternative option: Cu-Teflon insulated (no coax), Thicker Kapton coax (already available)

Signal: micro-coax Kapton 50 Ω @ LAr (used in calorimetry) for single-ended PA, or RG316 (coax PTFE insulated 10 g/m)

Weight ~ 3 g/m

Not yet investigated (but sample availables for γ spectroscopy meas) twisted pairs for differential out PA, (PTFE insulation, Siltem insulation)

Cables

Taking 10 mBq/kg (actual upper limit of γ- meas on Th and U on HV cable)→ 60 μBq from last meter of HV+signal cable (nearest to electronic).

Need more γ- spectroscopy meas, to screen cables and PCB/Crystal cables material (Cuflon) not yet measured. Once circuit pick-up, it has to be mounted on best-radipure PCB material

Conclusion

- FE circuits: good choice of circuits,ASIC are advancing. Urgent to test with crystal.
- Euroball capsule available for test but not exactly the first choice.
- Once test done need another production run, and then design and test PCBs for string.