GERDA DAQ - quo vadis?

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(temporary T9 coordinator)

Contents:
- FADC requirements
- FADC options
- possible DAQ structure
- slow control

active people

Alexander Burenkov (ITEP), Carla Cattadori (LNGS), Matthias Junker (LNGS), B.S., Calin Ur (Padova), ...

interested people:

Iris Abt (Munich), ...

FADC requirements

(feel free to comment!)

sampling frequency:

- Nyquist theorem: sampling freq > 2x analog bandwidth
- "rule of thumb": sampling freq > 10x BW ?

analog performance:

- measure energies from 2 keV to 8 MeV
- resolution should not be influenced by FADC noise
  → since signal is sampled over O(1000) time bins, 10 bits are ok (?)
- dynamic range from 2 keV to 8 MeV in one channel (?)

do we need 12 or 14 bit FADC ??? Since 14 bit FADCs are available …

system integration:

- generation and distribution of trigger
- external clock input?
- data readout speed (for calibration runs)
- supported readout modes

FADC solutions (1)

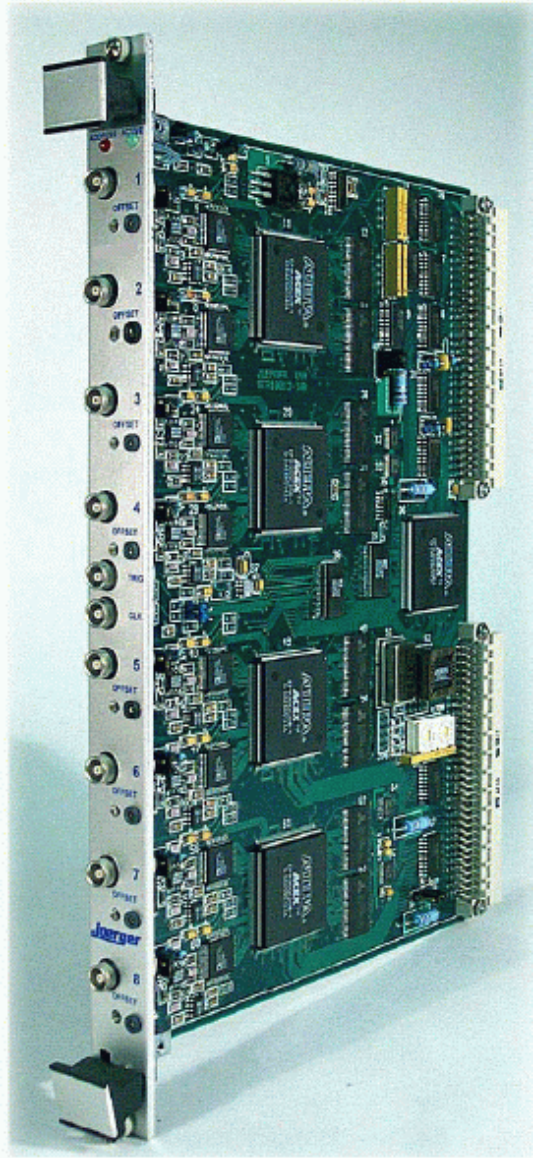
Struck SIS3301

- 6U VME board
- 14 bit, 105 Msps
- Effective Number Of Bits (ENOB) = 12
- digital Finite Impule Response (FIR) filter for triggering
- 2 memory banks per channel, 256k each
- memory can be divided in e.g. pieces of 2k / event
- single ended or differential input
- combination of large number of modules possible (common trigger, clock)

No waveform analysis on board

FADC solutions (2)

Joerger 10014

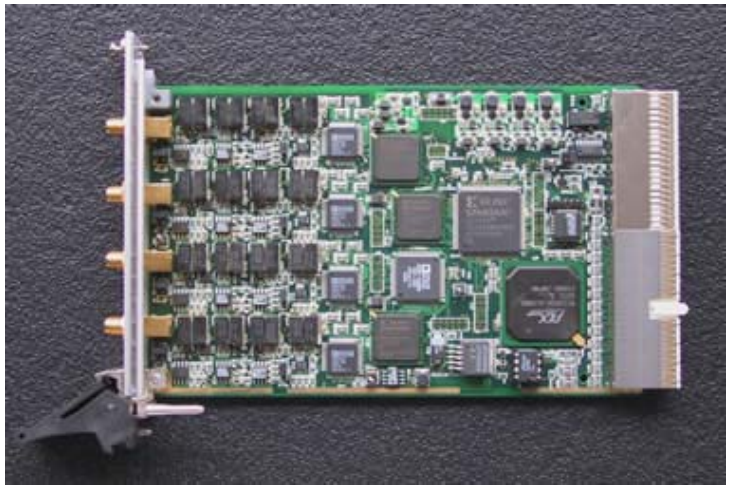


- 6U VME board
- 14 bit, 100 Msps
- analog input amplifier / channel
- single ended or differential input
- up to 512k memory / channel
- memory divisible in 16 sections
- trigger = comparator
- combination of many boards possible
- low power consumption

No waveform analysis on board

FADC solutions (3)

XIA – Pixie4

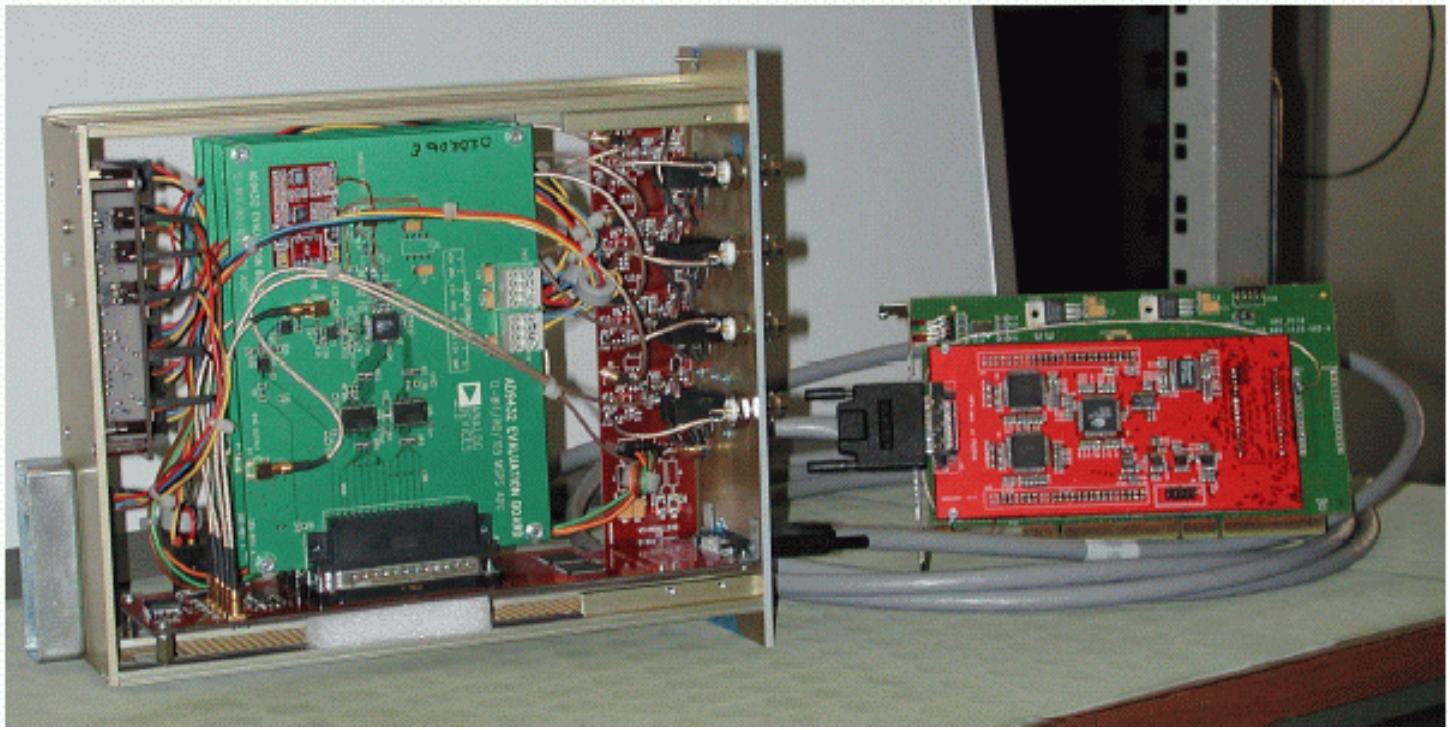


- 3U PXI card
- 14 bits, 75 Msps
- analog signal processing (gain, offset)
- FIR filter for triggering
- lots of signal processing on board
- combination of many boards possible

optimized for operation as Multi Channel Analyser (MCA), readout of event waveform "not supported"

FADC solutions (4)

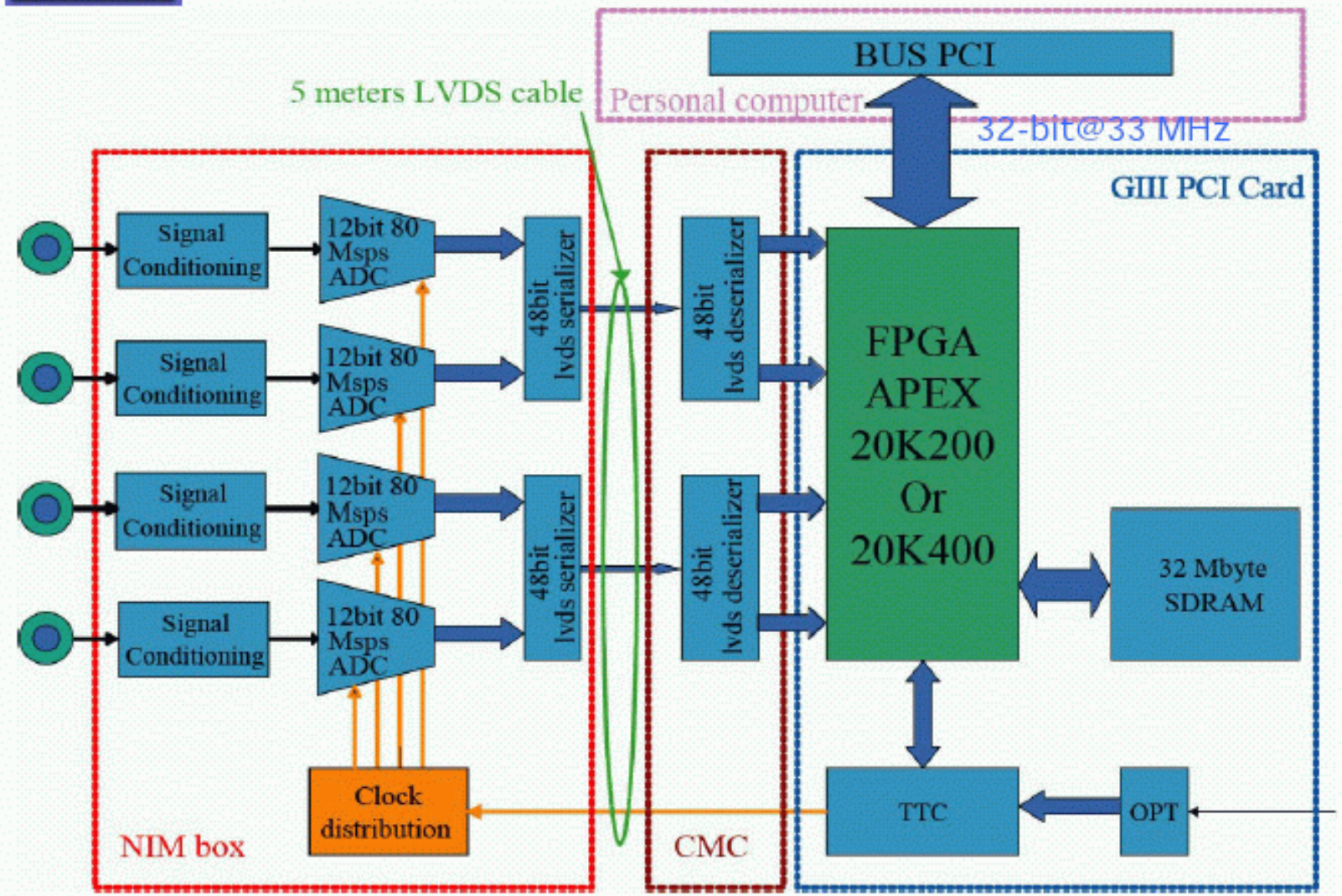
MD^{2}S readout from INFN Padova



- ✓ FADC in NIM crate, digital electronic = PCI board
- ✓ 12 bit, 65-80 Msps

see talk of Calin Ur in Munich, Sept 2004

MD²S *Block Diagram*



Plans for the next months

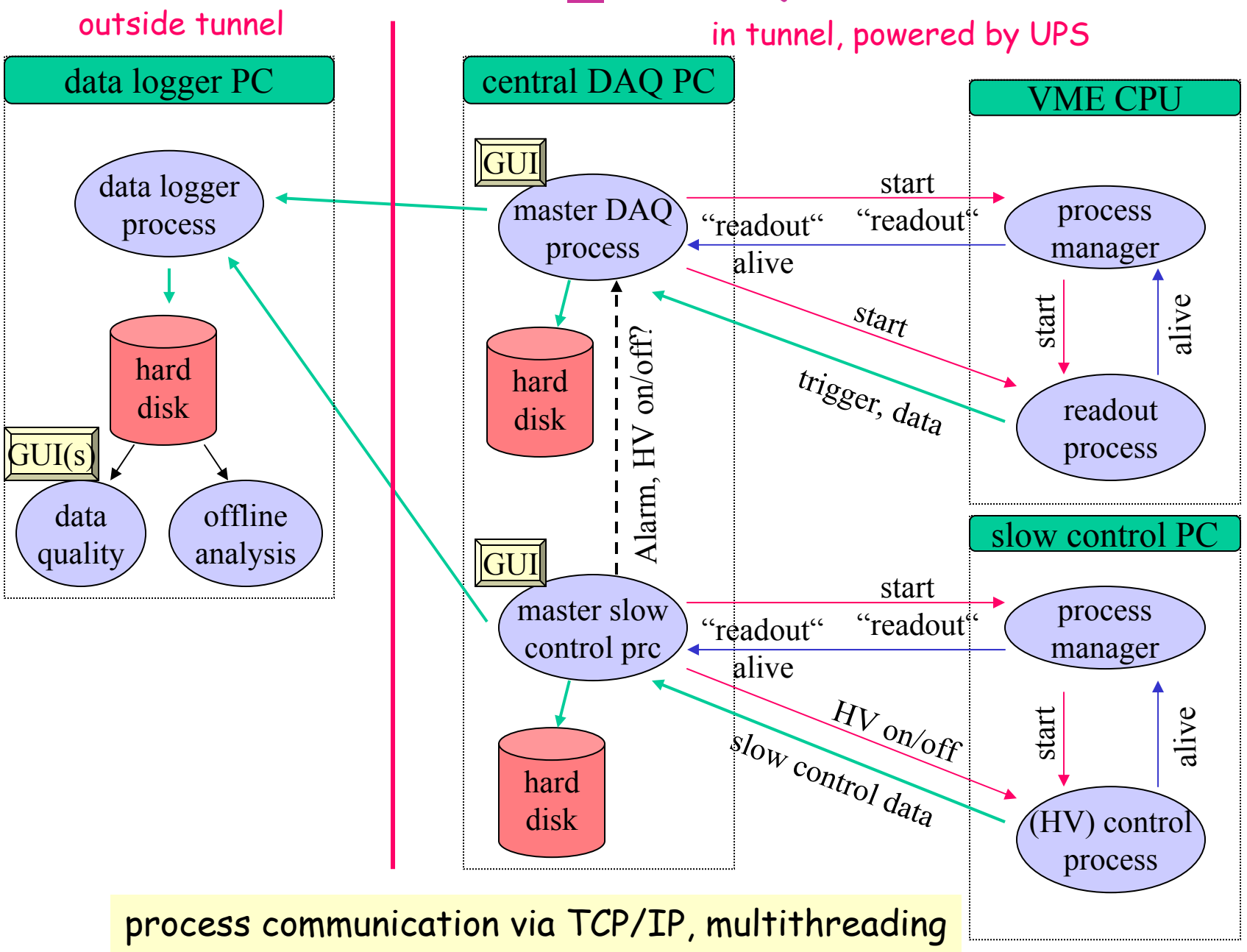
- define test procedure for analog test of FADC solutions
  (measure ENOB, temperature drifts, ...)

- define requirement for DAQ integration
  (trigger generation and distribution, synchronization, speed, ...)

- decide by the next collaboration meeting which FADC to use

- build the DAQ according to the chosen solution
  for phase I: only ~20 channels → a working solution
  can be implemented quickly
  for phase II: ~ 200 channels → more scalable solution needed

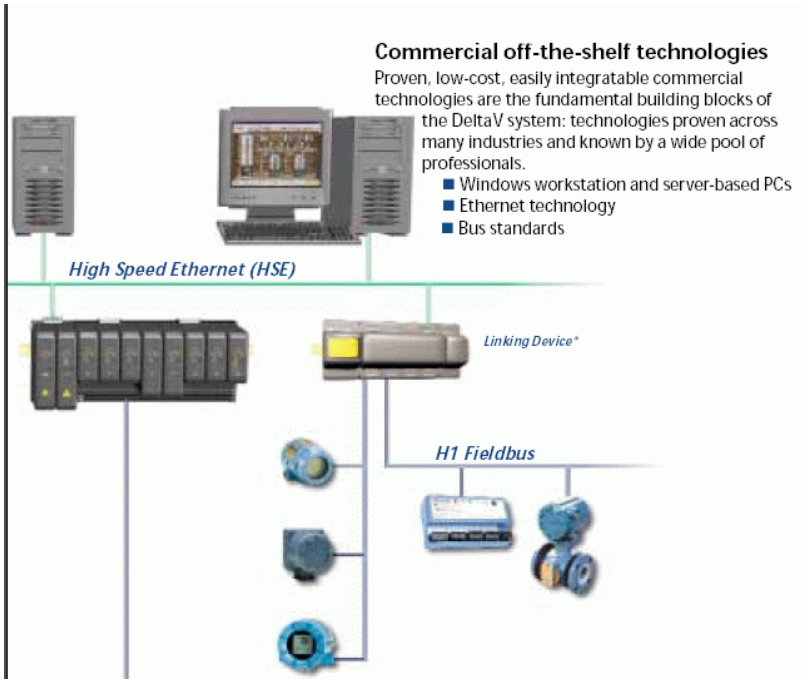
Scenario for a DAQ Architecture



Slow Control

I consider slow control to be part of DAQ

Safety relevant operation/monitoring done with DeltaV ProgramableLogicControl, used at LNGS by LUNA, Borexino, …



Rest like Temperature/HV: no standard defined, recycle existing hardware?

TempScan

200 channels for Pt-100 exist at MPI in Heidelberg with GPIB bus readout