DAQ status: FADC tests

Bernhard Schwingenheuer

MPI Heidelberg

Reminder of Febr meeting

First DAQ step: define the FADC option and built the system around it

Requirements: effective number of bits ENB > 10
~ 100 MHz sampling for analog bandwidth of 20 MHz
easy system integration
trigger generation
synchronization of modules
readout speed (for calibration runs)

idea of February meeting: test different FADC solutions and decide

Activities of Padova Group

An existing test bench for AGATA R&D measurements:
Hardware and Software for Data Taking and Analysis

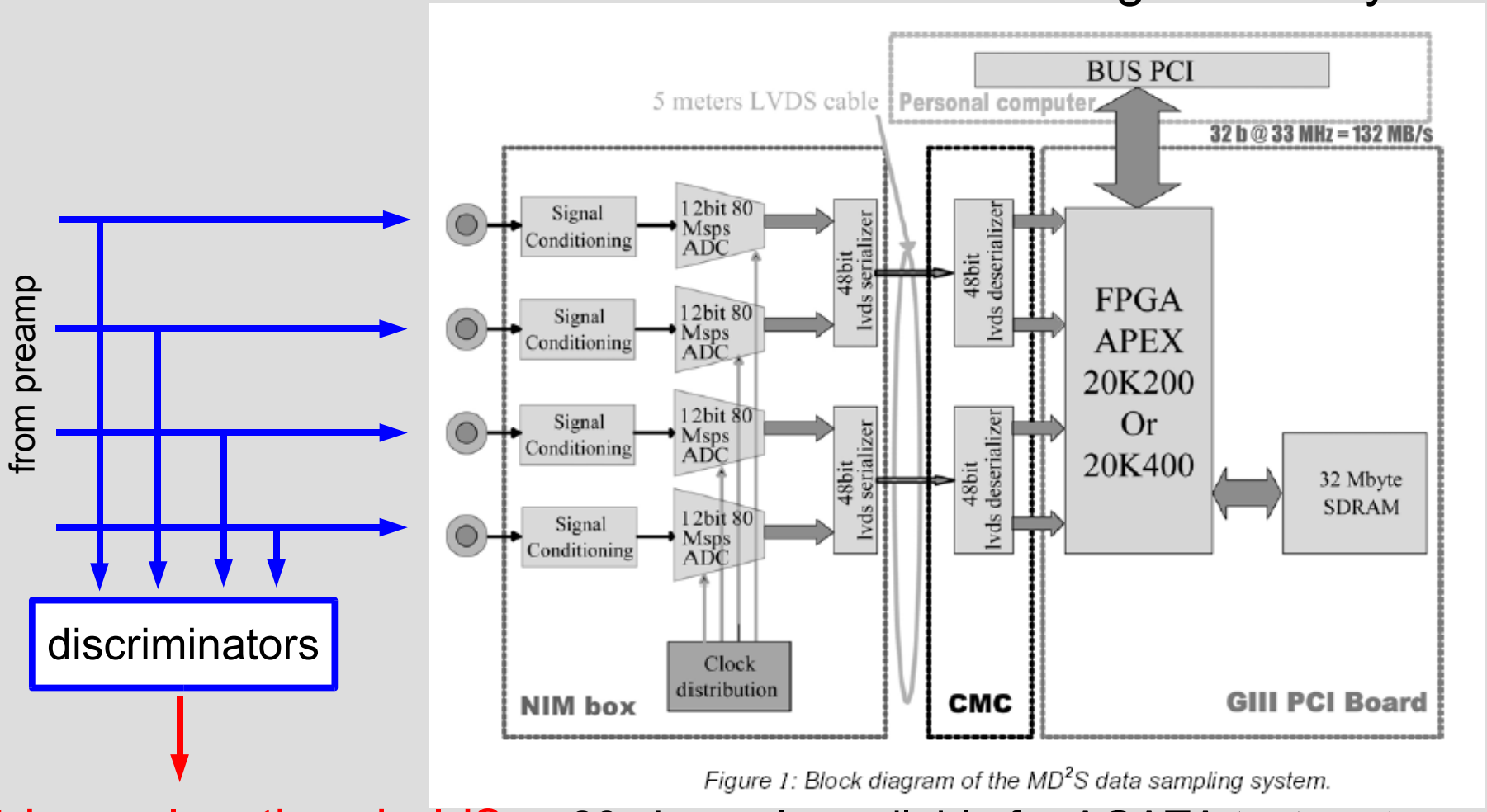
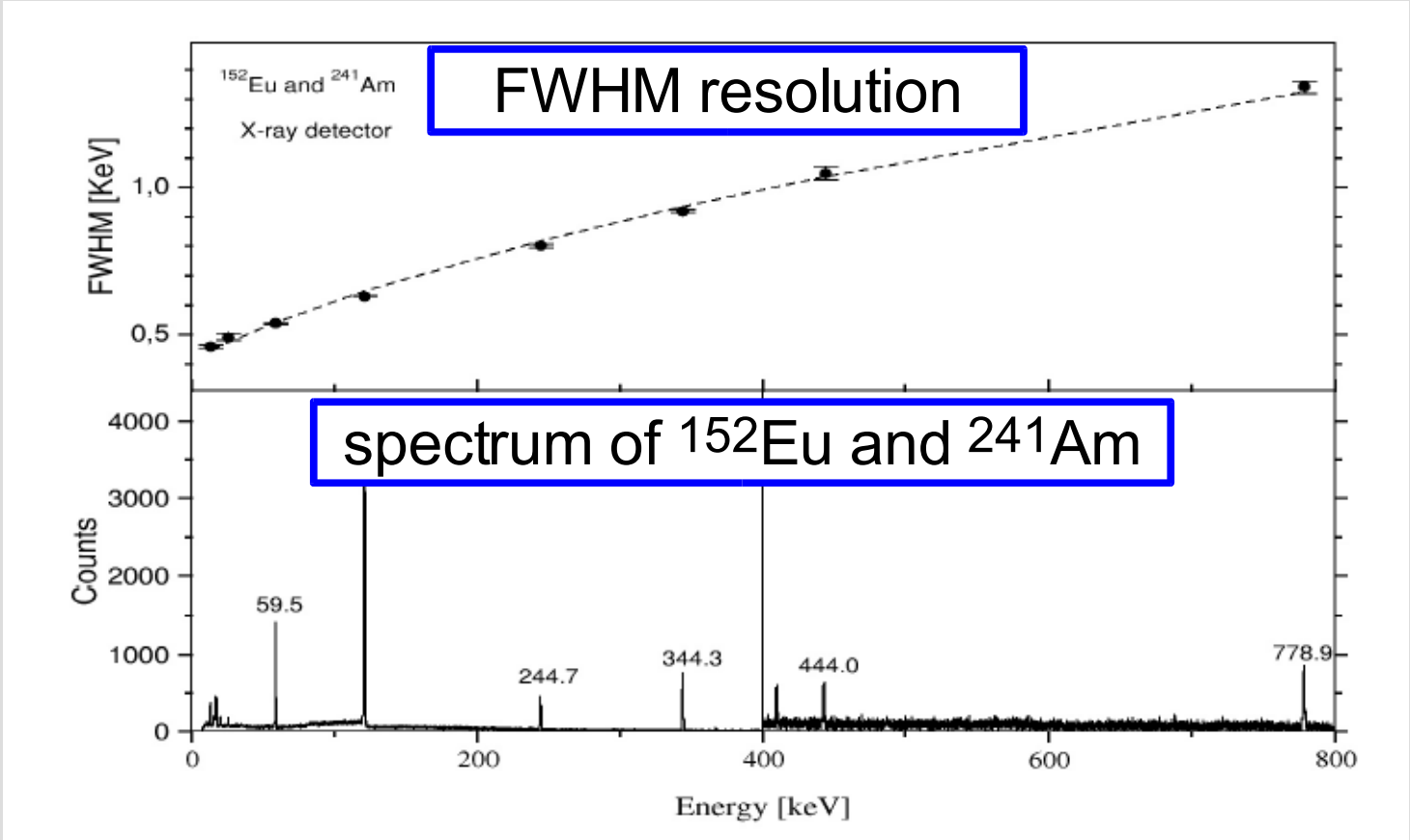


Figure 1: Block diagram of the MD²S data sampling system.

28 channels available for AGATA test system

Tests in Padova with X-ray source



Temperature stability:
from position of 344keV
for 3 K Temp drift
→ 0.3 LSB shift
(12 bit FADC)

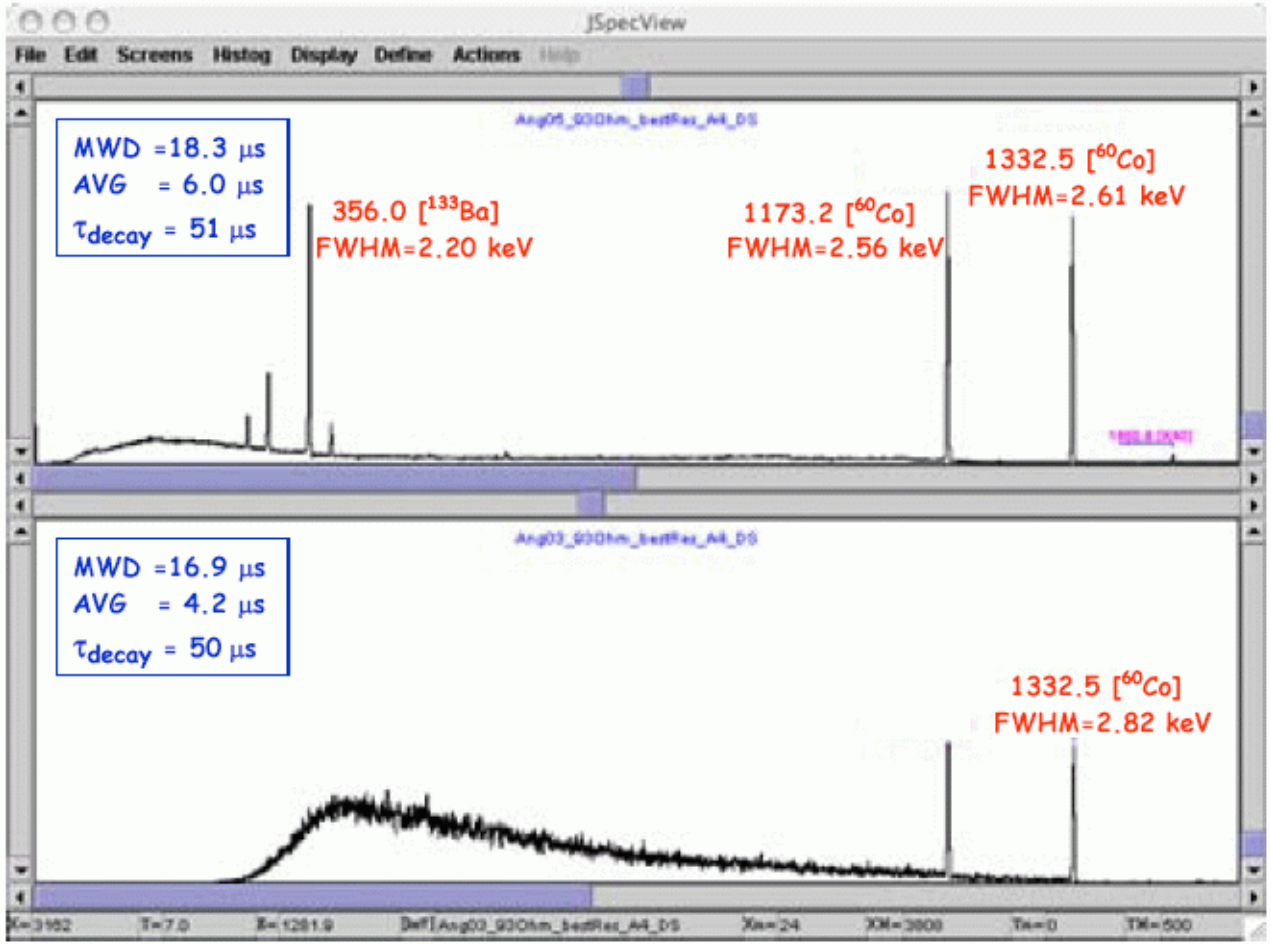
Uniformity:
resolution of all
channels very similar

Integral non-linearity:
< 0.5 LSB (line pos.)

Cross talk:
< 90 dB

Tests at LNGS with Ang3 and Ang5

^{60}Co & ^{133}Ba spectrum



Resolution of 1332 keV:

ORTEC MCA ~ 3 keV
with 6 µsec shaping

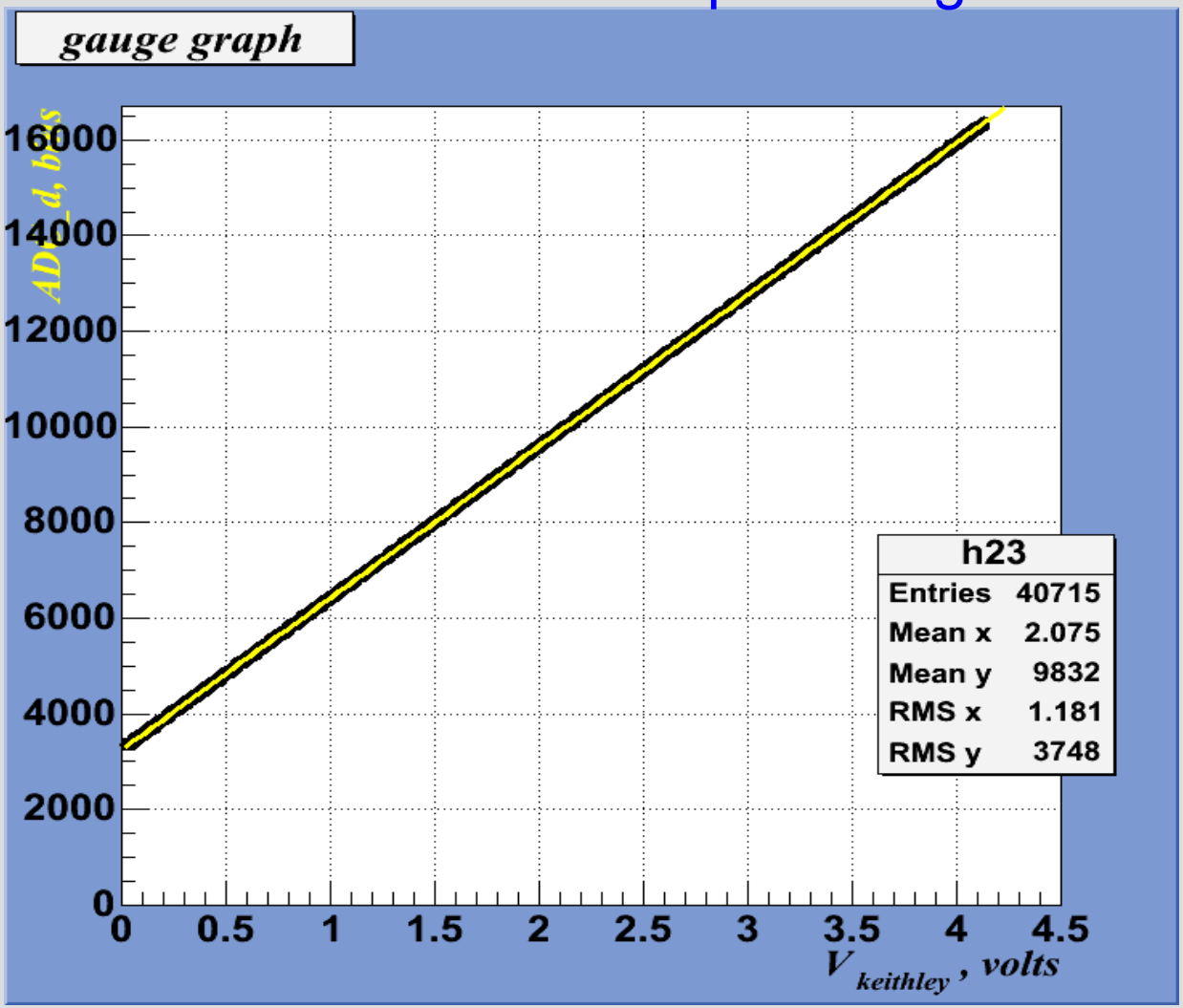
digital shaping including
baseline drift correction
2.6 – 2.8 keV,
big improvement

Pulse Shape:
for 300 nsec rise time
64 MHz fast enough

Conclusion: working system for Ge detectors!

Tests of Struck SIS3301 FADC

ADC count versus input voltage



ADC count = avg of 1000 samples, RMS of samples ~ 1.3 LSB

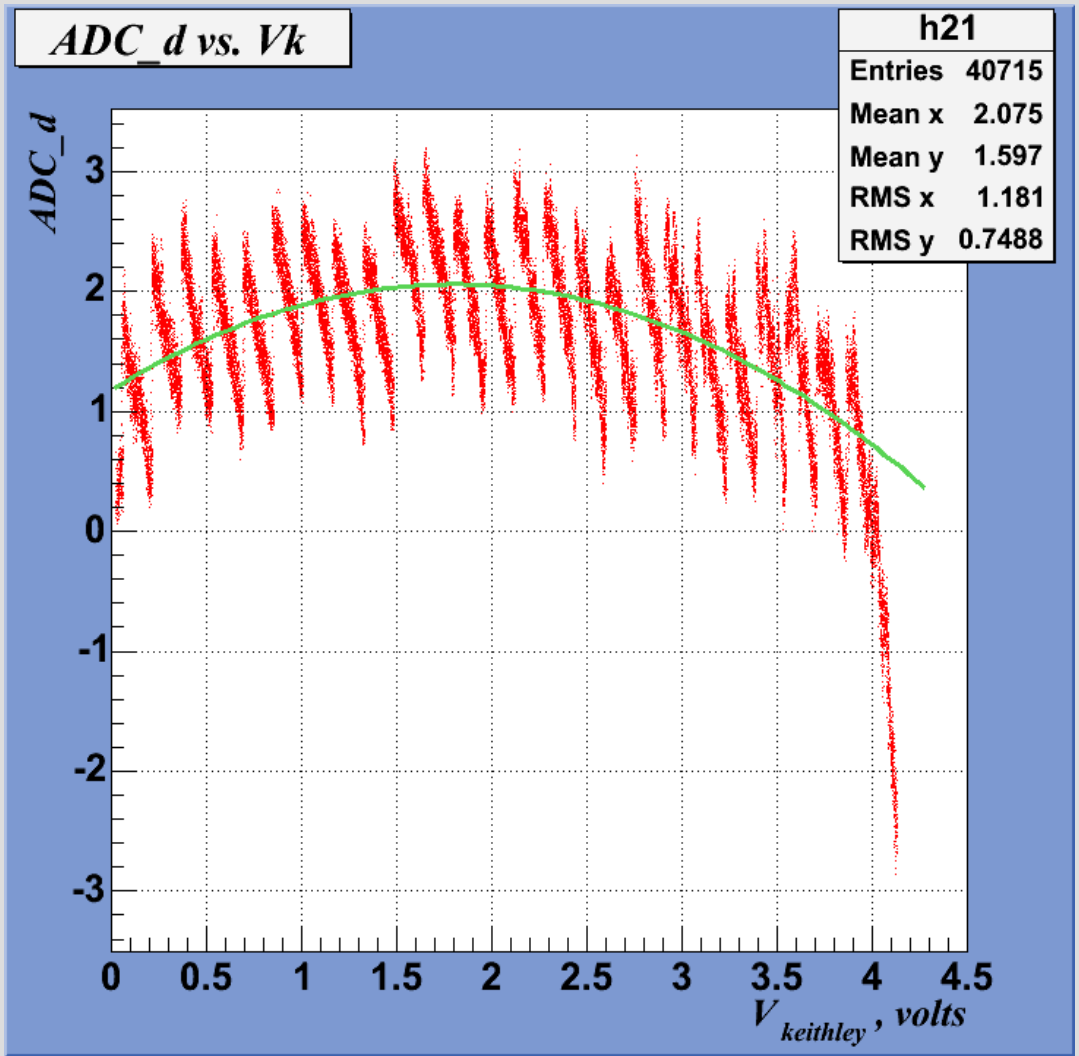
Characteristics:
8 channel VME module,
14 bit FADC
100 MHz sampling

internal trigger after digital noise filtering

all measurements done by Alexander Burenkov

Non-linearities

Residual ADC count vs voltage:
after subtraction of linear fit

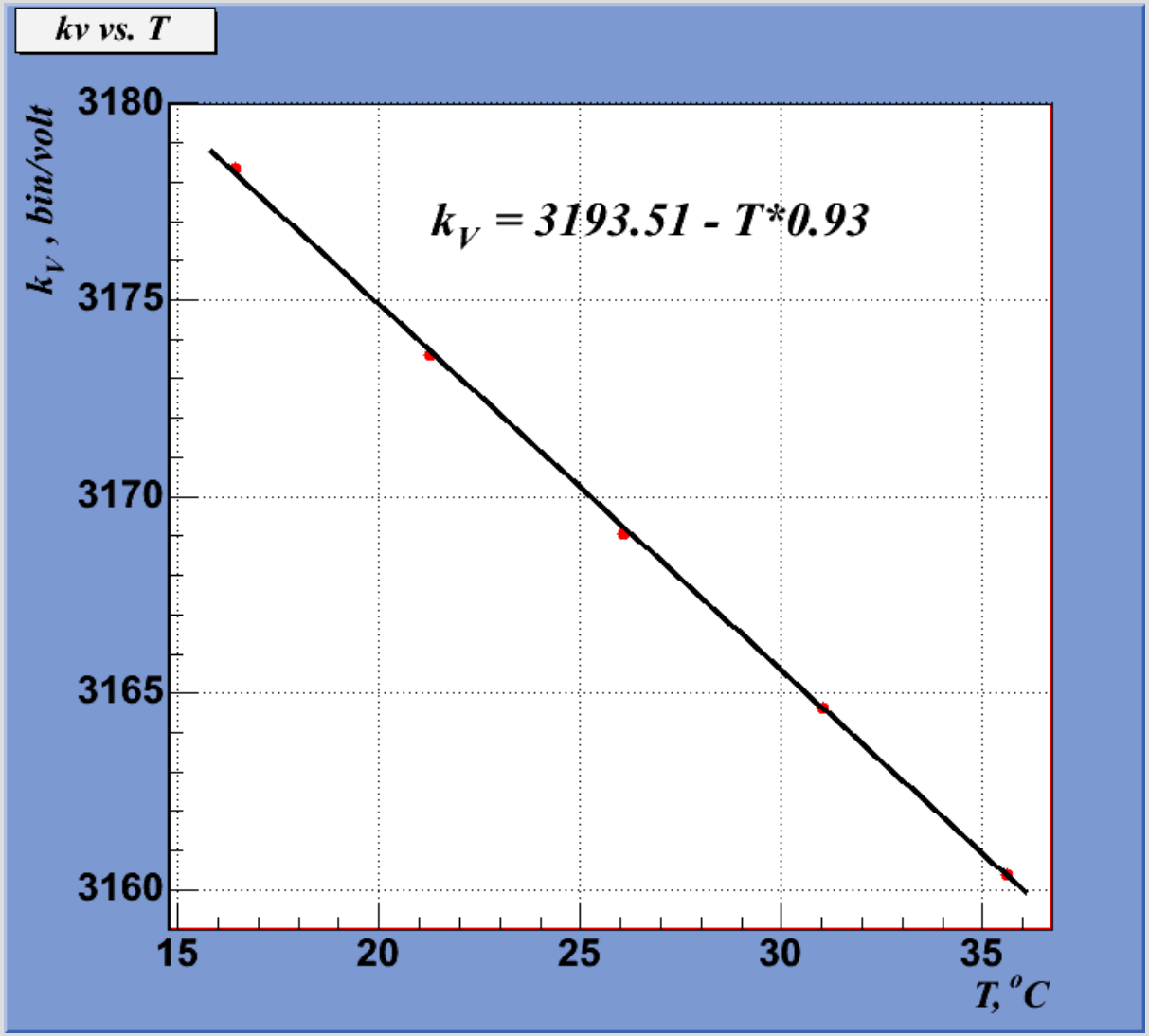


differential non-linearity ± 1LSB

integral non-linearity ±0.5 LSB

Temperatur drifts

ADC count per Volt versus temperature

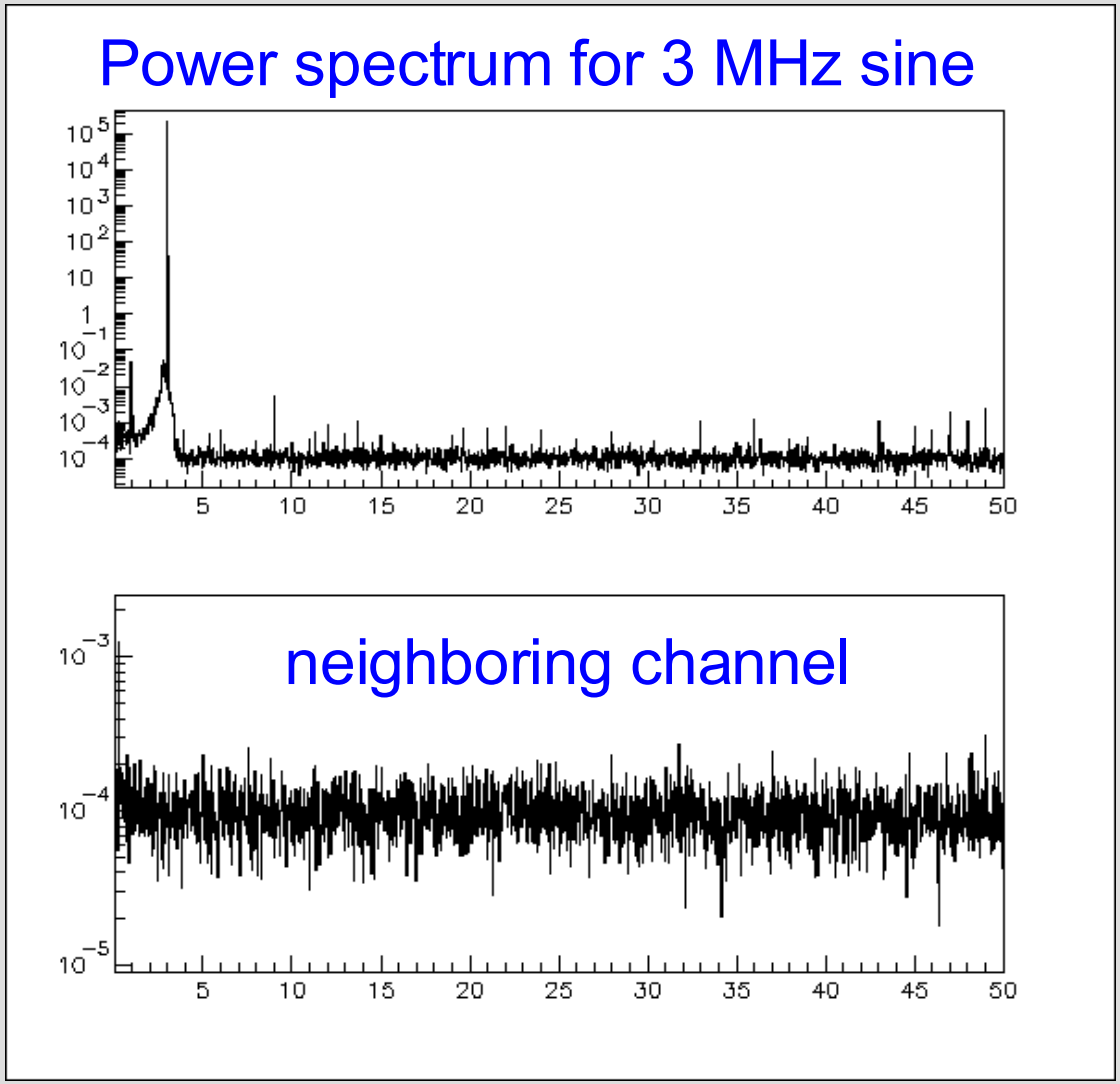


1 K change: – 0.9 LSB / Volt

example:
- 5 MeV full range (5 Volt)
- 1 K temp change
- 2 MeV signal drift = 1.8 LSB
  = 0.6 keV (< 3 MeV FWHM)

need temperature controlled room for analog electronics = part of the electronics lab should be a temperature controlled Faraday cage

Fourier Transformation



good signal to noise

no cross talk visible

Comparison MD²S - SIS3301

(other options XIA & Joerger not yet tested)

	MD²S	SIS3301
analog performance (ENB, ...)	✓	✓
sampling frequency ~ 100 MHz	✓	✓
synchronization: clock, trigger	✓	✓
trigger generation	external	internal
low trigger threshold	?	✓
analog signal processing (anti-aliasing, amplification)	internal	external
space requirement	32 ch / 10U	128 ch / 12U
price / channel	200 Euro	< 600 Euro
good for phase I	✓	✓
good for phase II	Probably not according to Carlos	✓

Summary

MD^{2}S is a working system, can be used for phase I (except low trg threshold?)

Padova group offers to duplicate existing system for GERDA phase I,
adjustments are possible (e.g. internal trigger since new FPGA is larger),
not a good system for phase II,
request: need decision NOW to get funding for next year

Struck SIS3301 is a working solution for phase I and phase II, 16 channels in hand,
readout software exists, analog input amplifier needs to be tested/optimized

REMINDER after all the discussion on the FADC:
FADC is only a “small” part of the DAQ + electronics system:
- control software for starting data taking (low + high voltage, FADC, data quality)
- slow control for monitoring temperatures, Rn concentrations, ...
- data bases
- analysis framework
- interface to Monte Carlo

need contributions to all topics, everyone is highly welcome with their expertise